

Power & Heat

ODSA Project Workshop March 28, 2019 Ali Husain, ON Semiconductor

Consume. Collaborate. Contribute.

Topics

POC 1.0

- Power Distribution
- Power Conversion
- Thermal Budgeting
- Differential thermal expansion (reliability)

FUTURE

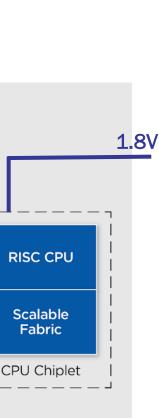
- Active Interposer
- Integrate Passive Components
- PMIC Chiplets



Power Architecture

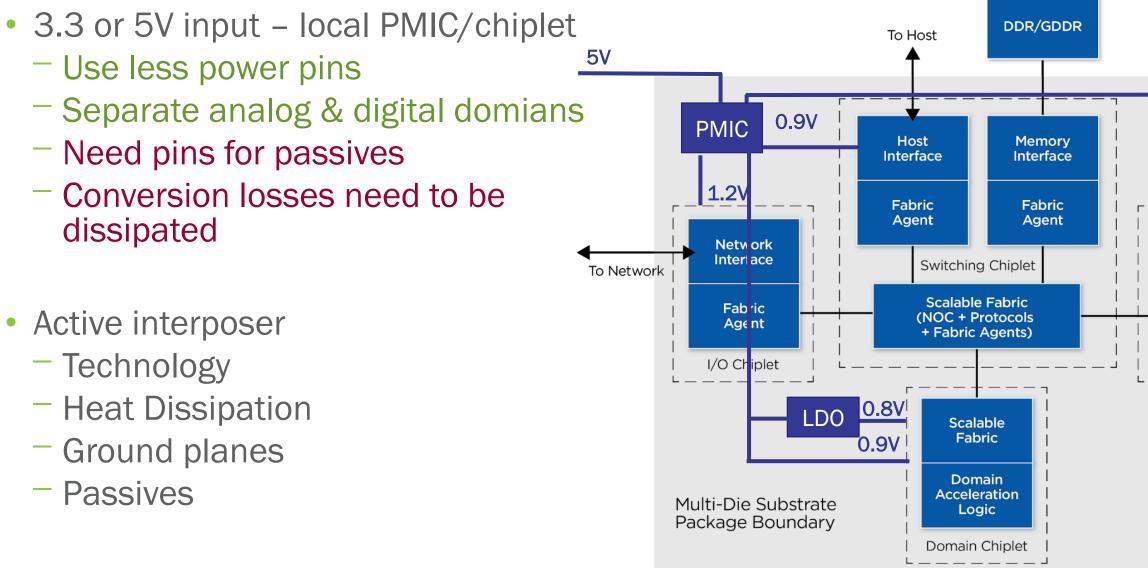
For Intel Cores, high power DDR/GDDR To Host input (>100A) at 1.8V **1.8**V Memory Host Interface Interface On-chip regulator converts from 1.2/3.3VFabric Fabric $1.8V \rightarrow 0.9V$ (unregulated) Agent Agent Network Interface Switching Chiplet To Network Scalable Fabric Fabric (NOC + Protocols Agent + Fabric Agents) **Digital & Analog Domains?** I/O Chiplet 0.9V Scalable Fabric Domain Acceleration Multi-Die Substrate Logic Package Boundary Domain Chiplet

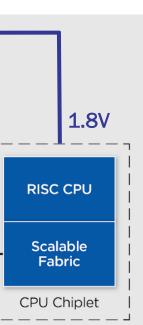
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Power Architecture – Future?

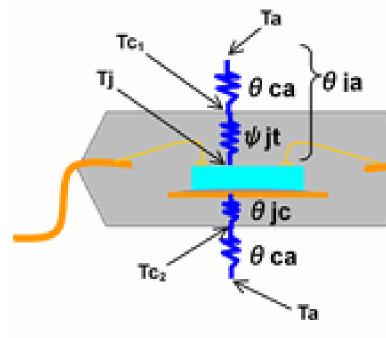






Heat

- Thermal Budgeting
- Temperature Sensors
- Chiplet performance vs. temperature
- Local Heating Effects
- → Power/Thermal Management Controller







Chiplet Necessary Specifications

- Input Voltage
- Max & Typical Supply Current (workload vs. current)
- R_{th} to interposer, case
- Power limiting functionality, speed
- PMBus or SVID interface?





