
Topics

POC 1.0

• Power Distribution
• Power Conversion
• Thermal Budgeting
• Differential thermal expansion (reliability)

FUTURE

• Active Interposer
• Integrate Passive Components
• PMIC Chiplets
Power Architecture

For Intel Cores, high power input (>100A) at 1.8V

On-chip regulator converts from 1.8V → 0.9V (unregulated)

Digital & Analog Domains?
Power Architecture – Future?

- 3.3 or 5V input – local PMIC/chiplet
  - Use less power pins
  - Separate analog & digital domains
  - Need pins for passives
  - Conversion losses need to be dissipated

- Active interposer
  - Technology
  - Heat Dissipation
  - Ground planes
  - Passives
Heat

- Thermal Budgeting
- Temperature Sensors
- Chiplet performance vs. temperature
- Local Heating Effects

→ Power/Thermal Management Controller
Chiplet Necessary Specifications

- Input Voltage
- Max & Typical Supply Current (workload vs. current)
- $R_{th}$ to interposer, case
- Power limiting functionality, speed
- PMBus or SVID interface?
(a) Passive Interposer
(b) Active Interposer