Layerscape Series: Scalability and Flexibility
Broadest Portfolio of Arm based SoC Devices

Scalable series of **Multicore** ARM-based SoC Families

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**LS1012A**
- A53
- 64-bit ARM
- 2Gbps Pkt
- GE, PCIe, SATA
- 1-2W

**LS1021A**
- 2x A7
- 32-bit ARM
- 3x GE
- Gen2 PCIe
- 2W

**LS1024A**
- 2x A9
- 32-bit ARM
- 2Gbps Pkt
- 2Gbps Crypto
- 3-5W

**LS1023A**
- 2x A53
- 64-bit ARM
- 1x10GE
- Gen2 PCIe
- 3.5-5W

**LS1026A**
- 2x A72
- 64-bit ARM
- 1x10GE
- Gen2 PCIe
- 6-10W

**LS1028A**
- 2x A72
- 64-bit ARM
- 1x10GE
- Integrated GPU
- Gen2 PCIe
- 4-9W

**LS1038A**
- 4x A53
- 64-bit ARM
- 1x10GE
- Gen2 PCie
- 6-10W

**LS1046A**
- 4x A72
- 64-bit ARM
- 2x 2.5/10GE
- Gen3 PCIe
- 5x 1GbE
- Gen2 PCie
- 8-12W

**LS1048A**
- 4x A72
- 64-bit ARM
- 2x 2.5/10GE
- Gen3 PCIe
- 5x 1GbE
- Gen3 PCie
- 15-20W

**LS1088A**
- 8x A53
- 64-bit ARM
- 8x 1/2.5/10GE
- Gen3 PCIe
- 8x 1GbE
- Gen3 PCie
- 20-35W

**LS2048A**
- 8x A72
- 64-bit ARM
- 8x 1/2.5/10GE
- Gen3 PCIe
- 8x 1GbE
- Gen3 PCie
- 20-35W

**LS2088A**
- 16x A72
- 64-bit ARM
- 16x 1/2.5/10GE
- Gen3 PCIe
- 16x 1/2.5/10GbE
- Gen3/4 PCIe
- 20-30W

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**Software Compatible**

**Expanded series for performance, power efficiency and lower BOM**
### Core Complex
- 16x 64-bit Cortex-A72 with Neon SIMD engine
- CPU Speed up to 2200 MHz
- Parity and ECC protected 48 KB L1 instruction and 32 KB L1 data cache
- 1 MB L2 cache with ECC protection/Cluster
- 8 MB Platform Cache

### Basic peripheral and Interconnect
- 2x USB 3.0 controllers with integrated PHY
- 2x eSDHC controller supporting SD 3.0 and eMMC 4.5 modes

### Networking elements
- Packet parsing, classification, and distribution
- Queue Management for scheduling, packet sequencing and congestion management
- Hardware buffer management for buffer allocation and de-allocation
- Data compression
- Data Center Bridging Support (iSCSI), TLV, DCBx, ETS(802.1Qaz), PFC(802.1Qbb)
- L2 Switching with 1G, 2.5G, 10G, 25G, 40G, 50G and 100G Ethernet
- Up to two RGMII interfaces
- 6x PCI Express Gen 4 controllers (2 with SR-IOV support)
- 4x SATA Gen 3.0 controllers

### Accelerators and Memory Control
- 2x 64-bit DDR4 Controller with ECC support up to 3.2 GT/s
- Security Engine (SEC)
- Security Subsystem: Secure boot, ARM Trust zone and security monitor

### Package & Qualification
- 16nm FinFet Compact
- 40 x 40mm Flip chip, 1mm pitch, 1517 pins
- Estimated Power 30W VDD (thermal) at 105C, 2.2GHz
- Commercial and Industrial temperature

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<th>Security</th>
<th>Core Complex</th>
<th>Networking Elements</th>
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<td>Security Engine</td>
<td>A72 A72 A72 A72 A72 A72 A72 A72</td>
<td>1Gbe 25Gbe</td>
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<tr>
<td>ARM Trust Zone</td>
<td>A72 A72 A72 A72 A72 A72 A72 A72</td>
<td>1Gbe 25Gbe</td>
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<td>1 MB L2 Cache 1 MB L2 Cache 1 MB L2 Cache 1 MB L2 Cache 1 MB L2 Cache 1 MB L2 Cache 1 MB L2 Cache</td>
<td>1Gbe 25Gbe</td>
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<td>Secure Boot</td>
<td>72-bit (64-bit with ECC Memory Controller)</td>
<td>10 Gbe 10 Gbe</td>
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<td>Power Management</td>
<td>72-bit (64-bit with ECC Memory Controller)</td>
<td>100Gbe 100Gbe</td>
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### Standard interfaces
- 2x SD/eMMC
- 3x SPI
- 4x UART, 8x I2C
- GPIO, JTAG
- FlexSPI

### Accelerators and Memory Control
- 8 MB Platform Cache
- Queue-Buffer Manager
- Data Compression Engine (100Gbps)
- x8 Gen4 PCIe SATA 3.0
- x8 Gen4 PCIe SATA 3.0
- x4 Gen4 PCIe SATA 3.0
- x4 Gen4 PCIe SATA 3.0
- x4 Gen4 PCIe USB 3.0 w/ PHY
- x4 Gen4 PCIe USB 3.0 w/ PHY

### Coherent Interconnect
- 1 MB L2 Cache
- 1 MB L2 Cache
- 1 MB L2 Cache
- 1 MB L2 Cache
- 1 MB L2 Cache
- 1 MB L2 Cache

### Memory Controller
- 1 MB L2 Cache
- 1 MB L2 Cache
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- 1 MB L2 Cache
- 1 MB L2 Cache

### Accelerators and Memory Control
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