Cost Modeling Analysis for Heterogeneous Integration of Chiplets
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Problem Statement

- Heterogeneous integration of chiplets is the new reality
- Need to quantify process and yield enhancements of chiplets
  - Creative disaggregation of a SoC
  - Cost, power, performance and area
- No available commercially or in open-source format for cost modeling
  - 1st pass analysis of the advantages/disadvantages
- Limited customization in commercial models

OPEN POSSIBILITIES.

SERVER

Need a common Chiplet Economic Model to accelerate collaboration
Motivation

• Need to understand the chiplet business case
• This requires a good cost model that accounts for:
  • Geometric scenario
  • Material costs
  • Test costs
  • Assembly costs
  • Other relevant costs associated with SoC development

Proposed Solution:

• Open-source model to enable community to model cost and tradeoffs
• Allows for customization per the needs of the organization
Features of the Model

- Phased Model Development:
  - Phase 1: Spreadsheet-based: rough model and a detailed model
  - Phase 2: Python script-based: account for uncertainties, sensitivity analysis etc.
- Allows for user to override inputs – color coded to indicate this
- Ability to integrate different process nodes
- Allows the die to be integrated with passive silicon (like a silicon interposer)
- Can integrate up to 40 chiplets; can also use this for monolithic designs
- Yield for each process node calculated based on the defect density
- Bose-Einstein model or Murphy models included
- Assembly sequence and KGD costs captured in the model
Factors Considered for the Model

- Yield
- IP
- Quality
- Material
- Assembly Sequence
- NRE
- Time
- Operations
- KGD
- Assembly
- Mask Set

24+ variables included

OPEN POSSIBILITIES.
# Model Structure

## Model Input
- 40+ Chips/Chiplets
- Active or Passive Silicon
- Silicon Node
- Wafer Pricing, Yield
- Substrate
- Forecast Volumes
- Assembly Sequence
- Yield, KGD
- IP Cost
- ASP
- ... 24+ Variables

## Model Output
- Graphical Output
  - Line Chart
  - Pie Chart
- Pairwise Scenario Comparisons
- Total Cost and Unit Cost ($)
- 5 Year Projections
- % Contribution of:
  - BoM, KGD, Test, NRE, IP etc.
- Gross Margin ($, %) for given ASP
Three Test Cases

• Test Case 1: Monolithic vs. chiplet options for standard single die Flip Chip BGA
  • 12% extra silicon area
  • 32% less expensive

• Test Case 2: Integrating 16 chiplets onto a substrate using a passive interposer
  • 12% extra silicon area
  • 40% less expensive

• Test Case 3: Large ASIC integrated with 4 HBM vs. ASIC divided into 2 chiplets integrated with 4HBM
  • 8% extra silicon area
  • 30% less expensive
Scenario 1: To Chiplet or Not to Chiplet?

- Cost wise, should we split a monolithic die into two smaller ones?
- Several input parameters assumed in model
- No interposer

Option 1

- 5nm Die
- 25.8 x 25.8 mm

Option 2

- 5nm Die
  - 14.5 x 25.8 mm
- 5nm Die
  - 14.5 x 25.8 mm

12% Extra SoC Area
Scenario 1: To Chiplet or Not?

- Chiplets are **32% less expensive** than monolithic.
- **Cost Drivers:**
  - Material > KGD > NRE > Misc Cost > IP Interface > Operating Cost > Quality
  - Chiplets in this case make economic sense.
Scenario 1: To Chiplet or Not?

- Cost difference becomes much more significant as the shipment volume increases.
- Shipment forecast and volume can have a significant impact on the relative benefit.

### Year vs. Shipment Volume

<table>
<thead>
<tr>
<th>Year</th>
<th>Shipment Volume</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>100K</td>
</tr>
<tr>
<td>2</td>
<td>150K</td>
</tr>
<tr>
<td>3</td>
<td>250K</td>
</tr>
<tr>
<td>4</td>
<td>1M</td>
</tr>
<tr>
<td>5</td>
<td>1M</td>
</tr>
</tbody>
</table>

### Total Cost

- **Chiplet**
- **Monolithic**

- Year 1: 100K
- Year 2: 150K
- Year 3: 250K
- Year 4: 1M
- Year 5: 1M

**Cost ($)**

- Option 1
- Option 2

**Open Possibilities.**
Scenario 1: What about Uncertainty?

- Baseline assumes that the Silicon Wafer Defect Density is fixed (0.1)
- Defect densities are always uncertain for newer silicon nodes
- What if the defect density is higher or lower for each die in each option?

<table>
<thead>
<tr>
<th>Cost Savings by Using Chiplets</th>
<th>Worst Case DD (0.05)</th>
<th>Baseline (0.1)</th>
<th>Best Case (0.11)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$8 (Gain)</td>
<td>$308 (Gain)</td>
<td>$449 (Gain)</td>
</tr>
</tbody>
</table>

- 6.3% probability that the chiplet option would be on par or worse
- Other uncertainties like forecast volume, pricing, IP cost, etc.) can be considered
- Economically viable designs needs to consider uncertainties
Scenario 2: Large or Split Die with Chiplets?

Cost wise, should we split a monolithic die into two smaller ones?

Several input parameters assumed in model

No interposer
Scenario 2: Large or Split Die with Chiplets?

- Chiplets are **40% less expensive** than the monolithic version
- Cost Drivers:
  - Material > NRE > KGD > IP Interface > Misc Cost > Operating Cost > Quality
  - Main die split in this case makes economic sense.
## Scenario 2: Model Details

<table>
<thead>
<tr>
<th>Cost Category</th>
<th>Option 1</th>
<th></th>
<th></th>
<th></th>
<th>Option 2</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Yr 1</td>
<td>Yr 2</td>
<td>Yr 3</td>
<td>Yr 4</td>
<td>Yr 5</td>
<td>Yr 1</td>
<td>Yr 2</td>
<td>Yr 3</td>
</tr>
<tr>
<td>Total Unit Cost</td>
<td>$1,005.02</td>
<td>$975.57</td>
<td>$945.77</td>
<td>$914.77</td>
<td>$896.94</td>
<td>$571.90</td>
<td>$552.35</td>
<td>$532.56</td>
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<table>
<thead>
<tr>
<th>Cost Contribution ($ of Total Unit Cost)</th>
<th>Option 1</th>
<th></th>
<th></th>
<th></th>
<th>Option 2</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Yr 1</td>
<td>Yr 2</td>
<td>Yr 3</td>
<td>Yr 4</td>
<td>Yr 5</td>
<td>Yr 1</td>
<td>Yr 2</td>
<td>Yr 3</td>
<td>Yr 4</td>
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<tr>
<td>Material</td>
<td>$882.70</td>
<td>$865.47</td>
<td>$845.81</td>
<td>$826.06</td>
<td>$809.27</td>
<td>$476.59</td>
<td>$470.26</td>
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<tr>
<td>NRE</td>
<td>$23.50</td>
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<td>$0.00</td>
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<td>$0.00</td>
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<tr>
<td>KGD</td>
<td>$44.13</td>
<td>$43.27</td>
<td>$42.29</td>
<td>$41.30</td>
<td>$40.46</td>
<td>$16.88</td>
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<td>Quality</td>
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<td>$0.60</td>
<td>$0.59</td>
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<td>Operating Cost</td>
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<td>IP Interface Cost</td>
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<td>$11.00</td>
<td>$25.00</td>
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<td>$16.00</td>
<td>$11.50</td>
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<td>Misc Cost (Asy, Test)</td>
<td>$22.07</td>
<td>$22.07</td>
<td>$22.07</td>
<td>$22.07</td>
<td>$22.07</td>
<td>$22.07</td>
<td>$22.07</td>
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<td>Gross Margin ($)</td>
<td>-$5</td>
<td>$24</td>
<td>$54</td>
<td>$85</td>
<td>$103</td>
<td>-$5.02</td>
<td>$24.43</td>
<td>$54.23</td>
<td>$85.23</td>
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<tr>
<td>Gross Margin (%)</td>
<td>-0.50%</td>
<td>2.44%</td>
<td>5.42%</td>
<td>8.52%</td>
<td>10.31%</td>
<td>-0.50%</td>
<td>2.44%</td>
<td>5.42%</td>
<td>8.52%</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Cost Difference</th>
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</thead>
<tbody>
<tr>
<td>Option 1</td>
<td>-$433.12</td>
<td>-$423.22</td>
<td>-$413.21</td>
<td>-$403.60</td>
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<tr>
<td>Option 2</td>
<td>-$392.71</td>
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<td></td>
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</tbody>
</table>
Scenario 3: HBM with 1 or 2 Dies?

- Cost wise, should we split a monolithic die into two smaller ones?
- Several input parameters assumed in model
Scenario 3: HBM with 1 or 2 Dies?

- Chiplets-with-HBM is about **30% less expensive** than monolithic-with-HBM

- Cost Drivers:
  - Material > KGD > IP Interface > NRE > Misc. Cost
  - Main die split in this case makes economic sense.
Future Work

• Phase 1:
  • Simplified “toy” model will be added for beginners
  • More use cases and model vetting
  • Addition of more variables
  • Some default values per inputs from contributors

• Phase 2:
  • Python script-based model to capture more factors
  • Sensitivity analysis of critical factors: yield, pricing, volumes, etc.
  • Script could be incorporated into EDA tools for iterative design tradeoff analysis
Call to Action

• Model will be released periodically and latest version will be listed on the ODSA website

• Reach out to us:
  • If you are interested in developing the cost model
  • If you have an existing set of parameters that could be included
  • If you can help us share and evangelize the concept of an open cost model
Thank you!