OPEN POSSIBILITIES.

Cost Modeling Analysis for Heterogeneous Integration of Chiplets

OCP GLOBAL SUMMIT
NOVEMBER 9-10, 2021

Cost Modeling Analysis for Heterogeneous Integration of Chiplets

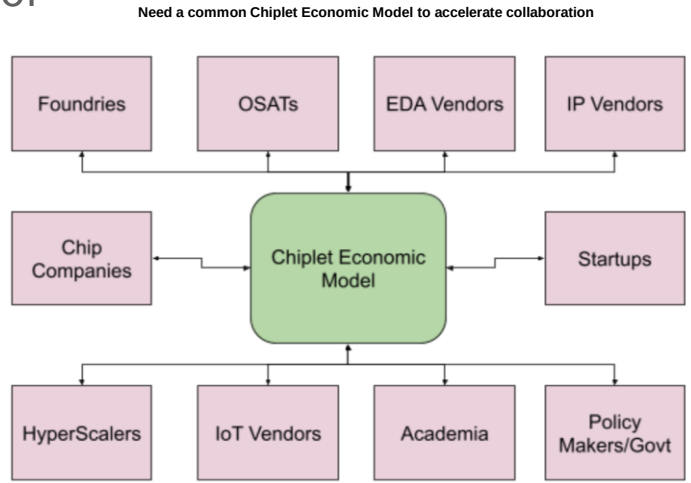
Mudasir Ahmad, Adv. Tech Development & Sourcing, Google
Javier DeLaCruz, Central Engineering, ARM
Anu Ramamurthy, Adv. Engineering Services, Microchip Technology

OPEN POSSIBILITIES.

OCP GLOBAL SUMMIT
NOVEMBER 9-10, 2021

Problem Statement

- Heterogeneous integration of chiplets is the new reality
- Need to quantify process and yield enhancements of chiplets
  - Creative disaggregation of a SoC
  - Cost, power, performance and area
- No available commercially or in open-source format for cost modeling
  - 1st pass analysis of the advantages/disadvantages
- Limited customization in commercial models



OPEN POSSIBILITIES.

Motivation

- Need to understand the chiplet business case
- This requires a good cost model that accounts for:
  - Geometric scenario
  - Material costs
  - Test costs
  - Assembly costs
  - Other relevant costs associated with SoC development

Proposed Solution:

- Open-source model to enable community to model cost and tradeoffs
- Allows for customization per the needs of the organization

Features of the Model

- Phased Model Development:
  - Phase 1: Spread sheet-based: rough model and a detailed model
  - Phase 2: Python script-based: account for uncertainties, sensitivity analysis etc.
- Allows for user to override inputs – color coded to indicate this
- Ability to integrate different process nodes
- Allows the die to be integrated with passive silicon (like a silicon interposer)
- Can integrate up to 40 chiplets; can also use this for monolithic designs
- Yield for each process node calculated based on the defect density
- Bose-Einstein model or Murphy models included
- Assembly sequence and KGD costs captured in the model

Factors Considered for the Model

SERVER

Yield

IP

Quality

Material

Test

KGD

Assembly Sequence

Time

Operations

NRE

Assembly

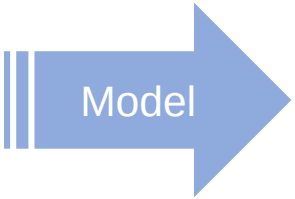
Mask Set

24+ variables included

Model Structure

Model Input

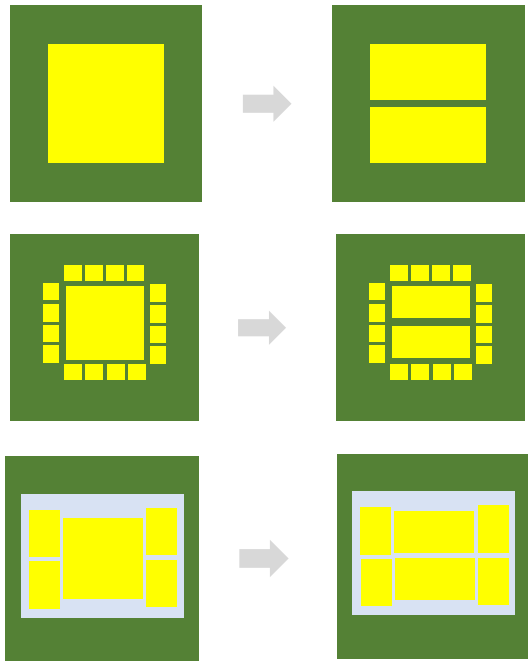
- 40+ Chips/Chiplets
- Active or Passive Silicon
- Silicon Node
- Wafer Pricing, Yield
- Substrate
- Forecast Volumes
- Assembly Sequence
- Yield, KGD
- IP Cost
- ASP
- … 24+ Variables



Model Output

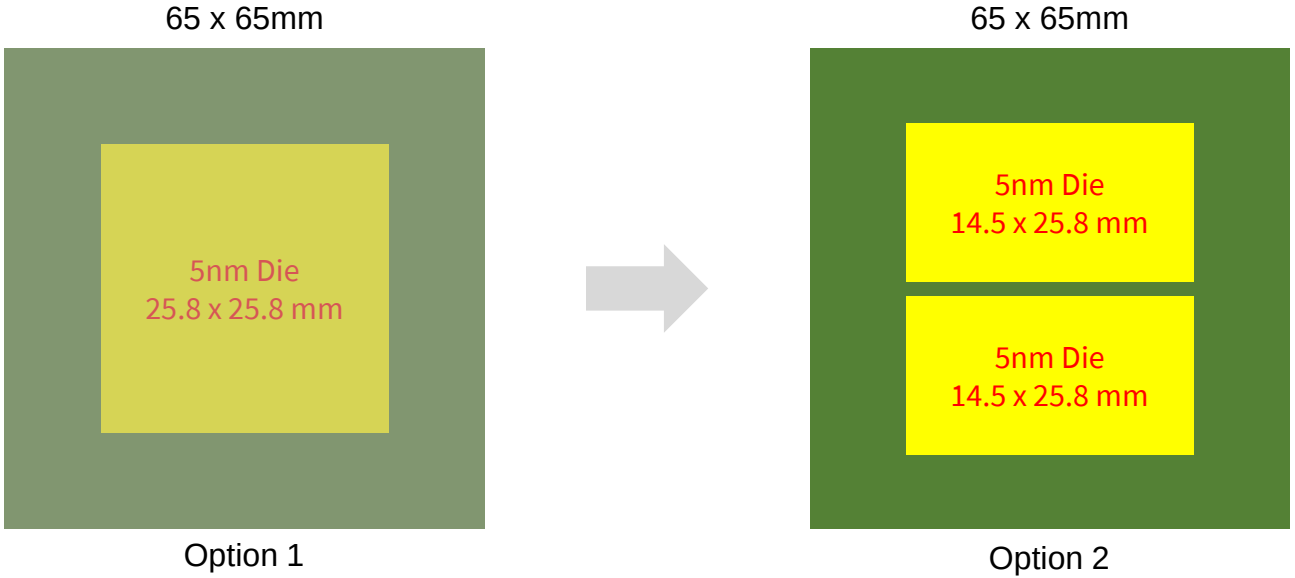
- Graphical Output
  - Line Chart
  - Pie Chart
- Pairwise Scenario Comparisons
- Total Cost and Unit Cost ($)
- 5 Year Projections
- % Contribution of:
  - BoM, KGD, Test, NRE, IP etc.
- Gross Margin ($, %) for given ASP

Three Test Cases



- Test Case 1: Monolithic vs. chiplet options for standard single die Flip Chip BGA
  - 12% extra silicon area
  - 32% less expensive
- Test Case 2: Integrating 16 chiplets onto a substrate using a passive interposer
  - 12% extra silicon area
  - 40% less expensive
- Test Case 3: Large ASIC integrated with 4 HBM vs. ASIC divided into 2 chiplets integrated with 4HBMs
  - 8% extra silicon area
  - 30% less expensive

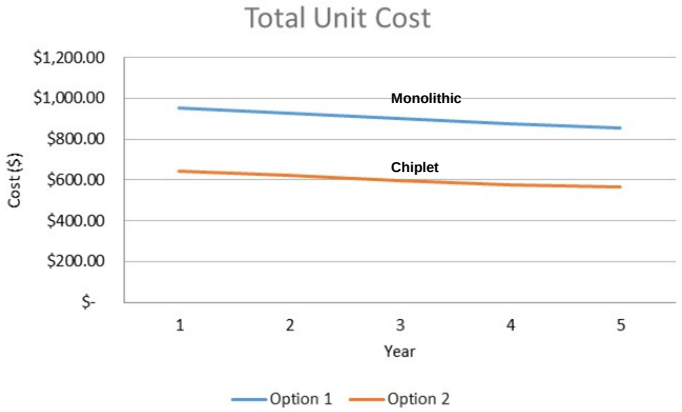
Scenario 1: To Chiplet or Not to Chiplet?



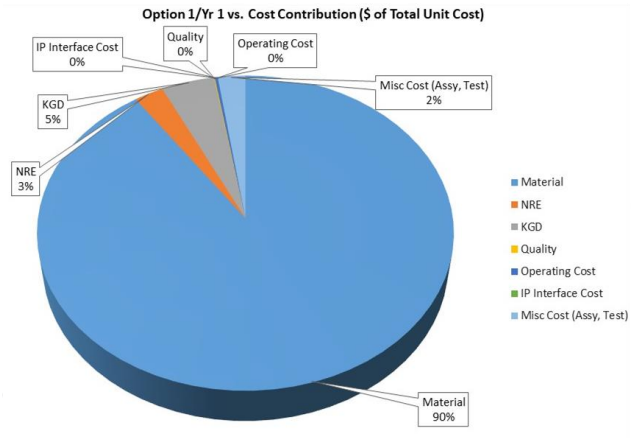
12% Extra SoC Area

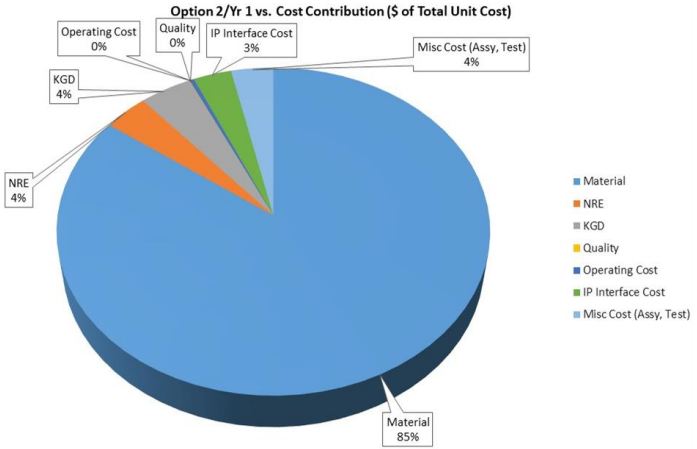
- Cost wise, should we split a monolithic die into two smaller ones?
- Several input parameters assumed in model
- No interposer

Scenario 1: To Chiplet or Not?

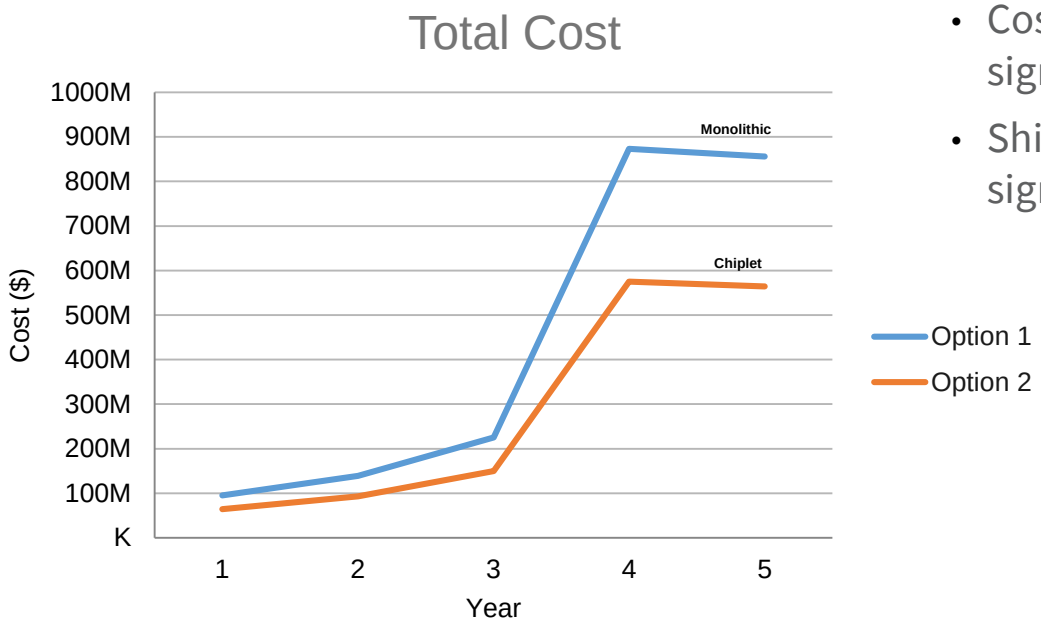


- Chiplets are 32% less expensive than monolithic
- Cost Drivers:
  - Material > KGD > NRE > Misc Cost > IP Interface > Operating Cost > Quality
- Chiplets in this case make economic sense.





Scenario 1: To Chiplet or Not?



- Cost difference becomes much more significant as the shipment volume increases
- Shipment forecast and volume can have a significant impact on the relative benefit

Year	Shipment Volume
1	100K
2	150K
3	250K
4	1M
5	1M

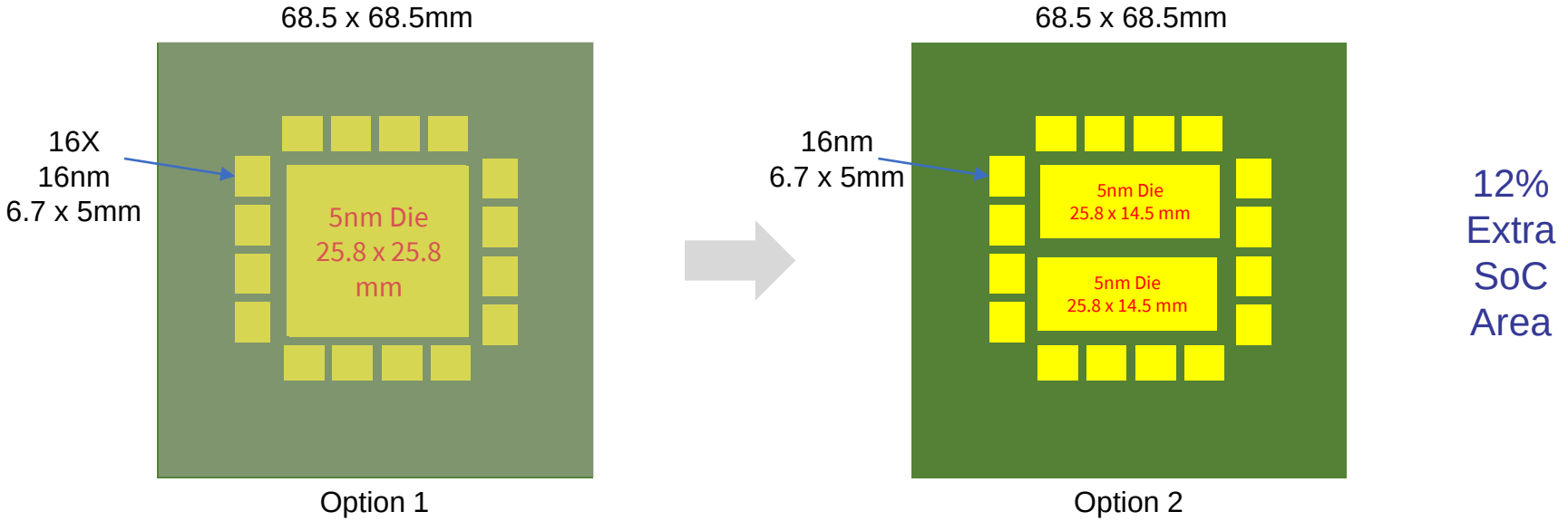
Scenario 1: What about Uncertainty?

- Baseline assumes that the Silicon Wafer Defect Density is fixed (0.1)
- Defect densities are always uncertain for newer silicon nodes
- What if the defect density is higher or lower for each die in each option?

	Worst Case DD (0.05)	Baseline (0.1)	Best Case (0.11)
Cost Savings by Using Chiplets	$8 (Gain)	$308 (Gain)	$449 (Gain)

- 6.3% probability that the chiplet option would be on par or worse
- Other uncertainties like forecast volume, pricing, IP cost, etc.) can be considered
- Economically viable designs needs to consider uncertainties

Scenario 2: Large or Split Die with Chiplets?

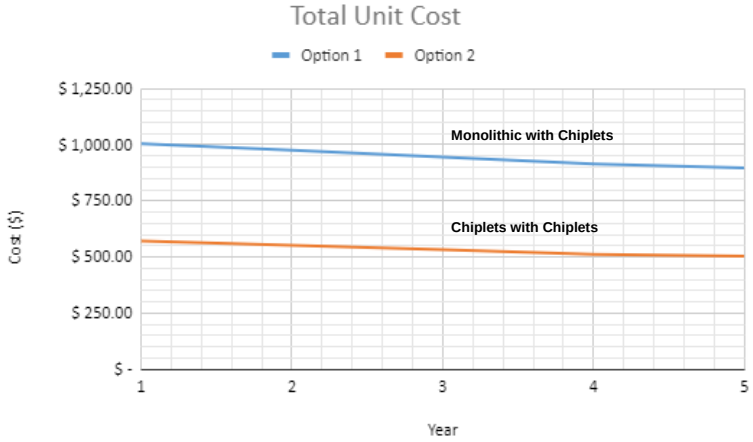


12% Extra SoC Area

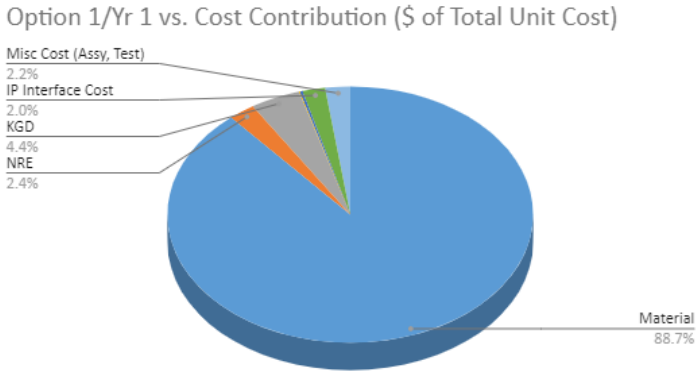
- Cost wise, should we split a monolithic die into two smaller ones?
- Several input parameters assumed in model
- No interposer

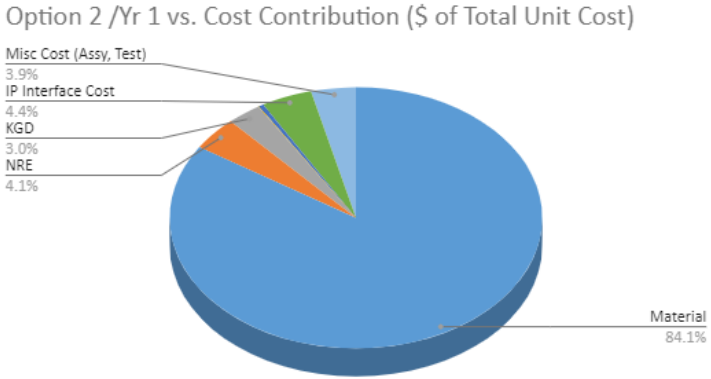
OPEN POSSIBILITIES.

Scenario 2: Large or Split Die with Chiplets?



- Chiplets are **40% less expensive** than the monolithic version
- Cost Drivers:
  - Material > NRE > KGD > IP Interface > Misc Cost > Operating Cost > Quality
- Main die split in this case makes economic sense.





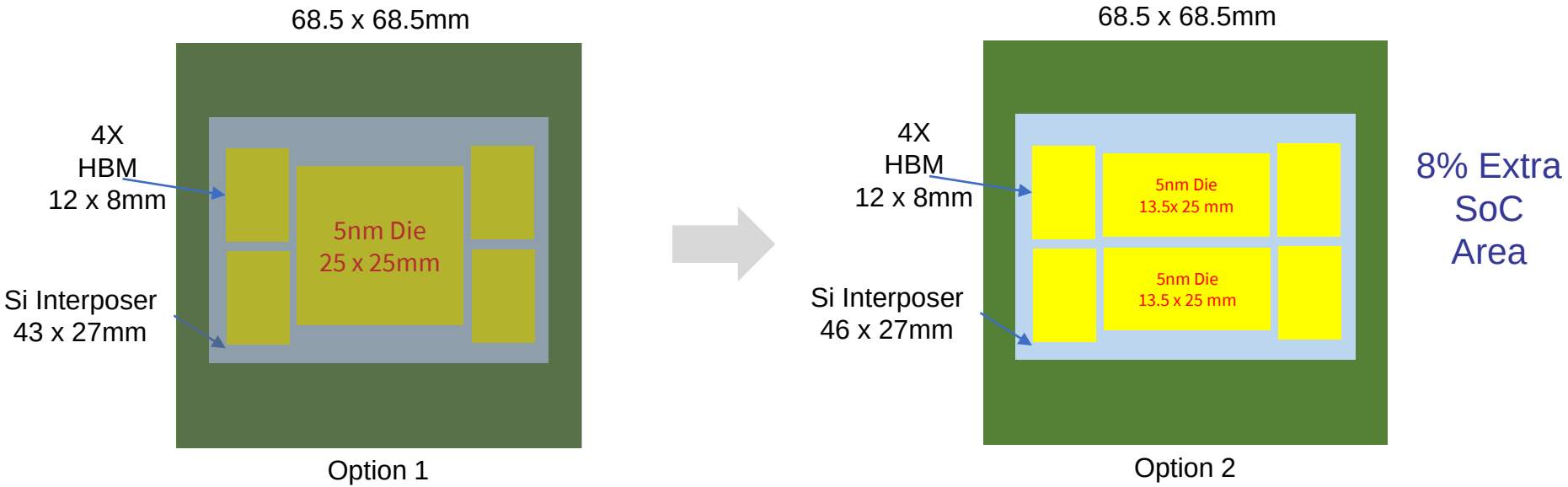
Scenario 2: Model Details

	Option 1					Option 2				
Cost Category	**Yr 1**	**Yr 2**	**Yr 3**	**Yr 4**	**Yr 5**	**Yr 1**	**Yr 2**	**Yr 3**	**Yr 4**	**Yr 5**
Total Unit Cost	$ 1,005.02	$ 975.57	$ 945.77	$ 914.77	$ 896.94	$ 571.90	$ 552.35	$ 532.56	$ 511.16	$ 504.23

	Option 1					Option 2				
Cost Contribution ($ of Total Unit Cost)	**Yr 1**	**Yr 2**	**Yr 3**	**Yr 4**	**Yr 5**	**Yr 1**	**Yr 2**	**Yr 3**	**Yr 4**	**Yr 5**
Material	$882.70	$865.47	$845.81	$826.06	$809.27	$476.59	$470.26	$461.28	$452.00	$445.47
NRE	$23.50	$0.00	$0.00	$0.00	$0.00	$23.50	$0.00	$0.00	$0.00	$0.00
KGD	$44.13	$43.27	$42.29	$41.30	$40.46	$16.88	$16.57	$16.12	$15.65	$15.33
Quality	$0.63	$0.62	$0.60	$0.59	$0.58	$0.25	$0.25	$0.24	$0.24	$0.23
Operating Cost	$2.40	$2.40	$2.40	$2.40	$2.40	$2.40	$2.40	$2.40	$2.40	$2.40
IP Interface Cost	$20.00	$16.67	$14.00	$11.00	$11.00	$25.00	$20.00	$16.00	$11.50	$11.50
Misc Cost (Assy, Test)	$22.07	$22.07	$22.07	$22.07	$22.07	$22.07	$22.07	$22.07	$22.07	$22.07
Gross Margin ($)	-$5	$24	$54	$85	$103	-$5.02	$24.43	$54.23	$85.23	$103.06
Gross Margin (%)	-0.50%	2.44%	5.42%	8.52%	10.31%	-0.50%	2.44%	5.42%	8.52%	10.31%

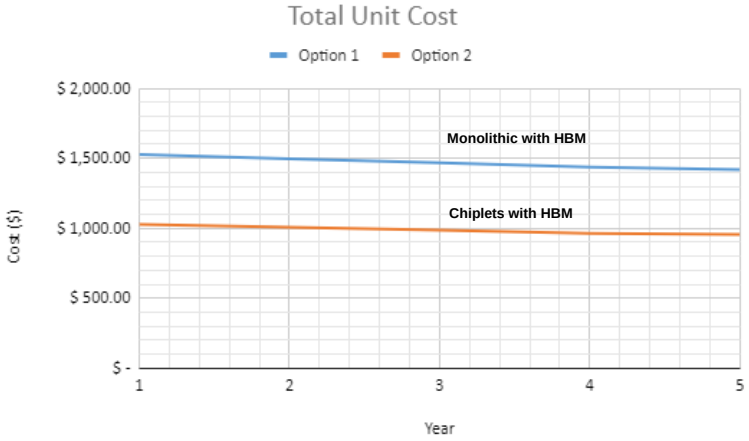
Cost Difference	**-$433.12**	**-$423.22**	**-$413.21**	**-$403.60**	**-$392.71**

Scenario 3: HBM with 1 or 2 Dies?

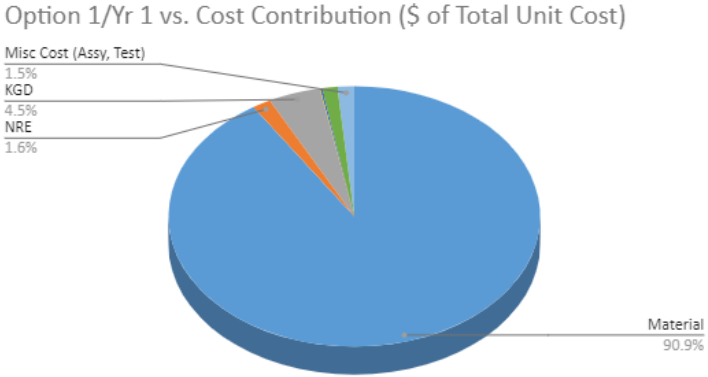


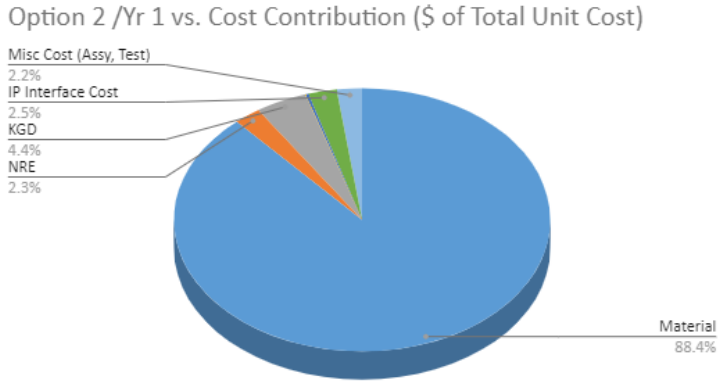
- Cost wise, should we split a monolithic die into two smaller ones?
- Several input parameters assumed in model

Scenario 3: HBM with 1 or 2 Dies?



- Chiplets-with-HBM is about **30% less expensive** than monolithic-with-HBM
- Cost Drivers:
  - Material > KGD > IP Interface > NRE > Misc. Cost
- Main die split in this case makes economic sense.





Future Work

- Phase 1:
  - Simplified “toy” model will be added for beginners
  - More use cases and model vetting
  - Addition of more variables
  - Some default values per inputs from contributors
- Phase 2:
  - Python script-based model to capture more factors
  - Sensitivity analysis of critical factors: yield, pricing, volumes, etc.
  - Script could be incorporated into EDA tools for iterative design tradeoff analysis

Call to Action

- Model will be released periodically and latest version will be listed on the ODSA website

- Reach out to us:
  - If you are interested in developing the cost model
  - If you have an existing set of parameters that could be included
  - If you can help us share and evangelize the concept of an open cost model

Thank you!

NOVEMBER 9-10, 2021