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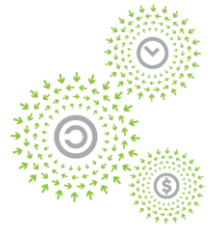
Distributed Disaggregated Chassis Evolution (V2):
Implementation and Update



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DDC-Distributed Disaggregated Chassis Evolution (V2): Implementation and Update

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DDC-(version1): Implementation Review

DDC-v1	DDC-v2	Function	Description	ODM SKU/Model	DriveNets NOS	Cisco NOS
DCP100 ==>	DCP1	Line Card	40x100G + 13x400G Fabric	UfiSpace-S9700-53DX DNI-AGCXD40V1	UfiSpace & DNI	UfiSpace
DCP400 ==>	DCP2	Line Card	10x400G + 13x400G Fabric	UfiSpace- S9700-23D	UfiSpace	UfiSpace
DCF48 ==>	DCF1	Fabric	48x400G Fabric	UfiSpace-S9700-48D DNI-AGCC048	UfiSpace & DNI	UfiSpace
DCF24 ==>	DCF2	Fabric	24x400G Fabric	Accton- ??		
DCM ==>	DCM1	Management	48x(1/10G) + 6x100G	Accton AS-5916-54XL	Accton	Accton
DCC ==>	DCC1	Control	Skylake or Later COTS	COTS Server	HP or Dell Servers	HP DL380P Gen 10
	DCP3	Line Card	New Spec in DDC-v2	TBD	TBD	TBD
	DCP4	Line Card	New Spec in DDC-v2	TBD	TBD	TBD
	DCCM1	Ctrl+Mgmt	New Spec in DDC-v2	TBD	TBD	TBD

Configuration	Scale	Sample Deployment	Elements
Stand Alone	4-Tbps	Stand Alone	{1-DCPx}
Small-1	16-Tbps	1 Cabinet	{1-DCF48, 2-4 DCPx, 2-DCM, 2-DCC}
Small-2	32-Tbps	1 and 1/2 Cabinets	{2-DCF48, 2-8 DCPx, 2-DCM, 2-DCC}
Medium-1	96-Tbps	5 Cabinets	{7-DCF48, 2-24 DCPx, 2-DCM, 2-DCC}
Large-1	192-Tbps	9 Cabinets	{13-DCF48, 2-48 DCPx, 4-DCM, 2-DCC}

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DDC-V1-Cluster-I
mplementation

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DDC-(version2): Follow-on

1. DDC Version 2 Spec – Spec two new WB elements {DCP3, DCP4} to take advantage of Broadcom’s DNX family newest technology based on J2C+ and J2C.
2. DDC Version 2 Spec – Describes a PTP Timing Synchronization Scheme across a DDC system (which was noted as a missing capability in DDC version 1)
3. DDC Version 2 Spec – Proposes Modularization and Optimization Design Practice by ODM for WB within DDC
4. DDC Version 2 Spec – Proposes an optimization possibility to combine the DCC and DCM (new) → DCCM1 which can be implemented with DCP4 with Large CPU/SSD/Memory option.
5. Nomenclature Change – To keep generic naming convention and to accommodate future developments and technologies.

DDC-V1 ==>	DDC-V2 Naming
DCP100	DCP1
DCP400	DCP2
DCF48	DCF1
DCF24	DCF2
DCM	DCM1
DCC	DCC1
(new) ==>	DCCM1 = Combo(DCC+DCM)

DDC-V2 New Specs
DCP3
DCP4
DCCM1
Timing/Synchronization in DDC System

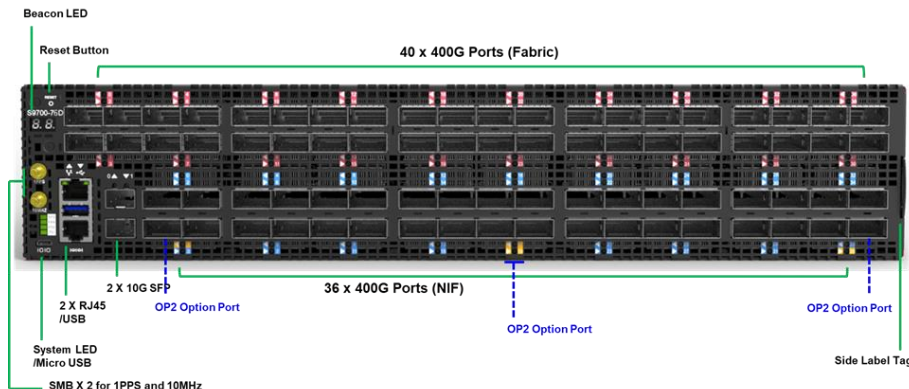
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DDC-v2: DCP3-Key Requirements

Feature	Description
Network	32/36x400G QSFPDD (dependent on OP2 Option)
Fabric	40x400G QSFPDD
Craft	RJ45 Serial Console Micro USB Serial Console USB3.0 Type-A
NM	1x10/100/1000 RJ45 Mgt 2x10G SFP+ DDC Mgt (PTP-Support)
Timing	SMB-10Mhz In/Out SMB-1PPS In/Out
NPU	BRCM 2xJ2C+ (BCM88850 or BCM88851) (SKU Option)
Route Scale	BRCM OP2 BCM16K x 4 (Factory Option)
CPU	Daughter Board: Skylake-D Generation or Later
BMC	Aspeed AST2400
Synchronization	Stratum 3E OCXO, Synch-E IEE 1588V2, T-BC/OC, T-TC, Class-C
LED	System Status LED Per Port Link + Act LEDs FAN Status LED PSU Status LED 2Digits 7-Seg Beacon LED
AirFlow	Redundant Hot Swap Fan, Port to Power (F2B)
PSU	Redundant Hot Swap AC or DC
MACSEC	For SKU with BCM88850. Linerate MACSEC on all 400G Network Ports. BCM88851 does not support MACSEC.

Sample UfiSpace Design



In Standalone: Needs Loopback Connector on Fabric Ports.

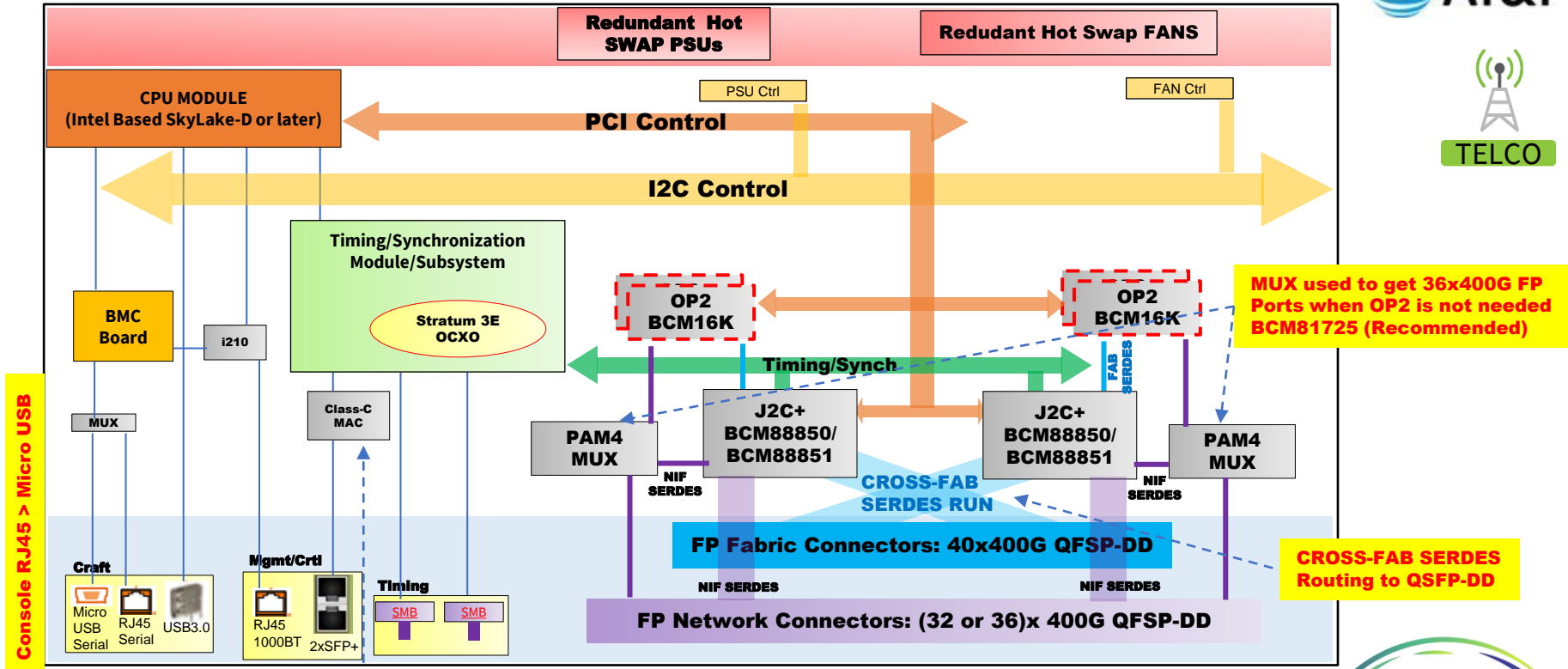
In DDC Cluster: 1 DCP3 replaces 3-DCP2

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DDC-v2: DCP3-High-Level Block Diagram

Back Panel: POWER/FAN SIDE (HOT Outflow)



MUX used to get 36x400G FP Ports when OP2 is not needed BCM81725 (Recommended)

CROSS-FAB SERDES Routing to QSFP-DD

Console RJ45 > Micro USB

CLASS-C MAC To Enable PTP
Transit from DCP => DCM => DCP

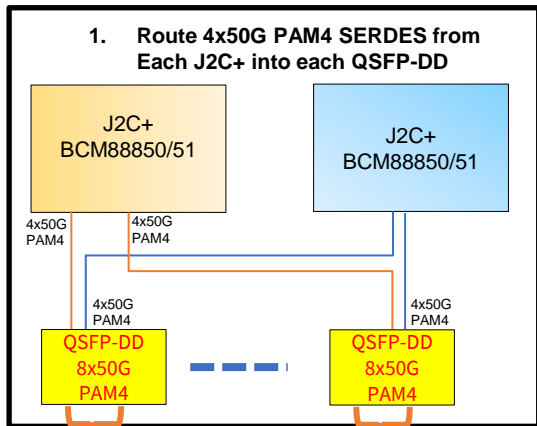
Front Panel: PORT SIDE (COLD Intake)

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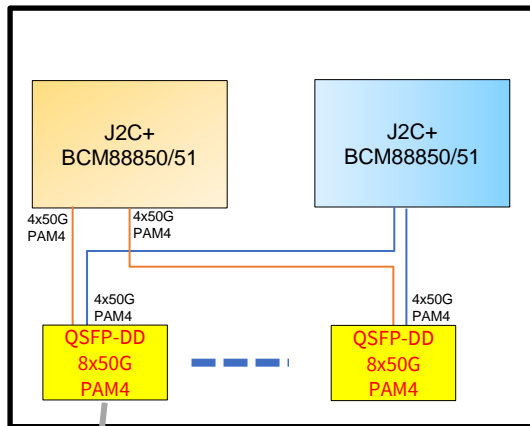


DDC-v2: DCP3-Special Serdes Routing to QSFP-DD

DCP3-Standalone Req

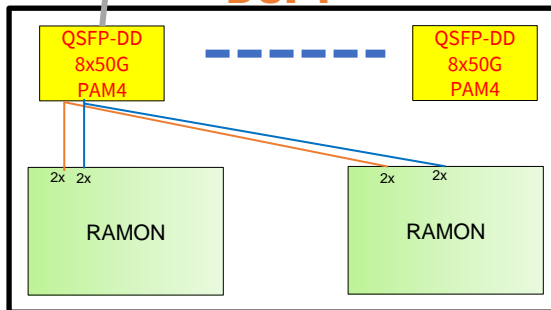


DCP3 Fabric/Cluster Operation Req



2. Route 4x50G PAM4 SERDES from Each J2C+ into each QSFP-DD in the sequence/order so that when connected to DCF1, the SERDES are spread over the two RAMONs in DCF1

DCF1



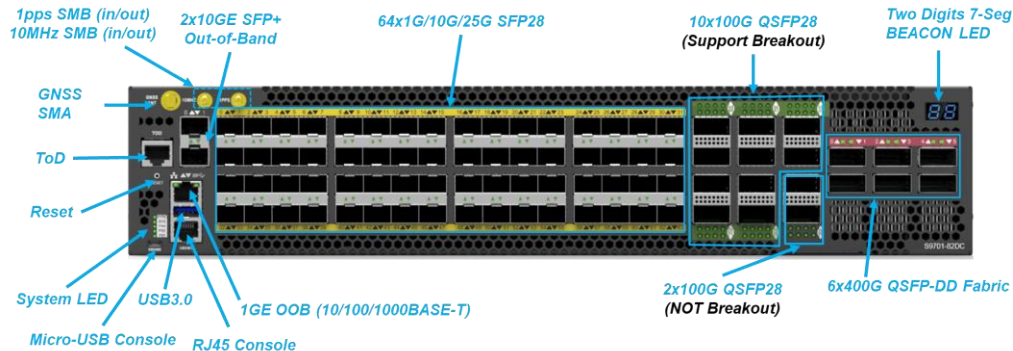
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DDC-v2: DCP4-Key Requirements

Feature	Description
Network	64x(1G/10G/25G) SFP+ 10x100G QSFP [Breakout:4x(10G/25G)QSFP] 12x100G QSFP [Not Breakout]
Fabric	6x400G QSFPDD
Craft	RJ45 Serial Console Micro USB Serial Console USB3.0 Type-A
NM	1x10/100/1000 RJ45 Mgt 2x10G SFP+ DDC Mgt (PTP-Support)
Timing	SMB-10Mhz In/Out (In or Out - Configurable) SMB-1PPS In/Out (In or Out - Configurable) SMA-GNSS Input RJ45-(TOD & 1PPS) (In & Out)
NPU	BRCM J2C BCM88802
Route Scale	BRCM OP2 BCM16K (Factory Option)
CPU	Daughter Board: Skylake-D generation or Later
BMC	Aspeed AST2400
Synchronization	Stratum 3E OCXO, Synch-E, Class-C IEE 1588V2, T-BC/OC, T-TC, T-GM
LED	System Status LED Per Port Link + Act LEDs FAN Status LED PSU Status LED 2Digits 7-Seg Beacon LED
AirFlow	Redundant Hot Swap Fan, Port to Power (F2B)
PSU	Redundant Hot Swap AC or DC

Sample UfiSpace Design (in progress)

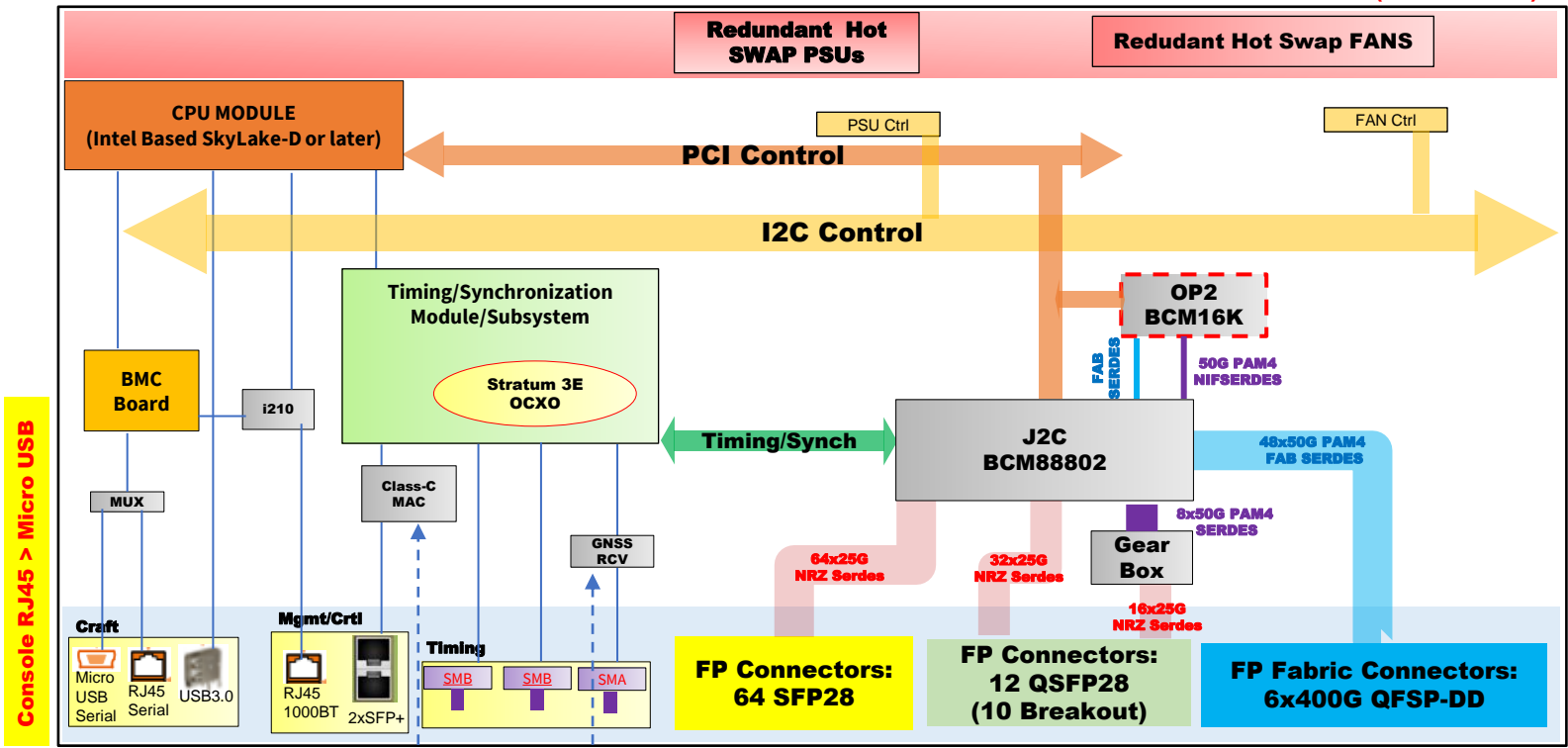


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DDC-v2: DCP4-High-Level Block Diagram

Back Panel: POWER/FAN SIDE (HOT Outflow)



CLASS-C MAC To Enable PTP
Transit from DCP => DCM => DCP

GNSS to support TC-GM

8 QSFP28: If breakout, no loss

4 QSFP28: If breakout, Loose 2 ports

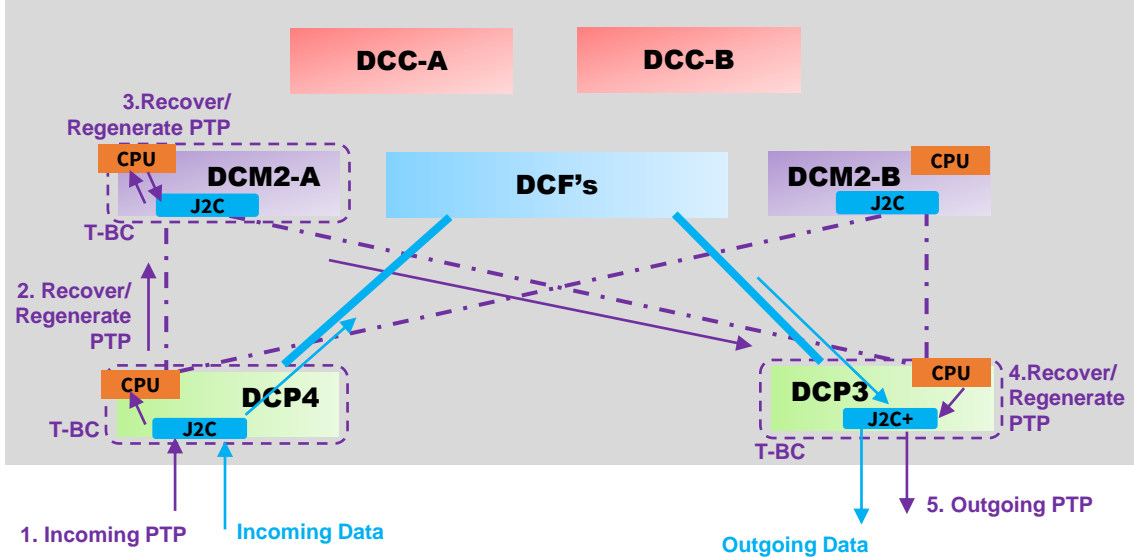
Front Panel: PORT SIDE (COLD Intake)

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DDC-v2: PTP Synchronization across DCPs within DDC system

- PTP Synchronization capability is only available on new DCPs hardware that meet the DDC-v2 timing specification of Class-C or better which has the Network Timing Subsystem and the BCM82752 (or equivalent) used for the 2x10G SFP+ ports on each DCP.
- To achieve this, need to Replace DCM1 (AS5916-54XL) with DCM2 (→DCP4) WB To function as DCM.
- Target objective for DDC system is Class-B or better.



Existing DCP1 and DCP2 does not have the hardware to support timing specification of DDC-V2. If a J2 white box is needed with SynchE/PTP timing support, then the specification of this design can be added to the DDC-v2 Specification as a subsequent release for contribution to OCP.

This slides shows how the enhanced HW can support PTP features. Much more in-dept of scenarios discussion needed to define the software requirements to support PTP in a realistic application of the DDC.

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DDC-v2: Modularization & Factory Options

- The High-Level Block Diagram for the DCP3 and DCP4 shows the CPU and Network Timing/Synchronization sub blocks. This was intentional.
- The Network Timing/Synchronization subsystem design should be reusable across DCP3 and DCP4 and future DCP specification.
- The overall WB system (power and cooling) and CPU sub-block should be design to accommodate a range of CPU/SSD/Memory Options.
- The intention is to be able to reuse the CPU module in future DCP specifications as well.
 - CPU: SkyLake-D 4-cores up to 16-cores (Present) / IceLake-D 20-Cores (near future)
 - Memory: 2x16G up to 4x64G (ECC)
 - SSD: RAID0 support up to 2x512G
- The design specification is for the worst use case to be able to pass the most stringent environmental requirements (e.g. AT&T TP76200, NEBS3). Certain factory options (like OP2 or BCM88850 vs BCM88851) will possibly result in different SKUs. However, this allows for a specification of a single design that can accommodate different options to meet the business requirements of different operators or use cases.

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DDC-v2: Optimization/Efficiency

- **One DCP3 = 3*DCP2** in terms of Network ports and Fabric Ports in (2RU, 3000W) versus (6RU, 6000W).
- DCP3 (with OP2) offers same route scale as DCP2 but supports 4X- VOQ over DCP2.
- **2*DCP4 (4RU, 2600W) = 1*DCP1 (2RU, 2000W)** for Equivalent Network and Fabric switching BW.
- DCP4 offers better route scale (~75%) and Queues scale (2x) over DCP1.
- DCP4 offers a more efficient use of resources over DCP1 when more 10G/25G interfaces are needed.
- DCP1 loses 50% of ports when used in breakout mode.

DCCM1 – concept is to combine the function of DCM1(AS-5916-54XL) and DCC1(HP-DL380P Gen10) into one WB. This can be accomplished using the DCP4 with a Maximum CPU module option:

*SkyLake-D 16-Core (present)
or IceLake-D 20-Core(future)
4x64G ECC DRAM
RAID0 2x512G SSD*

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Call to Action

- DDC Specification is part of Telco-Edge Project.
- ODMs: Accton/Edgecore, UfiSpace, Delta Network International
- NOS: DriveNets, Cisco
- DDC-v1 in Operation in AT&T Network carrying production traffic...
- Encourage other Providers and Carriers to investigate/adopt.

Where to buy: [Contact listed ODM or NOS](#)

Project Wiki with latest specification : <https://www.opencompute.org/contributions>
Type AT&T into Search box

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Open Discussion



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