I/O Connectivity Chiplet

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Chiplet Examples for Heterogenous System Design (KGD)

- New Design paradigm , from IP reuse to Chiplet reuse
- Primary drivers for chiplet functionality:

Processor

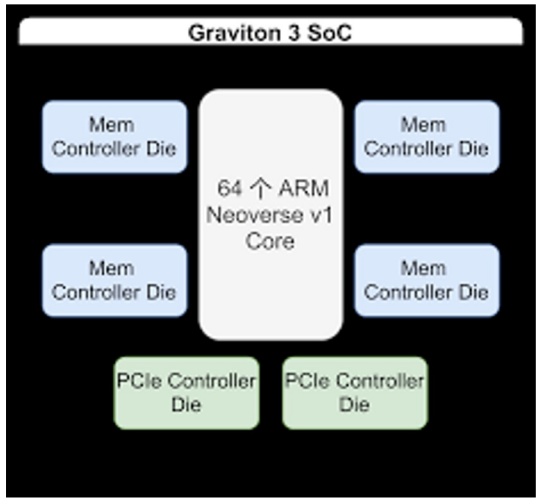
- Multi-Core
- GPGPU
- CPU + Workload accelerator
- Scientific computing

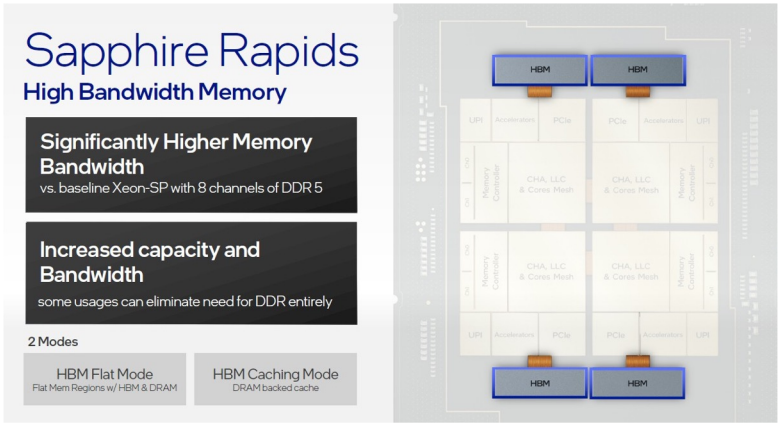
Memory / Storage

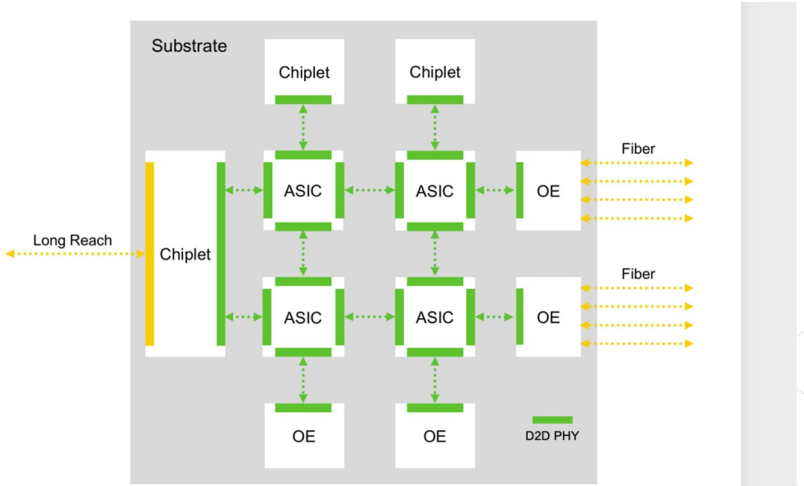
- HBM - Cache Extensions
- PIM (Processing In Memory)
- Packet Buffering / Look Ups
- Data Analytics / Cache Ext

CONNECTIVITY

- Host / Client / IO Peripherals
- NoC (Chip / Interposer)
- Server SoC (CPU+Chipsets)
- WEB servers , Fabric , NIC

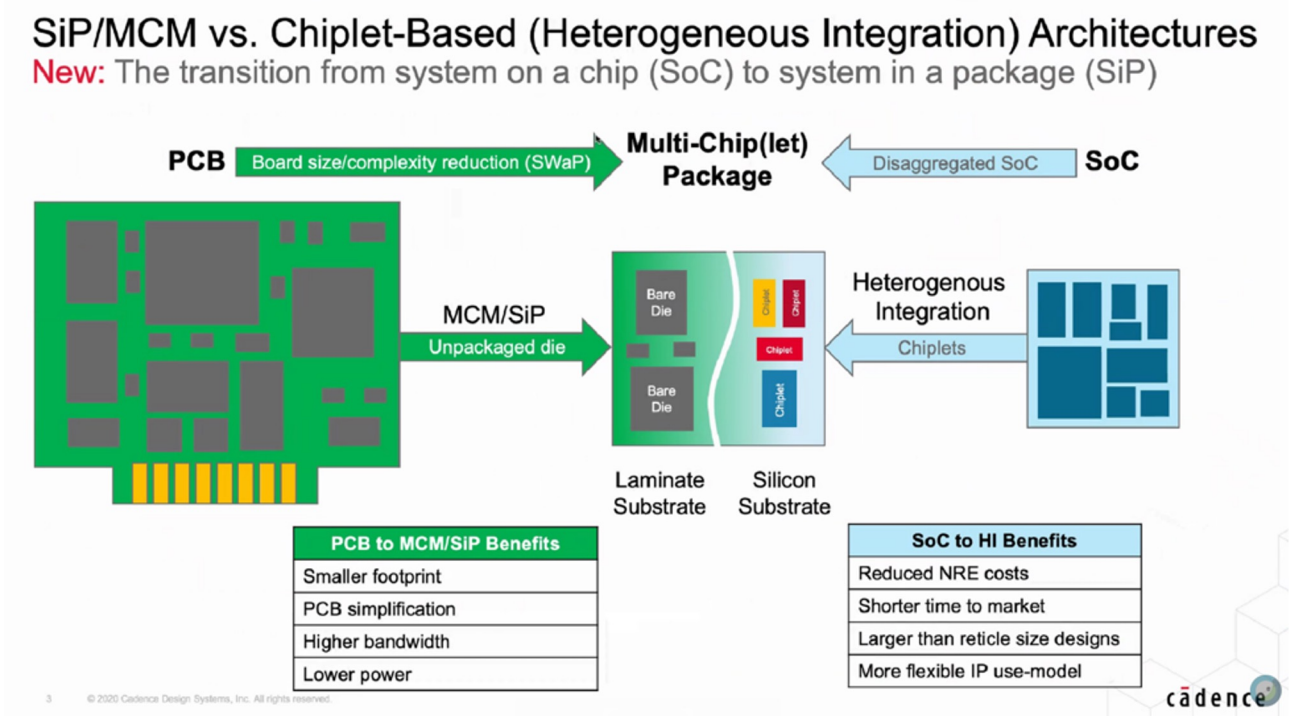




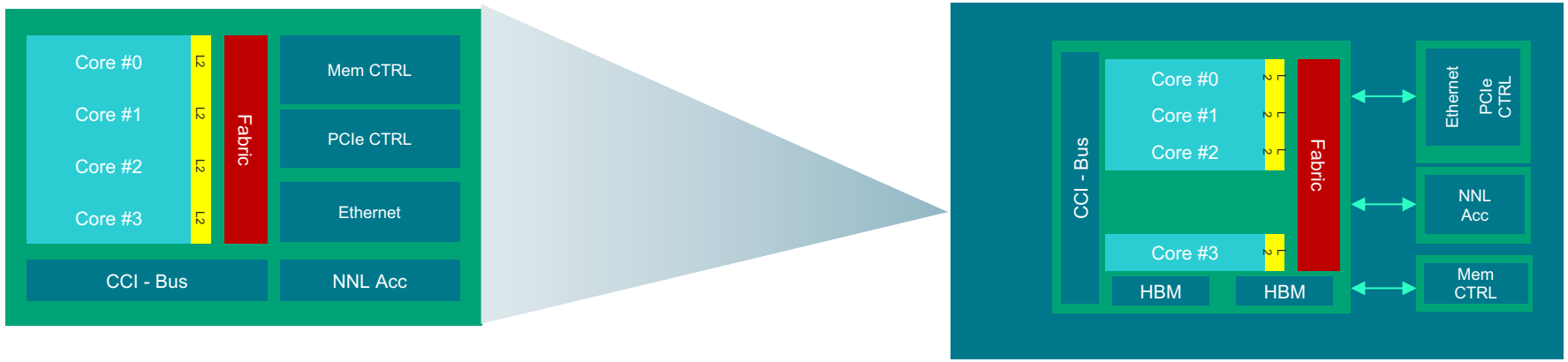


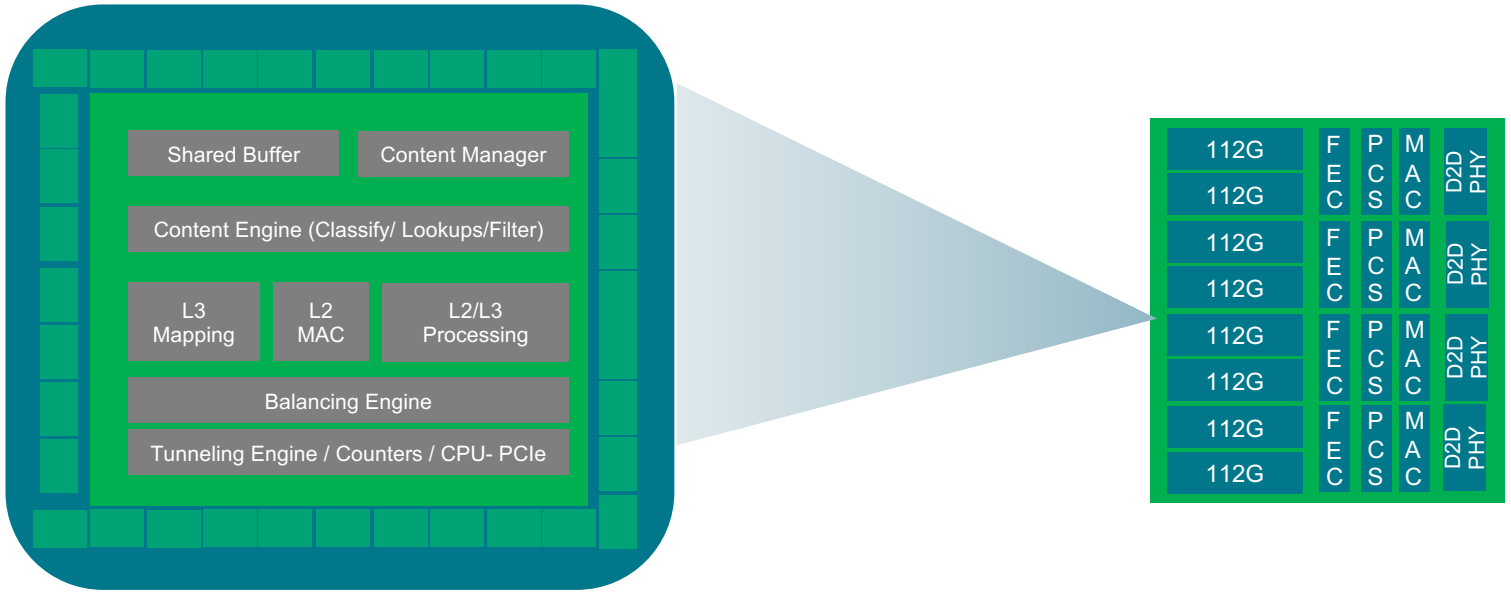
Heterogenous System : Chiplet IO Connectivity

- Design partitioning is primary driven by “functional independence”
  - Functional independence Lego Block Mindset , Repeatable & Scalable Architecture
  - On of the key requirement for “Scalability” is IO Connectivity [Bandwidth]
  - This is legacy classic case of transitions from System Chiplet



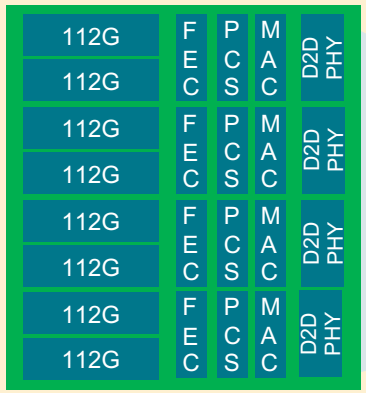
Classic Examples of Chiplet – IO Connectivity Dependency



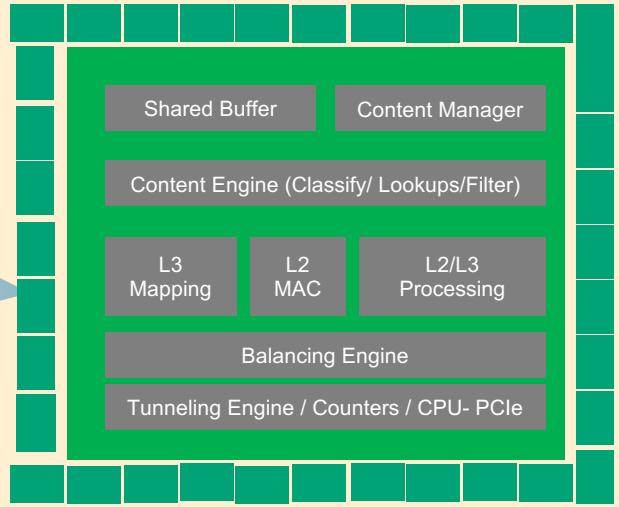


Chiplet Landscape (IO Chiplet - Connectivity)

Connectivity

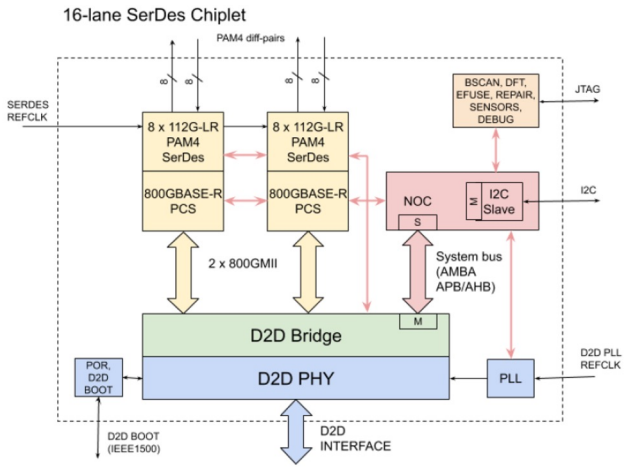


CDNS has all these IP + System know how

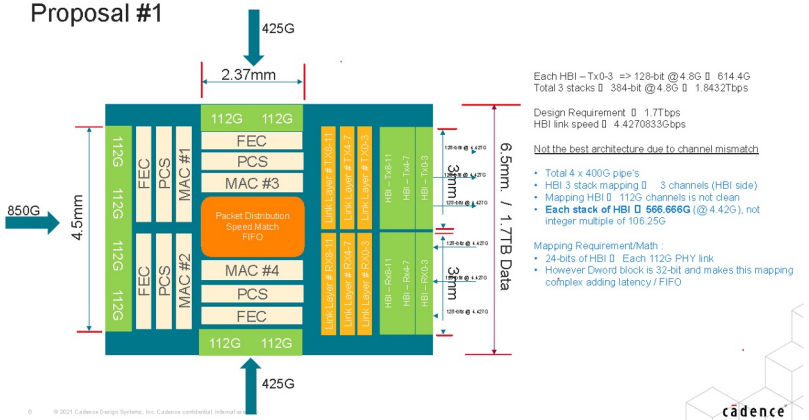


- L0/L1 layer implemented on the chiplet
- Provides optimal fabric design flexibility – scalability , larger buffer for high bandwidth i.e., 25T+ on monolithic die
- Can be potentially extended to enable GB , FEX & Multi-Channel features on the chiplet

Block Diagram



Proposal #1



Each HBI – Tx0-3 => 128-bit @4.8G 614.4G
Total 3 stacks 384-bit @4.8G 1.8432Tbps

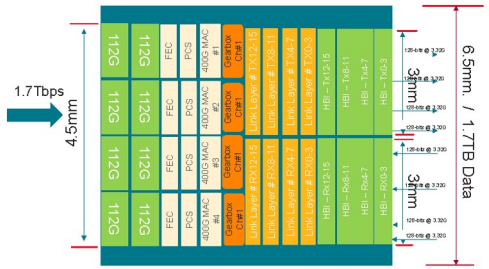
Design Requirement 1.7Tbps
HBI link speed 4.4270833Gbps

Not the best architecture due to channel mismatch

- Total 4 x 400G pipe's
- HBI 3 stack mapping 3 channels (HBI side)
- Mapping HBI 112G channels is not clean
- **Each stack of HBI 566.666G** (@4.42G), not integer multiple of 106.25G

Mapping Requirement/Math :
- 24-bits of HBI Each 112G PHY link
- However Dword block is 32-bit and makes this mapping complex adding latency / FIFO

Proposal #2B



Each HBI – Tx0-3 => 128-bit @4.8G 614.4G
Total 4 stacks 512-bit @4.8G 2.4576Tbps

Design Requirement 1.7Tbps
HBI link speed 3.32031256bps

Not the best architecture due to channel mismatch

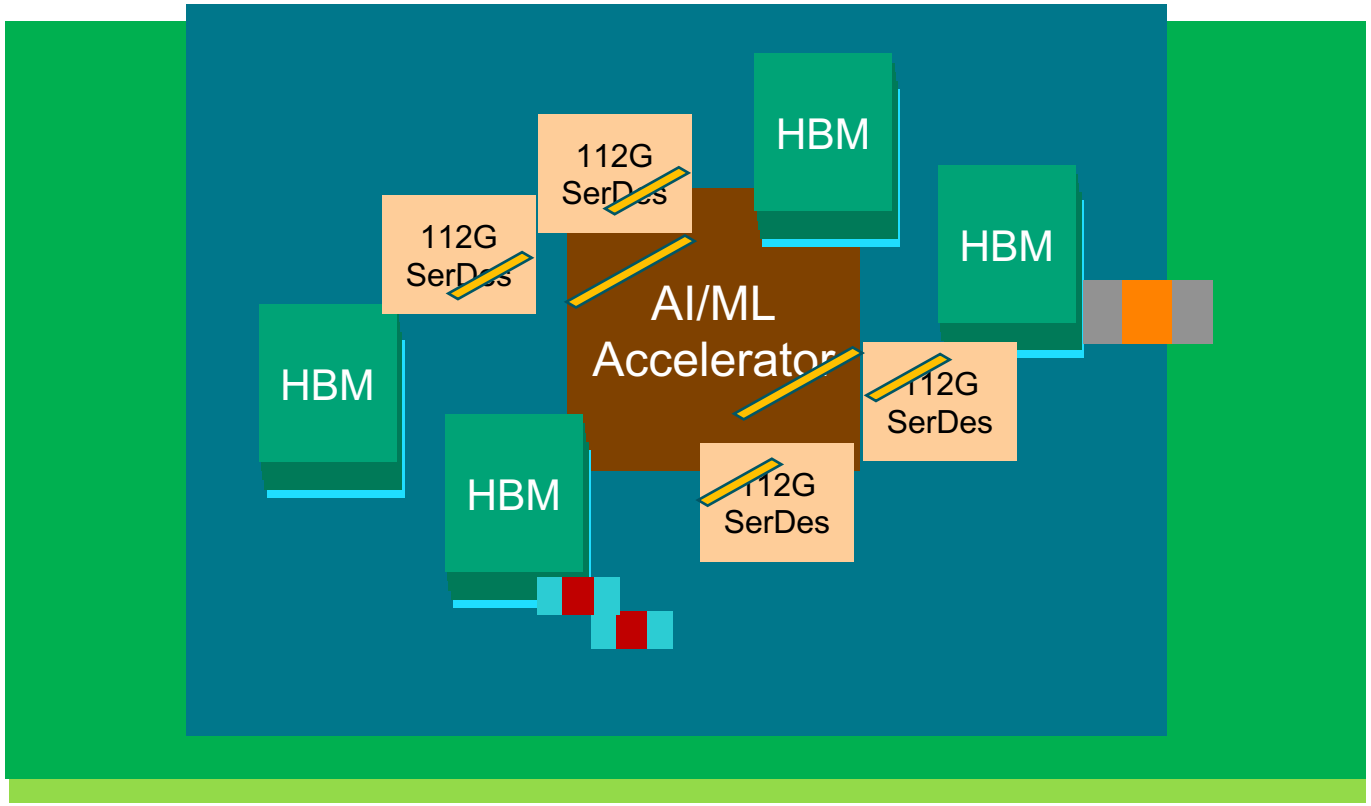
- Total 4 x 400G pipe's
- HBI 4 stack mapping 4 channels (HBI side)
- Mapping HBI 112G channels is clean (1:1)
- Each 128-bit @ 3.3203125G 4 x 106.25G (425G)
- **Each stack of HBI 425G** (@3.32G)

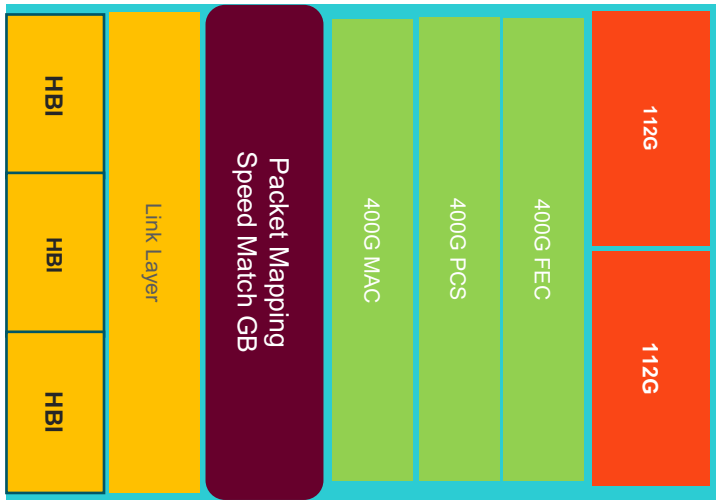
Mapping Requirement/Math :
- 128-bits of HBI Each 112G PHY link

IO Tool Automation for Connectivity – Chiplet

- Primary factor for designing Connectivity IO Chiplet
  - Architectural (MAC / PCS / Gearbox / Glue Logic)
  - Physical/Electrical Constraints – bandwidth , beach front , BER , latency , power , package
- Automation primary focus on the ”Architectural” element considering the physical constraints as fixed constants (data-path connectivity only)
- Automation is agnostic towards any PHY being considered
  - BoW , OHBI , Ultra-Link , UCIe
  - Only parameter necessary is the data-path (if provided would be beneficiary)
- Automation targets :
  - Design Optimization (PPA)
  - TTM (Scalability)

IO Connectivity Deep Dive – Chiplet

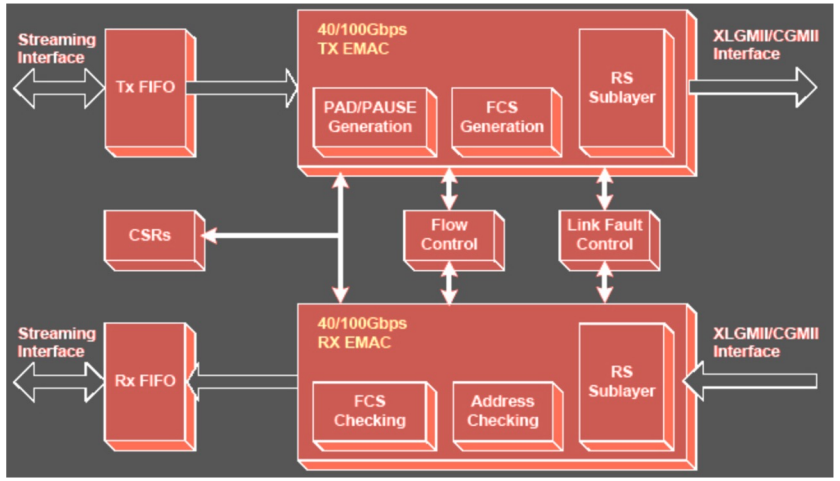


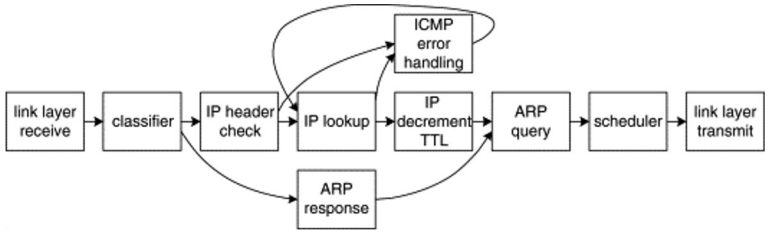


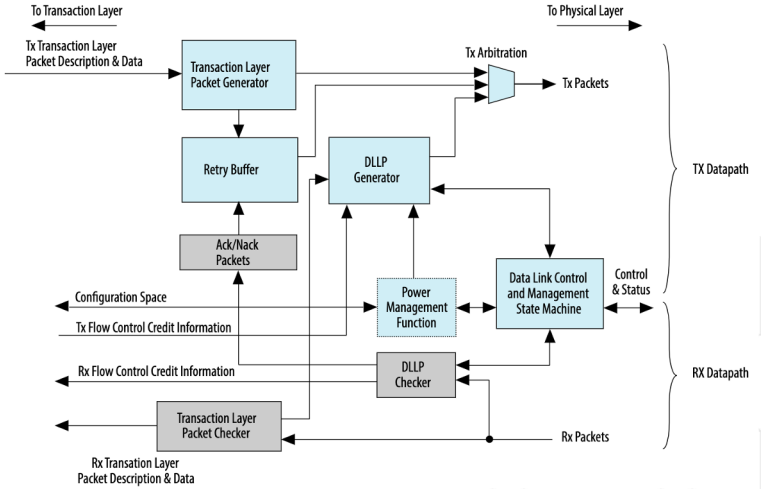
Focus is to optimize the L0/L1 connectivity on the chiplet – Scalable to be re-usable across different market segments / products

Automation Engine – Parameter for IO Chiplet (Connectivity)

- MAC Engine
  - 1G/10G/25G/56G/112G/200G/400G/800G
  - Channelized / Non-Channelized
  - IFG
  - Tunneling Protocol (RIoT / VXLAN / NVGRE..)
  - SyncE (Timing)
  - DMA
  - Flow Control
  - Filtering
  - Padding /Frame Length
  - CRC Checks
  - Clocking
  - Management (Statistics / Traffic Monitoring)
- Packet Processing / Mapping
  - Architectural Design
  - Based on customer/application requirement
  - Flow Injection / Header Checker
  - Classifier / Scheduler
  - Network Rules
  - Application Rules
- Link Layer
  - Link Training (LTSSM)
  - Data integrity mechanism
  - Retry Buffer
  - Packet Generator / Checker
  - Power Management
  - Arbitration

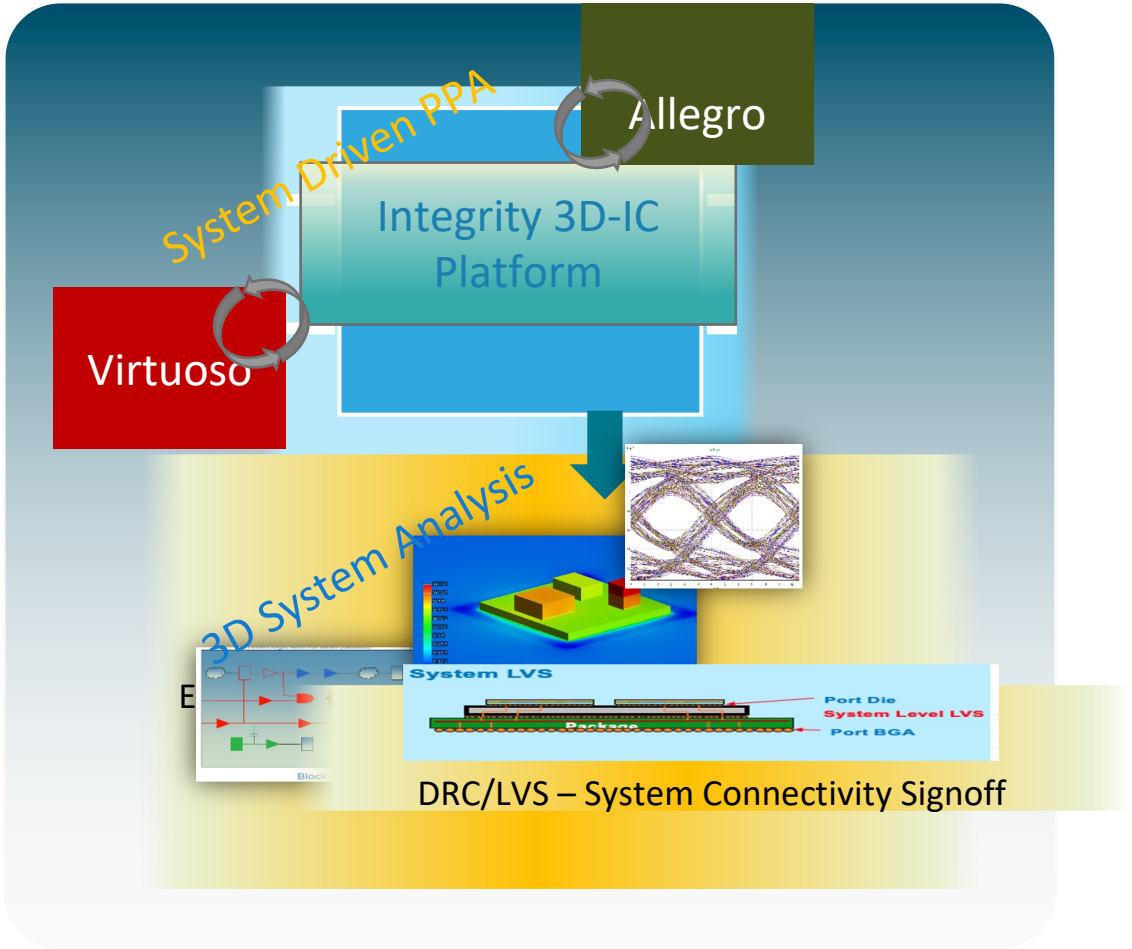






Cadence – Accelerating Chiplet Design

- Design Automation – PAA (IP & Architecture)
- 3D-IC : Design Planning , Implementation & Sign-off



Integrated 3D Design Planning and Implementation

Comprehensive system enabling “System Driven PPA”

Early 3D Thermal, Power & STA analysis

Scaling Horizontally & Vertically