Community Led Hyperscale Open Innovation

OCP – ODSA Project

Commercialization Use Case

eTopus Inc.

ODSA BOW project for Chiplets

Kash Johal, VP Sales

etopus
we accelerate

Why ODSA at eTopus

- 1. eTopus was requested to develop a BOW solution by existing SERDES client
  - eTopus is a leader in SERDES IP – 1-112G @ 16nm, 7/6nm fully validated
  - Millions of units shipped into Tier 1 accounts

  - a. We developed the solution based on customer demand &
    applicability of BOW PHY to chiplets which is an emerging target market
  - First customer can not share specific details as we are under NDA
  - Second engagement with FPGA company – Quicklogic to use BOW PHY
  - b. eTopus involvement with ODSA?
    - Since 2021
    - More Active in 2022 meetings and calls
    - Standardization & ODSA is key enabler for chiplets beyond closed internal teams

ODSA Use Case at eTopus

- Product intersection with ODSA BOW & Chiplet spec
- 1. ODSA BOW d2D PHY is our focus
- 2. 22nm GF will be complete Mid 2022, 4G/8G 0.6-0.75 pj/bit
  - 7/6nm TSMC will be done end 2022 4G-16G < 0.5pj/bit target
  - 2023 Interested in supporting next gen BOW – merge with UCIe Physical specs
- 3. First customer engagement in progress
  - Can not release details due to NDA
- 4. Second customer engagement in progress
  - Quicklogic - FPGA chiplet - will discuss specifics in their presentation
- 5. Specifics on deployment timeline
  - First customer will receive delivery in 2022

BOW what is great & what is problematic

- Great
  - Flexible architecture – can bypass link layer
  - Non terminated – for lowest power & Terminated – higher speeds
  - Flexible bump pitch we are using 130 u & 45
  - Works great for straight simple routes – streaming interfaces
  - Excellent work on interoperability being done

- Not so Great
  - 16 bits data is limiting for common interfaces
  - Low latency FEC not defined for high speed connections
  - Connecting chiplets with multiple layers, angles is problematic
  - it's not like connecting 8-10 chips on a PCB

What is Next for ODSA at eTopus

- Supporting multiple processes with BOW PHY support
- 22nm -> 7/6nm -> 5/4nm……
- Supporting I/O chiplets to simply attach directly to SOC / FPGA

- Our focus is leveraging common interfaces across BOW/UCIe
- Leveraging I/O chiplets for standard interfaces:

  - 800G ethernet across 64 lanes @16G/link
  - 1.6T ethernet across 64 lanes at @32G/link
  - PCIe Gen 6/CXL3 across 32/64 lanes (various link speeds)
  - JESDD upcoming PAM4 across @8/16G/link
  - USB 4v2 (PAM3) upcoming USB 4 across @ 8/16G links

OPEN
Compute Project®

etopus
we accelerate

Questions