

BoW Progress Report

- Completed and moved BoW Specification rev 0.7 to Github:
 - https://github.com/opencomputeproject/ODSA-BoW
- The review committee planned weekly meetings and participants inputs on Spec 0.7 boiled down to ~20 distinct issues

 Major Step: Successfully finalized and reached a consensus on the BoW Interface Objectives

BoW High-Level Objectives (Based on industry surveys)

- A set of backward compatible die-to-die parallel interfaces that provides the flexibility to trade off the following key factors:
 - → Throughput per die edge
 - → Design Complexity
 - → Packaging Technology Cost

<u>Backward Compatibility Definition</u>: Each future version of this interface is expected to be compatible with at least two previous significant versions.

BoW Interface Objectives

- High Energy Efficiency Target <1 pJ/bit
- Beachfront Bandwidth (aggregate Transmit + Receive):
 - >100Gbps/mm with all packaging options
 - >1Tbps/mm with preferred packaging option
- Trace length ranges on laminate substrate:
 - Unterminated reach <10mm
 - Terminated reach <50mm
- Latency & BER Target Requirements:
 - Low-latency mode (w/o FEC): Latency <5ns & BER < 1E-15
 - Latency <5ns required for high-performance compute applications
 - Ultra-low BER mode (w/ FEC): Latency <15ns & BER < 1E-25

<u>Latency Definition</u>: Delay from the source PCS parallel interface to destination PCS parallel interface

BoW Interface Objectives (Cont.)

- Portable across wide process nodes ranging from 28nm to 5nm
 - A necessity for heterogenous integration with wide range of chiplets
- Single supply core supporting Vdds compatible with CMOS process nodes from 28nm to 5nm
- Support Conventional & Advanced Packaging Technologies
 - Low-Cost Organic Substrates (bump pitch 100u-130um)
 - Advanced 2.5D Interposer (bump pitch 30u-55um)
- Be unencumbered by Patent Licensing Fees/Royalties

BoW Next Step

- The next goal is to release BoW Spec 0.9 by March 2020
- In preparation to release rev 0.9, the committee is planning to close the following key 6 issues:
 - Reference Bump Maps
 - Clocking Requirements
 - Test and Testability
 - Calibration Mode
 - Initialization
 - Interoperability

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