BoW: Basic, Fast, Turbo
Die-to-Die Open Interface Solutions

ODSA Project Workshop

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Consume. Collaborate. Contribute.

Interface standardization

- Chiplet based systems will likely have a variety of different interfaces moving forward

  - Fast Serial interfaces with some compatibility to existing standards (eg 112GXSR)

  - Novel USR interfaces driven by an ecosystem (eg. Kandou/Marvell)

  - Simple interfaces for moving reasonable bandwidth between die from less cutting edge nodes

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Does it make sense?

- Does it make sense to have another parallel standard?
  - AIB is a good starting point, currently has datarate and footprint definitions that limit use on a laminate
  - Making the spec as open as possible can hopefully speed up useability

- How do we decide if this effort is providing a value to the community?
  - Inertia from participants, adoption in products
    - Standardization coalesces
    - Adoption in custom/'contained' interfaces
    - Moving to interoperable interfaces between various die

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The basic idea

- Blast from the past – use simple CMOS IO to communicate

- We stopped using these when SERDES simplified board routing (less traces=less $$)

- Keeping everything on a laminate keeps things simple
  - More routing traces than a board
  - Less ESD requirements

- Make an interface that works on a cheap laminate or a fancy silicon based interconnect
  - Enable compatibility where we can
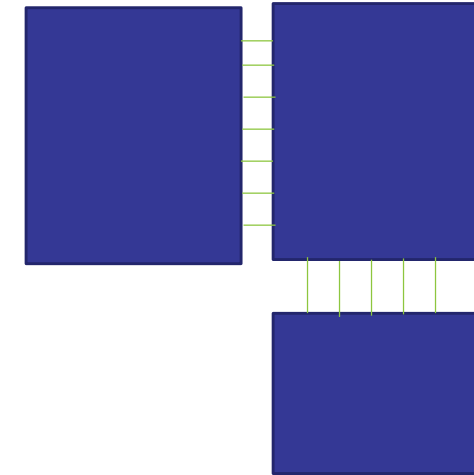
BoW Intro:

- High level proposed solution:

  - Simple source synchronous DDR interface
    - Clock adjust needed for DDR

  - Non Terminated (Termination may be ok, just adds power at lower rates)

  - 1-4 Gbps (or more?)

  - Low overhead IO cell (limited ESD)

BoW Extensions:

- Data Integrity / Power functions – need to discuss
  - ECC – How critical is BER? How much does interface spend vs.
  - DBI – is power worth the pins?

- Extension Mode 2: Bow-Fast
  - Higher speed uses optional termination (~2-3x rate), minor impact on power

- Extension Mode 3: Bow-Turbo
  - Add potential bidirectional feature – implemented in the IO cell
    - Hybrid circuit – can be implemented in multiple ways (examples from BaseT)

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Proposal for dart throwing

Function	Pins	Notes
RX Data	32	
Data Clock	2	Differential
Parity	1	

Function	Pins	Notes
TX Data	32	
Data Clock	2	Differential
Parity	1	

Minimum streaming IF

Other Function	Notes
Data Bus Inversion	~19% power savings
Parity	Not needed if ECC
FIFO Reset	Helpful for control/init
ECC	Error detect/correct
Sideband	Various calibration/etc

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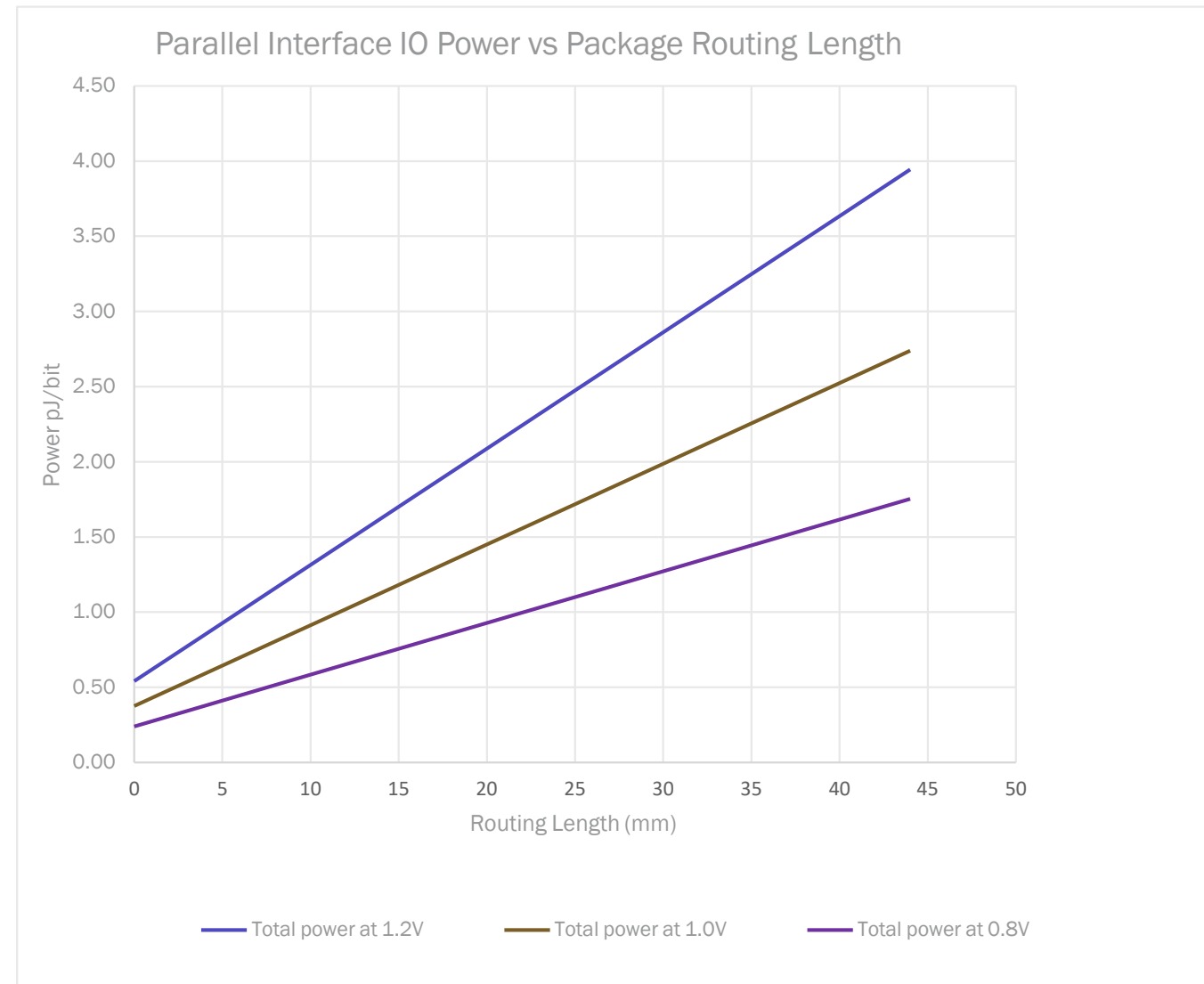
Datarate discussion

- Current proposal: Per databit wire configurable from 1-4Gbps

- What datarates make the most sense for the standard?
  - 1-2Gbps (AHB) limits usefulness on laminate (too many wires to move reasonable bandwidth
  - Configurable datarate including 1-2 Gbps could enable AHB compatibility
  - >5Gbps may require termination

- Having a settable datarate with simple divides maximizes compatibility
  - For 4, 2, 1 Gbps -> simple dividers

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Voltage discussion

- Simple, single voltage based approach – challenge is what voltage to choose?

- 1.2 is HBM legacy, costs power

- 0.9V is often available, decent power, interoperable with AIB*

- 0.75 / 0.8 often available as well, popular chiplevel VDD values

- Lower voltages will have lower power, too low will be a challenge for IO design
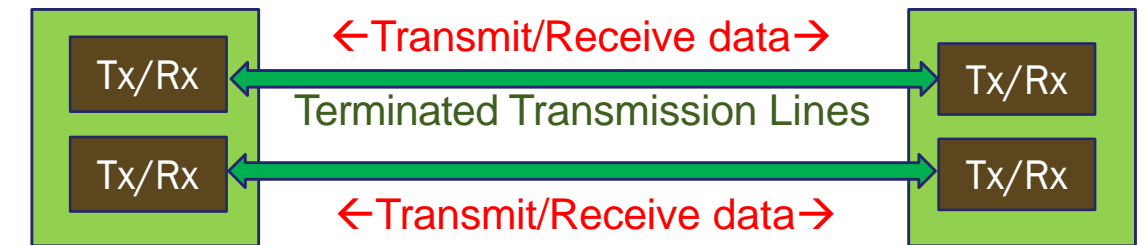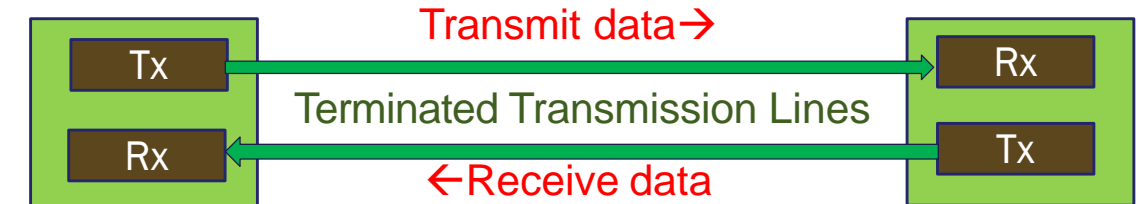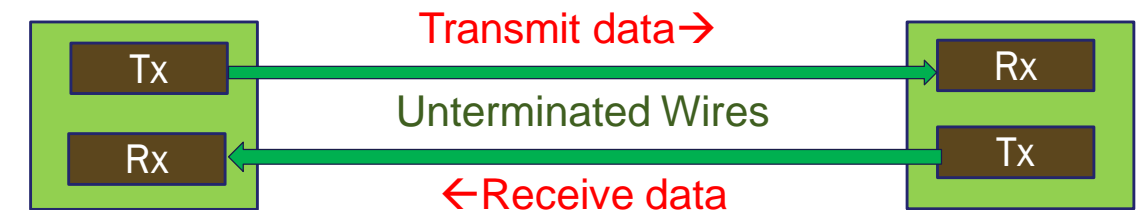
Power (energy)

- Simple energy calculation
  - Pathological worst case w/DBI
    - 0.4
  - No on chip routing from IO to bump assumed
    - Add 0.1 – 0.25 pJ depending on length
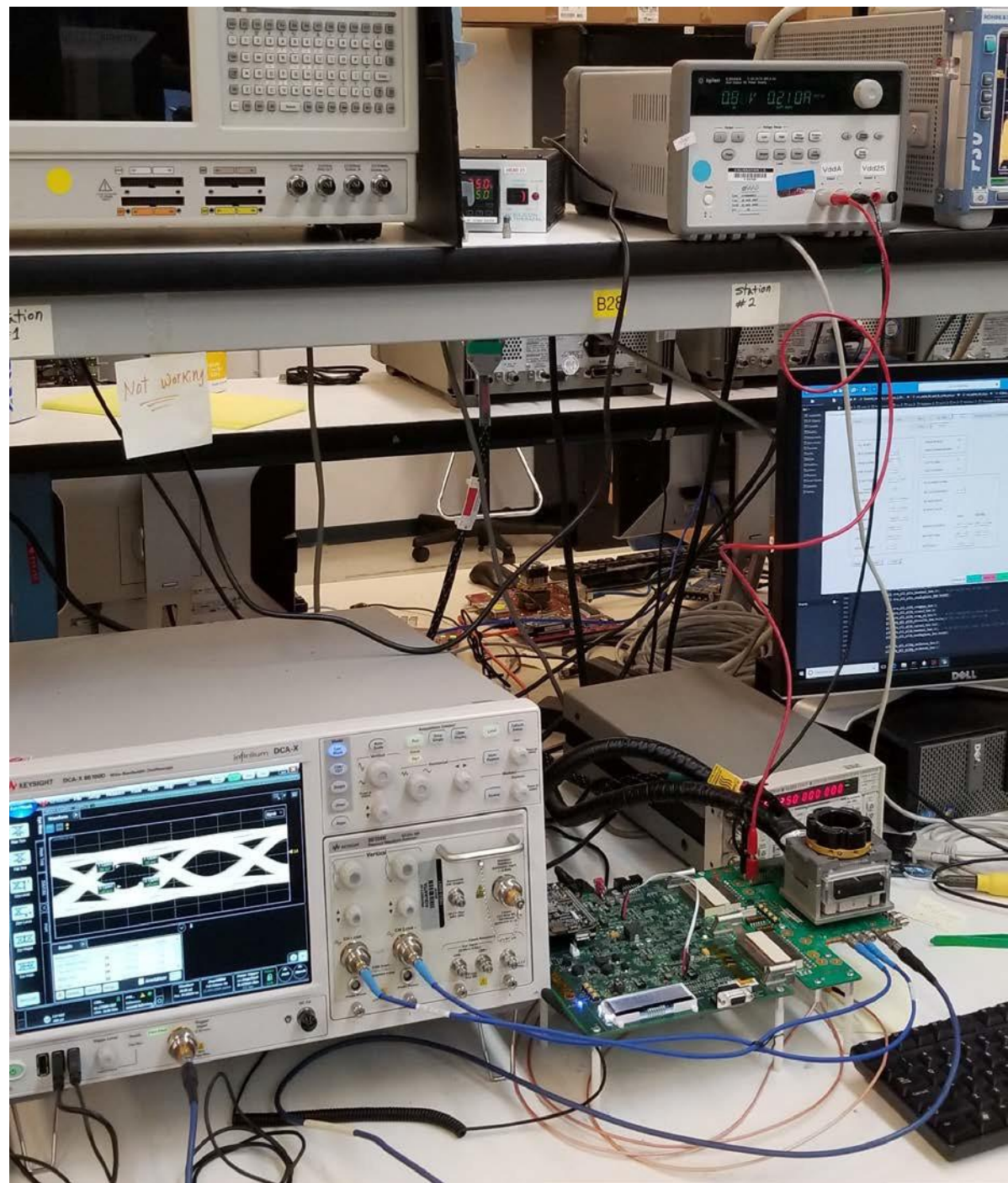 - Termination +~0.2 pJ low speed, less at high speed

Parallel Interface IO Power vs Package Routing Length

Legend: Total power at 1.2V — Total power at 1.0V — Total power at 0.8V

X-axis: Routing Length (mm), Y-axis: Power pJ/bit

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Operation Modes BoW on Organic Package Substrate

- BOW Basic
  - Unterminated lanes → up to 5 Gbps/wire
  - Source Synchronous with clock alignment

Tx → Rx **Transmit data→**
Unterminated Wires
Rx ← Tx **←Receive data**

- BOW Fast
  - Terminated lanes → up to 12Gbps/wire
  - Source Synchronous with clock alignment

Tx → Rx **Transmit data→**
Terminated Transmission Lines
Rx ← Tx **←Receive data**

- BOW Turbo
  - Simultaneous Bidirectional → both directions
  - Terminated lanes → up to 2x12Gbps/wire
  - Source Synchronous with clock alignment

Tx/Rx ↔ Tx/Rx **←Transmit/Receive data→**
Terminated Transmission Lines
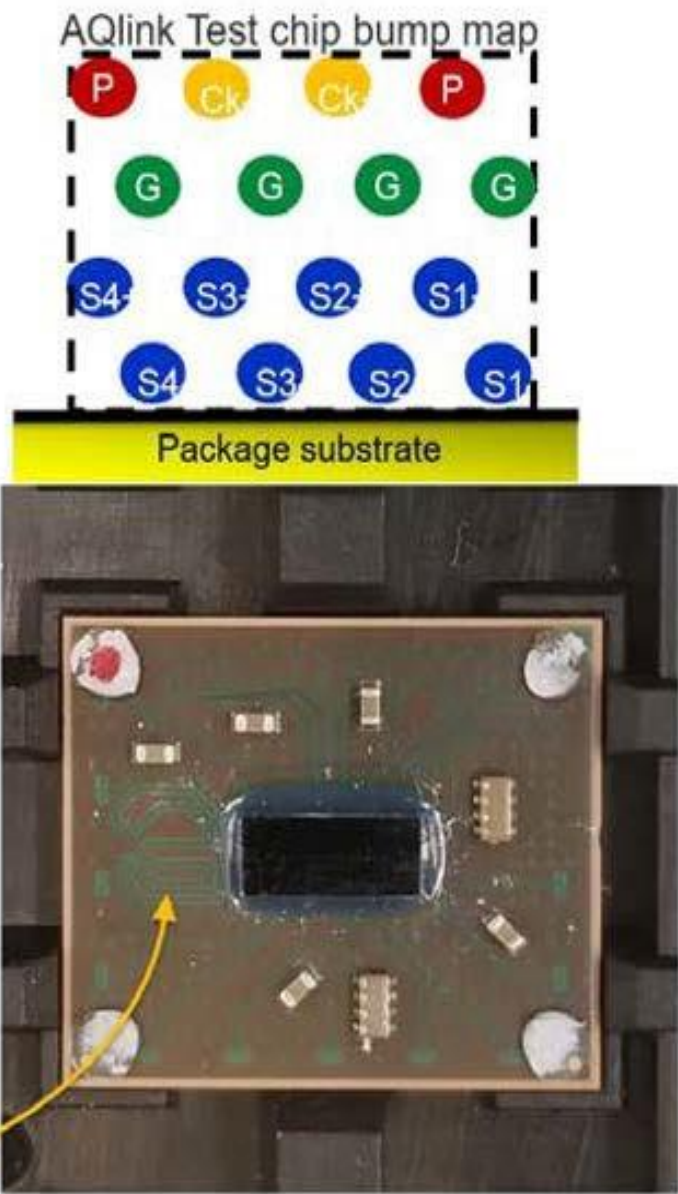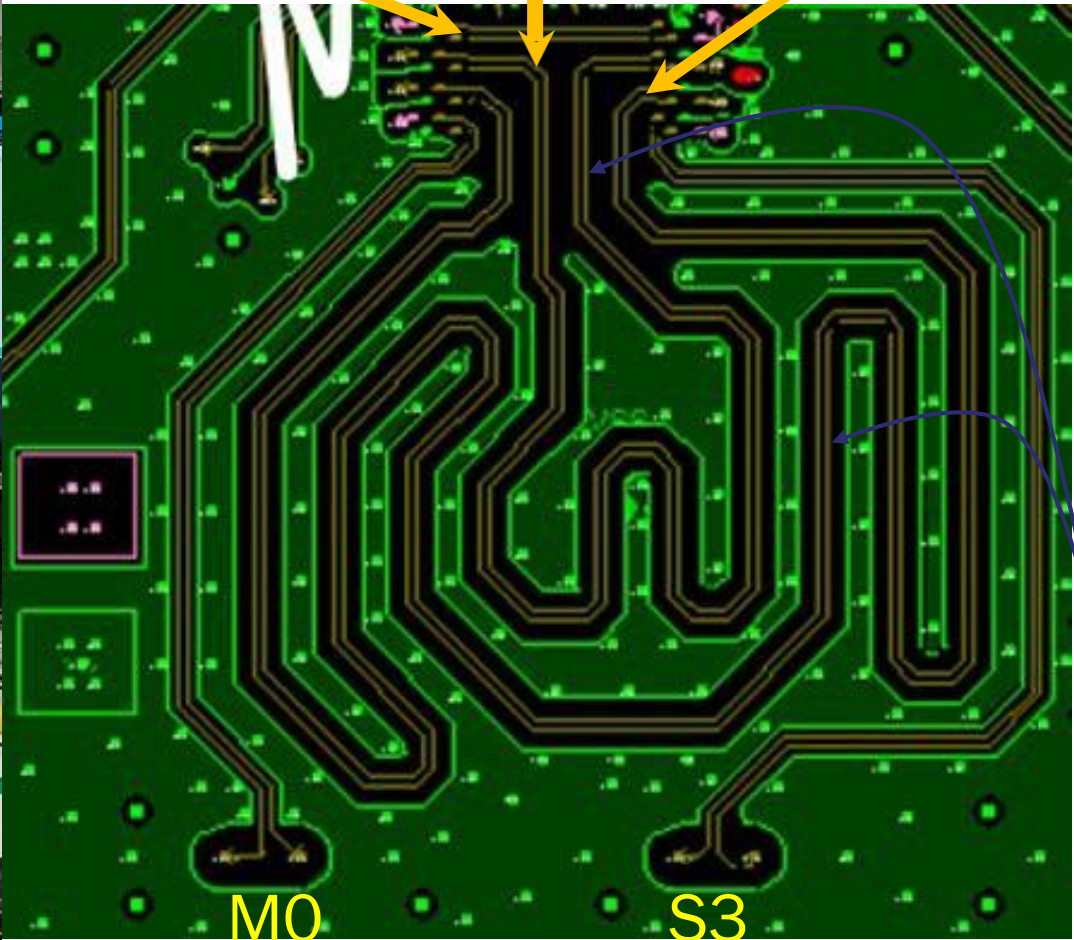Tx/Rx ↔ Tx/Rx **←Transmit/Receive data→**

Note: Bidirectional signaling been around for decades, in all phone lines, and at multi-Gig in BASE-T PHYs since late 1990s. The cancellation requirement for a link with small loss is fairly relaxed
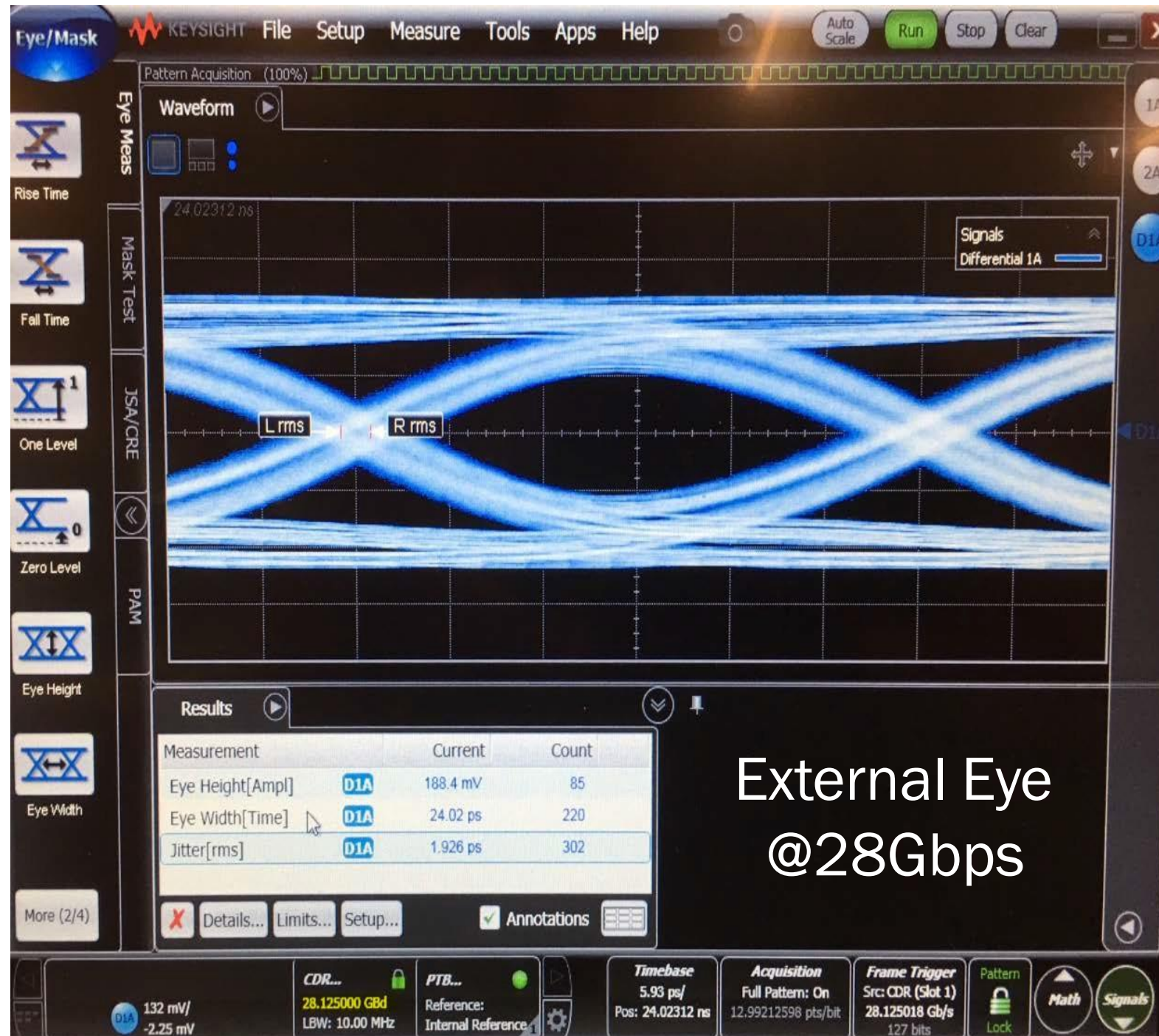
AQlink Demo Silicon in GF 14nm

LR: M1 ⇔ S2	MR: M2 ⇔ S1	SR: M3 ⇔ S0
2mm	10mm	25mm

M0   S3

traces on test chip

AQlink Test chip bump map

Package substrate

AQlink External Ports

External Eye @28Gbps

Consume. Collaborate. Contribute.

- One port per AQlink Quad core is an external port. Each external port trace:
  - 10mm package
  - 30mm board (1/2 package loss)
  → Effective 10+15=~25mm package
  → Loopback trace=2x25=50mm

- A differential external loop back operates error free up to ~25Gbps per direction (BER~1E-15)

- If loopback connected in single-ended fashion, the link operates error free up to ~15Gbps/direction (BER~1E-15)

- To provide further margin, and simplify the Phase alignment circuitry, maximum Bow-Turbo speed limited to 12Gbps/direction
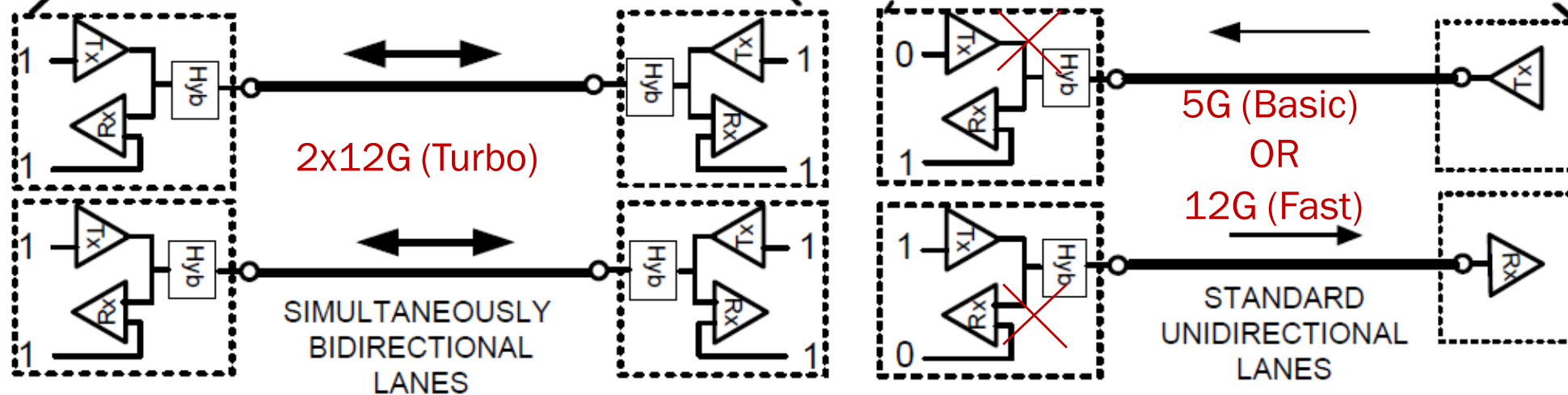
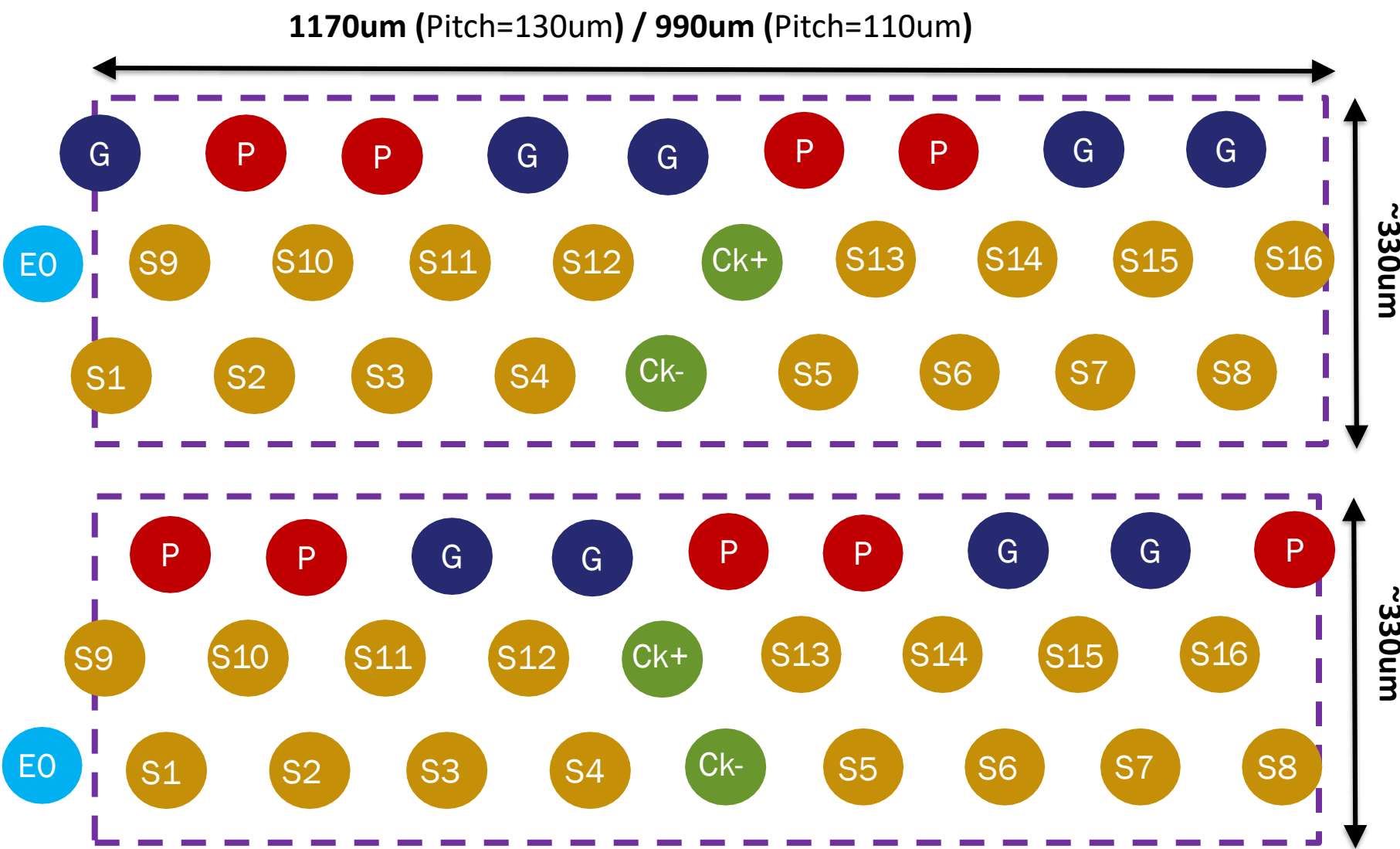# AQlink Internal Eye for Bidirectional 28Gbps (>1E^{11} bits per point)

Top Level View: Bow-Turbo Backward Compatible to Fast/Basic
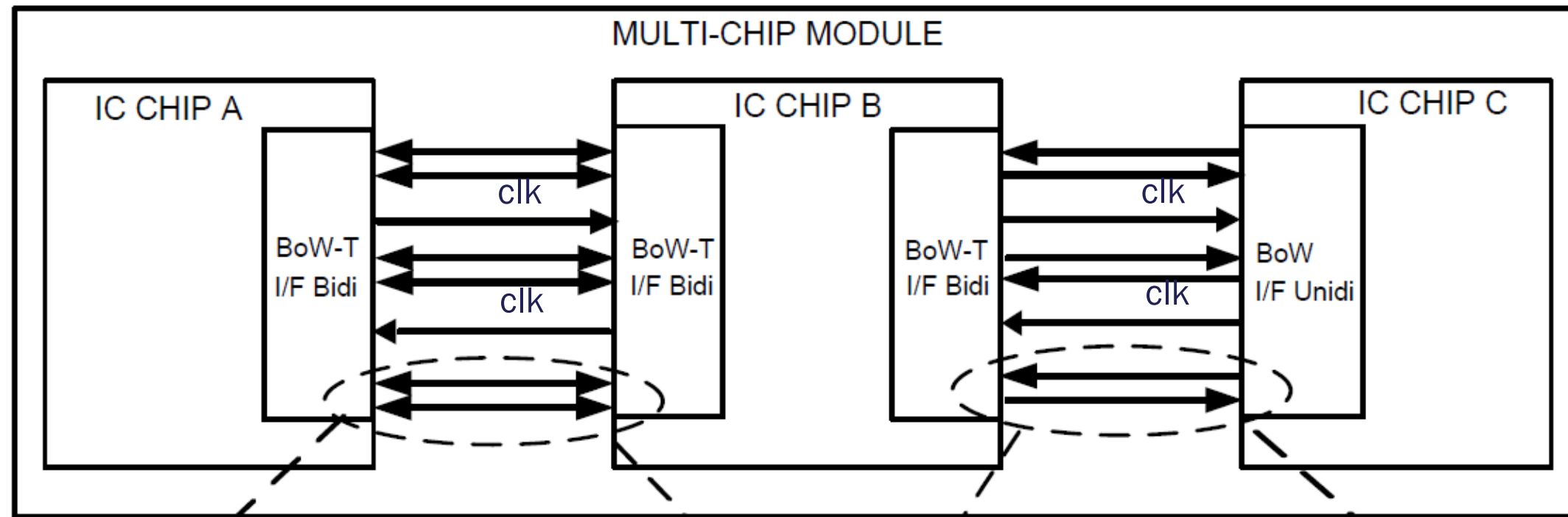
- A Bow-Turbo Core is configurable to be backward compatible to
  - BoW-Fast
    - by disabling Tx or Rx per lane
  - BoW-Basic
    - by disabling Tx or Rx per lane
    - disconnecting the line terminations

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BoW Bump Map Slice

**1170um (**Pitch=130um**) / 990um (**Pitch=110um**)**

~330um

~330um

16 Data + 2 Clock

16-bit wide parallel port
Configurable to be Backward compatible with
conventional parallel CMOS IOs
Slice with same circuitry & layout but different
RDL comes in 2 bump maps to create efficiency
in building larger BoW modules

Vertically stackable to increase throughput per die edge

1 Stack → 16x2x16Gbps/pad=512Gbps
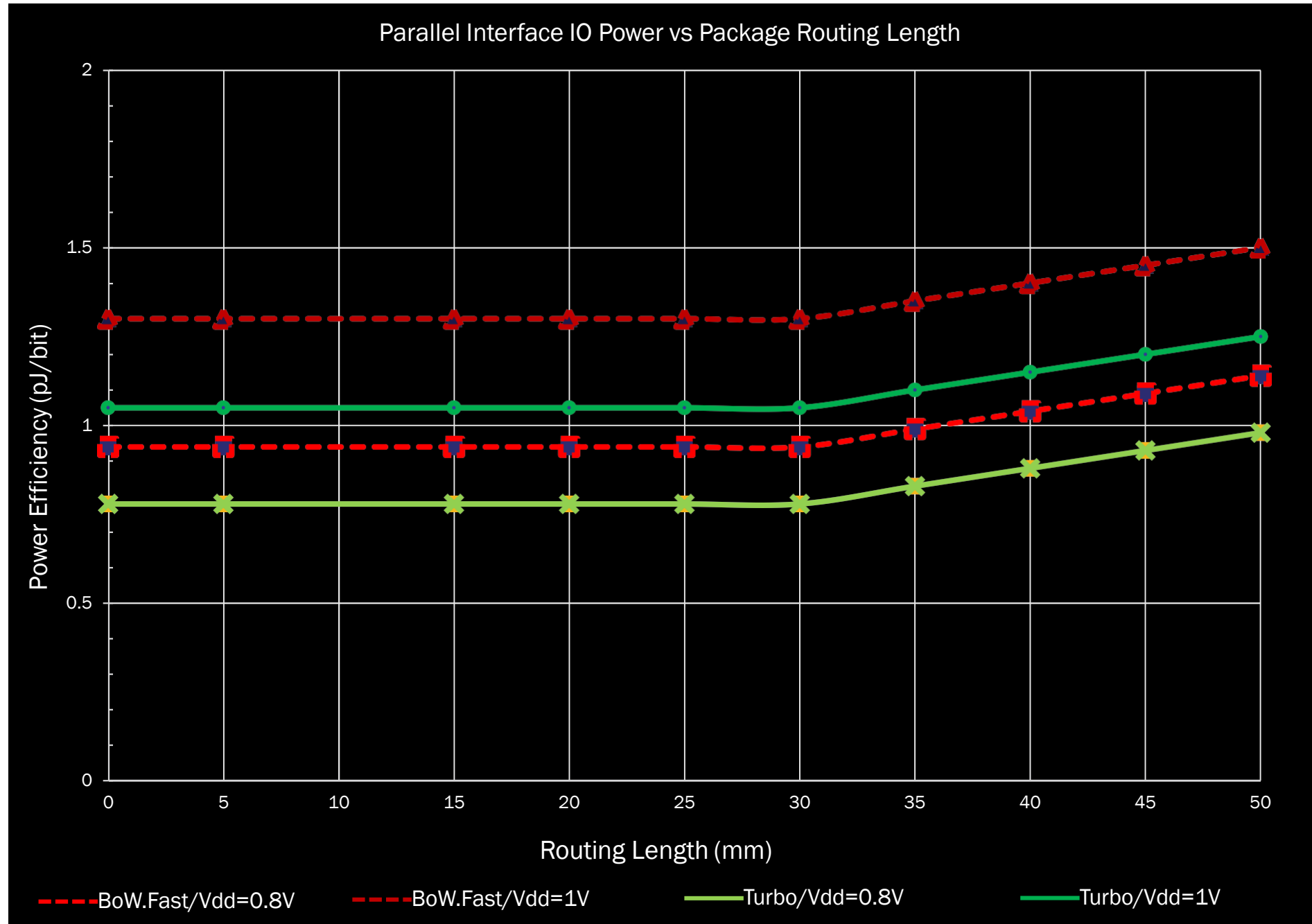
2 Stack → 16x2x16Gbps/pad=1024Gbps

Optional ECC

Optional bump can be added for an ECC bit per 16
data group to provide error correction capability
for BER<1E-30

Sample BoW Staggered Bump Map – Terabit Core
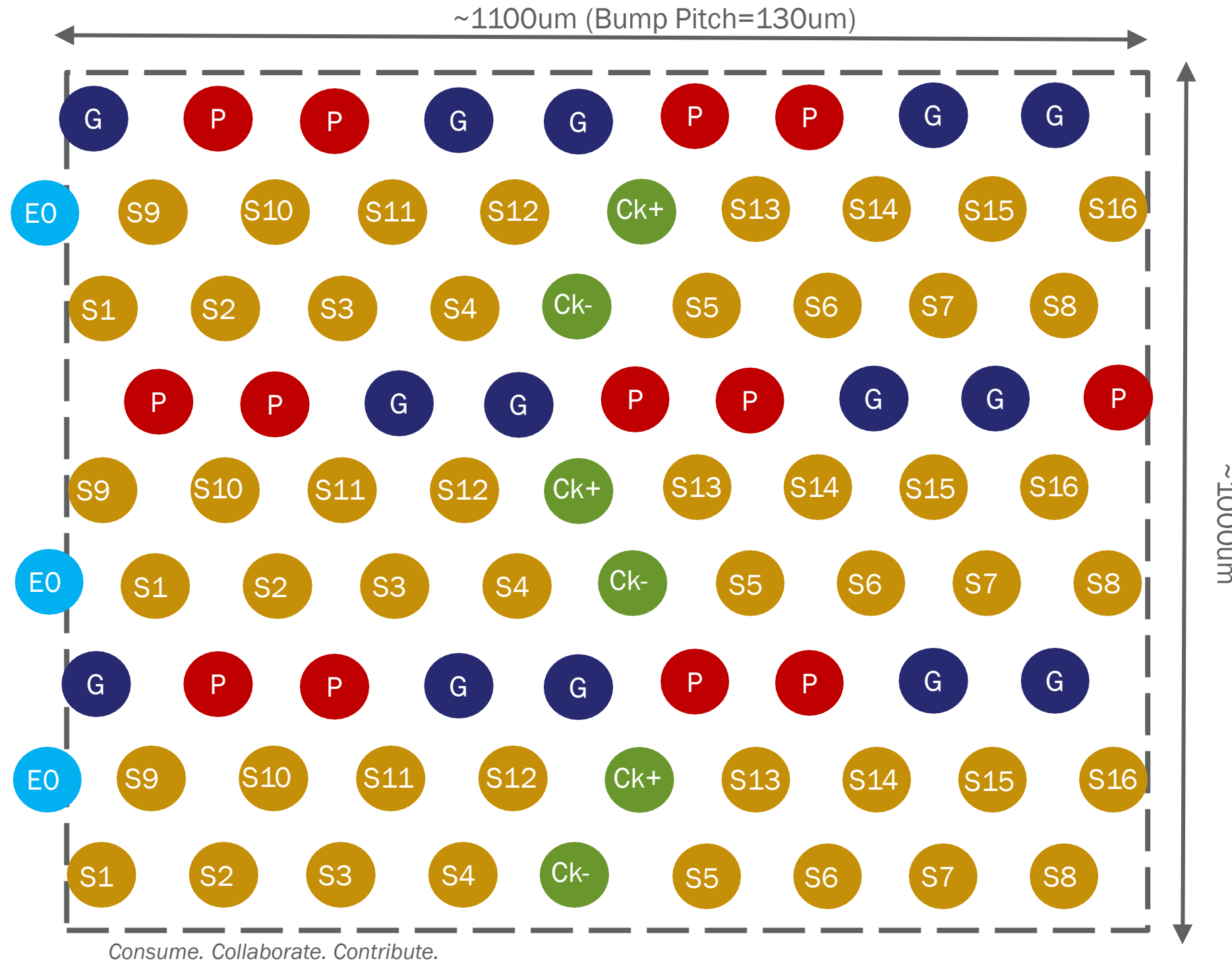
- Terabit Module has 48 data pads:
  - 48x2x10.5Gbps/pad=~1Tbps

- A single bump map can be used for Basic/Fast/Turbo
  - Important for backward compatibility

- Two clock ports per 16 ports
  - Configurable to be clock output or clock input pads when connected to non-Turbo interface (Tx or Rx only)

- Optional ECC
  - Option column to add one ECC bit per 16 data group at the edge of the Terabit Core bump map to provide error correction capability if BER<1E-20

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Power Efficiency of BoW Fast/Turbo

Parallel Interface IO Power vs Package Routing Length

- Assuming 80% data activity rate ➔ Baud*0.4

- Power efficiency calculated for data from the edge of the interface core on side to edge of interface core on the other side

BoW-Turbo Interface Performance Specifications

Parameter	Parameter
Single Supply Voltage	0.75V-1.2V (+/-5%)
Throughput/Trace (Max)	24Gbps (2x12Gbps)
Power Efficiency	0.75 pJ/bit (0.8V/30mm)
Package Trace length (Max)	50mm (Package Substrate: GZ41)
Latency	<2ns
Pad Pitch	130um
Terabit IP Core Dimension	Chip Edge: 1100um. Height:1000um
Power/Area for 1Tbps Throughput	750mW/1.1mm^2
BER	<1E-15 (No ECC) / <1E-20 (with ECC)
ESD / CDM protection	400V/100V
Silicon Proven	GF 14nm

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BoW Turbo Spec Summary

- Over 1Tbps/mm chip edge over organic substrate & 130um pad pitch
  - Throughput per port of at least 2x10.5Gbps (Max: 2x12Gbps)
  - Small per port area of <0.018mm^2
- Less than 1pJ/bit at Vdd=0.8V and trace length=50mm
- Single power supply that is compatible with synthesized logic core
- Concept proven in 14nm Silicon
- Backward compatible with BoW Basic/Fast die-die interfaces
  - Can use matching bump map as Bow Basic/Fast
  - A Chiplet with Bow Turbo interface can interoperate with other Chiplets using other BoW interfaces

Test Options

- Need discussion to find suitable test solutions
  - Calibration?
  - 1149.1 legacy
  - IEEE 1500 (HBM type systems)
  - Could define at speed / functional interop test if needed

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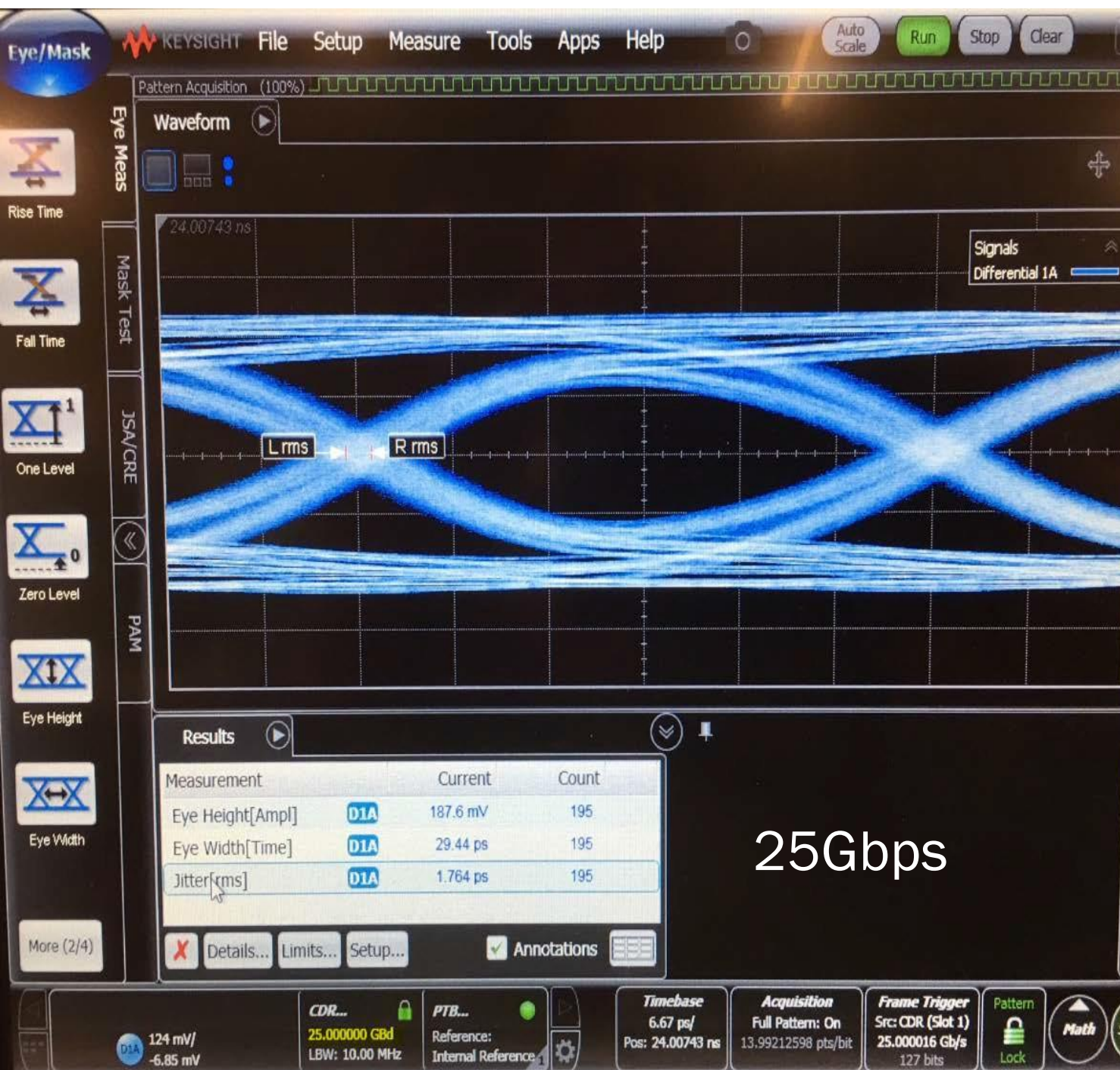Compute Project

Call for Volunteers

- We need your help to define a generally useful and interoperable interface

- What do we need?
  - Good ideas on what applications the BoW makes sense for
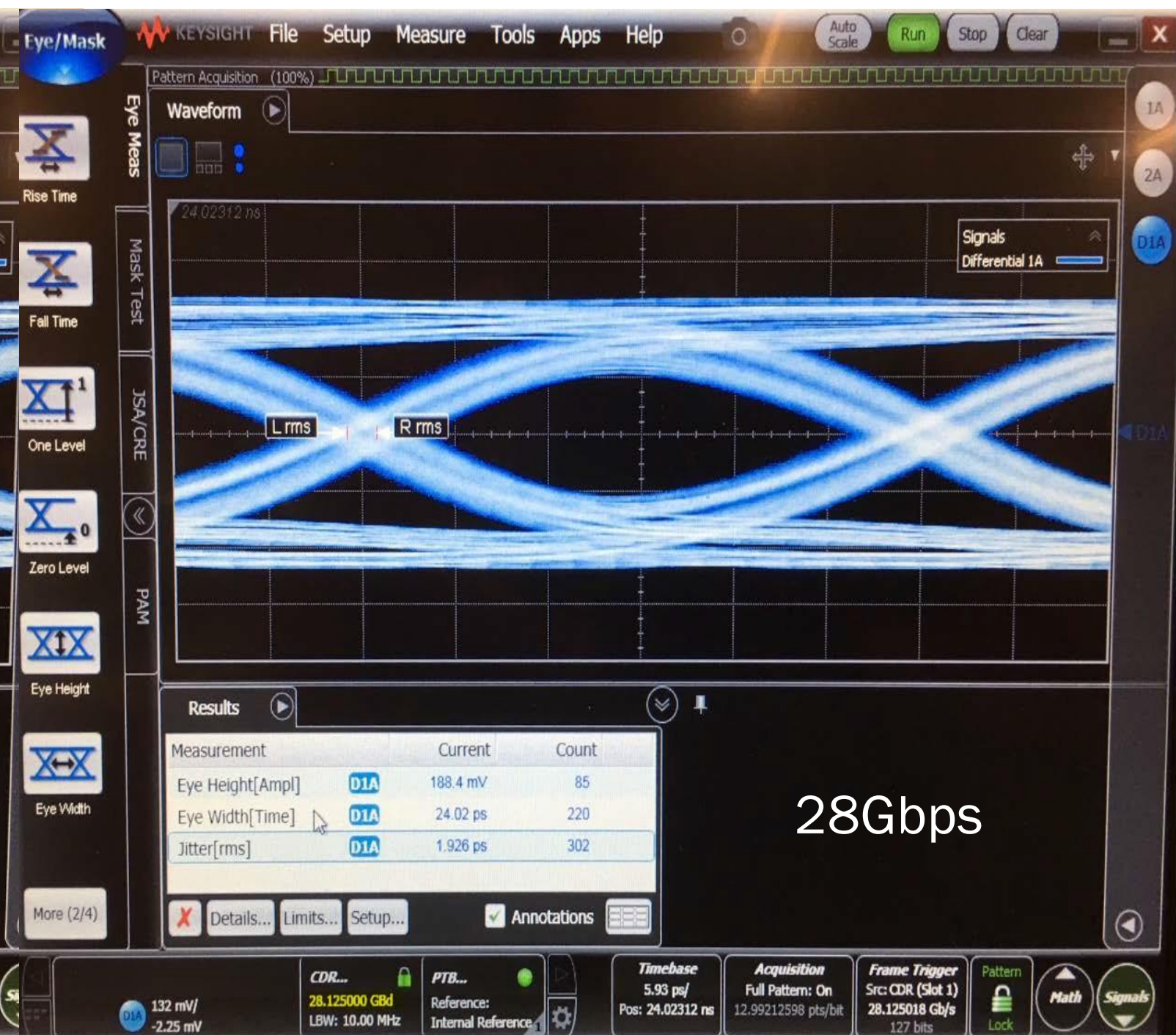 - SI/PI input for various options
  - Defining test for interface

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Thank You
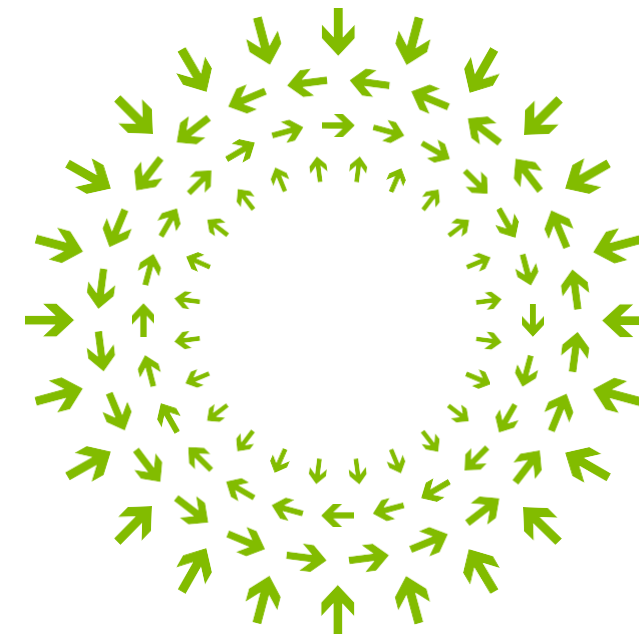
AQlink External Eye Diagrams
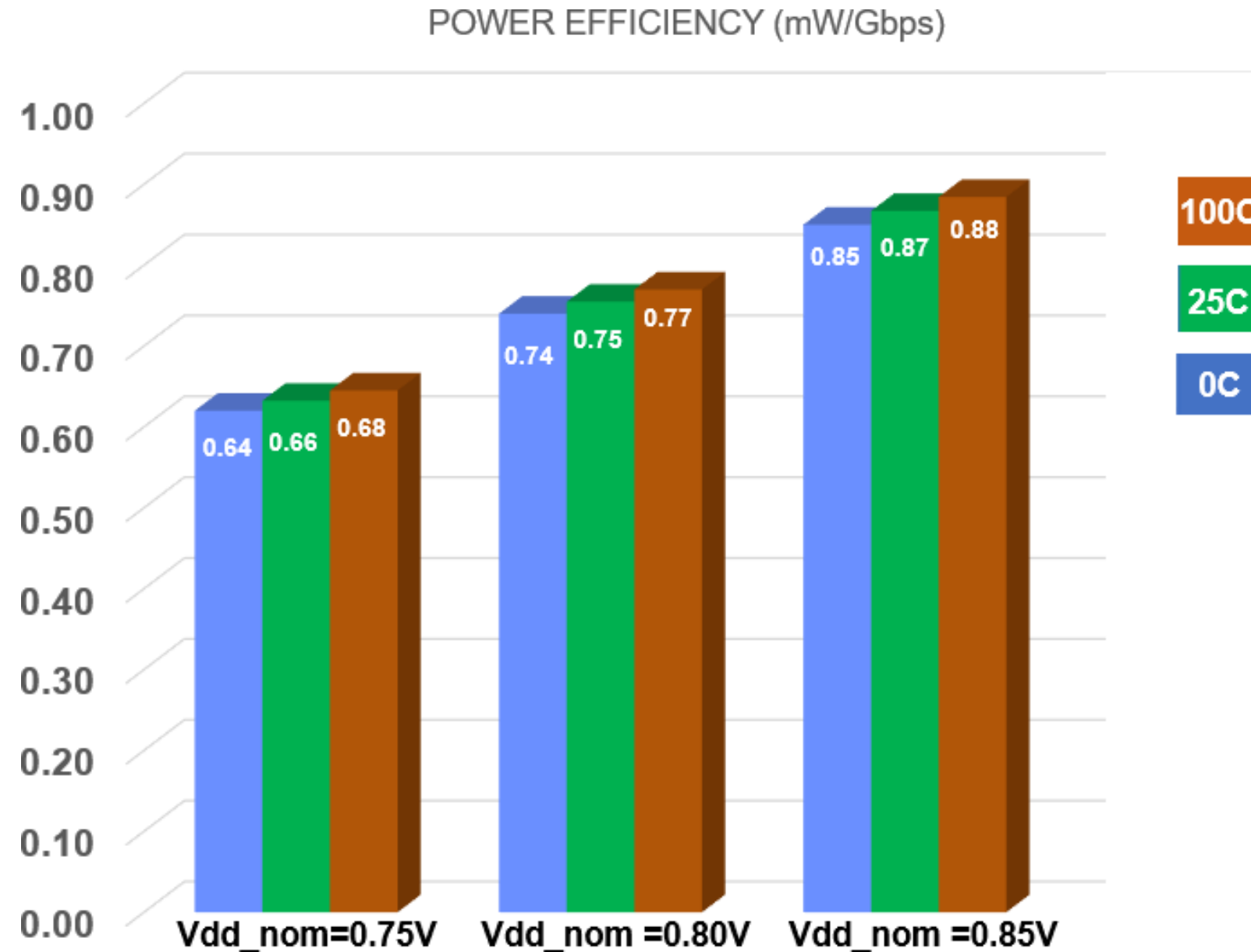

25Gbps

28Gbps

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ESD Measurements

- ESD performance measured for single-duplex mode on a 12mm x 14mm package

ESD Test Performed	Description	Test Status
HBM all pins	+/-250V (Spec)	Pass
HBM all pins	+/-400V	Pass
CDM all pins	+/-50V (Spec)	Pass
CDM all pins	+/-100V	Pass

AQlink Measured Power Efficiency (Quad) TT15 part

POWER EFFICIENCY (mW/Gbps)

Nominal Vdd range = 0.75V - 0.85V (+/-3% tolerance)