The HiWire Consortium Joins Forces with OCP

Standardizing Active Electrical Cables (AECs)

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Compute Project[®]



Presenters



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Agenda

- Why AECs Now?
- AEC Use cases
 - NIC TOR Connectivity
 - Distributed, Disaggregated Chassis (DDC)
- HiWire Consortium Background and Deliverables
- Challenge Ahead : 800G / 1.6T and beyond
- Call to Action



AEC Introduction







AEC Introduction

FEC and Gearbox Functions Integrated in the Cable







Why now? DACs are running aground..

Speed Lane / Cable	Max Reach	AWG / OD @ 2.5m	Cable Volume Ratio	% Ports Supporting solvable w/DAC	% HSDC Plugged with DAC
1Gb / 1Gb	100m	24 / 5.5mm	100%	100%	~100%
10Gb / 40Gb	10m	30 / 4.5 mm	67%	100%	~70%
28Gb / 100Gb	5m	30 / 6.6 mm	144%	100%	~55%
56Gb / 400Gb	3m	26 / 9.4mm	292%	100%	~35%
112Gb / 800Gb	2m	25 / 12.6mm 2m max	524%	?	?

HSDC front panel interconnect density is increasing rapidly DAC volume / pliability and thickness is reducing utility Optics are high power / high cost and reduced reliability AECs offer 75% reduction in DAC volume (back to Cat6e level @ 800G) AECs offer 50% less power and cost than Optics AECs maintain DAC MTBF levels (100M hrs+)



AEC Use Cases

Distributed Disaggregated Chassis (DDC) Applications



NIC (Server) to TOR





HSDC NIC-TOR cable densities start to exceed 100 connections/rack

Compute

At 56G and 112G/lane, DAC thickness and pliability becomes a blocking issue for HSDC interconnect

AEC enable a return to ~Cat6e thickness (6.8mm)

AECs also enable advanced digital functions

- DualTOR Active/Standby
- Line rate encryption / decryption
- Advanced control and telemetry

AECs grow to 75% of HSDC DAC NIC-TOR Connections by 2026



Source : 650 Group, Mar, 2022



Introduction to DDC

- OCP contributed specs
- NOS & Chassis distribution
- White-boxes + cabling
- Ecosystem breaks vendor lock

Building networks like cloud Scale / Economics / Innovation









DPE Compute



350Tb Core Router

- 24xJericho2C+ Whitebox Network Processors
- 20xRamon Whitebox Network Fabric
- DriveNets Network Management Software

960 x 400G LP AEC Fabric

- Left Side HPC-style 800m / 32AWG
- Right Side Tray Style 1.6km / 30AWG

DACs – not an option, no space AOCs – not an option no budget

- 2x as much fabric power / +20% cluster power
- 2x as much cost
- 100x worse MTBF much higher TCO





Reducing Embedded Carbon

Changing scale





multiple functions

Fits any location



DDC hardware lives longer and does more



- Credo founded the HiWire Consortium in 2019
- Objective : USB-IF for AECs
 - Specific cable implementation
 - Validation test specification
 - Enable 3rd party lab for validation
 - Mark for certification
- 46 members produced AEC specification v1.0 – contributed tc OCP
- Further work will be inside OCP



Challenge Ahead : 800G/1.6T+

- A single chip module setting may not be sufficient to cover all host to active pluggable cases at 112G/lane
- C2M Interface adds options
 - Already have short/long channel in IEEE 802.ck standard
 - Proposals to add

Project

- Link training to C2M (CMIS-LT or in-band)
- Non-standard hosts (more than traditional 16dB C2M link budget)
- New firmware features (hitless upgrades, local/remote control, event logging)
- Additional telemetry (mission mode FEC histogram, etc.)
- AEC Project charter is to evaluate these options, solicit feedback and create a reference implementation for 800G/1.6T AECs



Call to Action

- Join us and help develop the ecosystem of Plug & Play AECs
 First call: 6PM PDT, May 17th, <u>https://meet.goto.com/05/ocp-interconnects-sub-project-call</u>
- Key Activities
 - Add additional SKUs / speeds into the AEC specification
 - 200G / 400G baseline (56G/lane) is in place
 - 400G 4x100G with gearboing (28G/lane) is in place
 - 112G/lane (1, 2, 4, 8 and 16 lanes) needs to be done
 - 112G/lane bitmuxing needs to be defined and done
 - Develop and ratify a test specification
 - Discuss 3rd party lab enablement