The HiWire Consortium Joins Forces with OCP

Standardizing Active Electrical Cables (AECs)

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Agenda

• Why AECs Now?
• AEC Use cases
  – NIC – TOR Connectivity
  – Distributed, Disaggregated Chassis (DDC)
• HiWire Consortium Background and Deliverables
• Challenge Ahead : 800G / 1.6T and beyond
• Call to Action
AEC Introduction

- 200G/400G/800G Versions
- 200GAUI-4 / 400GAUI-8 / 800GAUI-8
- QSFP56/OSFP/QSFP-DD MSA

- Deterministic, Pre-calibrated line side (no AN/LT)
- Raw BER < 1e-8; Post-FEC BER < 1e-15
- Max 56ns latency
AEC Introduction

**FEC and Gearbox Functions Integrated in the Cable**

- Plug & Play Breakout / Speed Shifting Functions
- 28G / 56G / 112G Speed Shifting
- 1:2 and 1:4 Breakout Options
- OSFP / QSFP-DD / QSFP56 / QSFP28

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**L1 - Physical**
- <10dB Host Channel
- >30dB Line Channel

**L2 - Link**
- Speed Shift / FEC Termination
- Retimer

**L3 - Network**
- <10dB Host Channel

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Why now? DACs are running aground..

<table>
<thead>
<tr>
<th></th>
<th>Speed Lane / Cable</th>
<th>Max Reach</th>
<th>AWG / OD @ 2.5m</th>
<th>Cable Volume Ratio</th>
<th>% Ports Supporting solvable w/DAC</th>
<th>% HSDC Plugged with DAC</th>
</tr>
</thead>
<tbody>
<tr>
<td>1Gb / 1Gb</td>
<td>100m</td>
<td>24 / 5.5mm</td>
<td>100%</td>
<td>100%</td>
<td>~100%</td>
<td></td>
</tr>
<tr>
<td>10Gb / 40Gb</td>
<td>10m</td>
<td>30 / 4.5mm</td>
<td>67%</td>
<td>100%</td>
<td>~70%</td>
<td></td>
</tr>
<tr>
<td>28Gb / 100Gb</td>
<td>5m</td>
<td>30 / 6.6mm</td>
<td>144%</td>
<td>100%</td>
<td>~55%</td>
<td></td>
</tr>
<tr>
<td>56Gb / 400Gb</td>
<td>3m</td>
<td>26 / 9.4mm</td>
<td>292%</td>
<td>100%</td>
<td>~35%</td>
<td></td>
</tr>
<tr>
<td>112Gb / 800Gb</td>
<td>2m</td>
<td>25 / 12.6mm</td>
<td>524%</td>
<td>?</td>
<td>?</td>
<td></td>
</tr>
</tbody>
</table>

HSDC front panel interconnect density is increasing rapidly
DAC volume / pliability and thickness is reducing utility
Optics are high power / high cost and reduced reliability
AECs offer 75% reduction in DAC volume (back to Cat6e level @ 800G)
AECs offer 50% less power and cost than Optics
AECs maintain DAC MTBF levels (100M hrs+)
AEC Use Cases

Distributed
Disaggregated Chassis
(DDC) Applications

NIC (Server) to TOR
NIC – TOR AEC Adoption

HSDC NIC-TOR cable densities start to exceed 100 connections/rack

At 56G and 112G/lane, DAC thickness and pliability becomes a blocking issue for HSDC interconnect

AEC enable a return to ~Cat6e thickness (6.8mm)

AECs also enable advanced digital functions
- DualTOR Active/Standby
- Line rate encryption / decryption
- Advanced control and telemetry

AECs grow to 75% of HSDC DAC NIC-TOR Connections by 2026

Source: 650 Group, Mar, 2022
Introduction to DDC

- OCP contributed specs
- NOS & Chassis distribution
- White-boxes + cabling
- Ecosystem breaks vendor lock

Building networks like cloud
Scale / Economics / Innovation
350Tb DDC Router from OCP’21

- 350Tb Core Router
  - 24xJericho2C+ Whitebox Network Processors
  - 20xRamon Whitebox Network Fabric
  - DriveNets Network Management Software

- 960 x 400G LP AEC Fabric
  - Left Side HPC-style 800m / 32AWG
  - Right Side Tray Style 1.6km / 30AWG

- DACs – not an option, no space
- AOCs – not an option no budget
  - 2x as much fabric power / +20% cluster power
  - 2x as much cost
  - 100x worse MTBF – much higher TCO

Reducing Embedded Carbon

Changing scale

multiple functions

Fits any location

DDC hardware lives longer and does more
HiWire Consortium joins Forces with OCP

- Credo founded the HiWire Consortium in 2019
- Objective: USB-IF for AECs
  - Specific cable implementation
  - Validation test specification
  - Enable 3rd party lab for validation
  - Mark for certification
- 46 members produced AEC specification v1.0 – contributed to OCP
- Further work will be inside OCP
Challenge Ahead: 800G/1.6T+

• A single chip – module setting may not be sufficient to cover all host to active pluggable cases at 112G/lane

• C2M Interface adds options
  ─ Already have short/long channel in IEEE 802.ck standard
  ─ Proposals to add
    • Link training to C2M (CMIS-LT or in-band)
    • Non-standard hosts (more than traditional 16dB C2M link budget)
    • New firmware features (hitless upgrades, local/remote control, event logging)
    • Additional telemetry (mission mode FEC histogram, etc.)

• AEC Project charter is to evaluate these options, solicit feedback and create a reference implementation for 800G/1.6T AECs
Call to Action

• Join us and help develop the ecosystem of Plug & Play AECs
  – First call: 6PM PDT, May 17th, https://meet.goto.com/05/ocp-interconnects-sub-project-call

• Key Activities
  – Add additional SKUs / speeds into the AEC specification
    • 200G / 400G baseline (56G/lane) is in place
    • 400G – 4x100G with gearboing (28G/lane) is in place
    • 112G/lane (1, 2, 4, 8 and 16 lanes) needs to be done
    • 112G/lane bitmuxing needs to be defined and done
  – Develop and ratify a test specification
  – Discuss 3rd party lab enablement