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ODSA: Optical I/O Chiplet for Heterogeneous Computing

SERVER

Optical I/O Chiplet for Heterogeneous Computing

Shahab Ardalan, PhD, Ayar Labs

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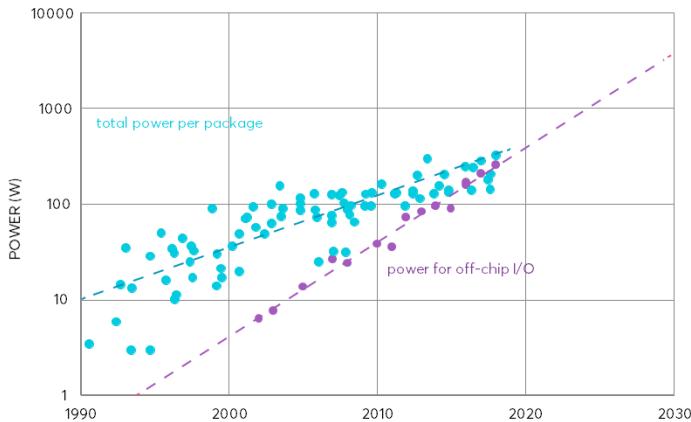


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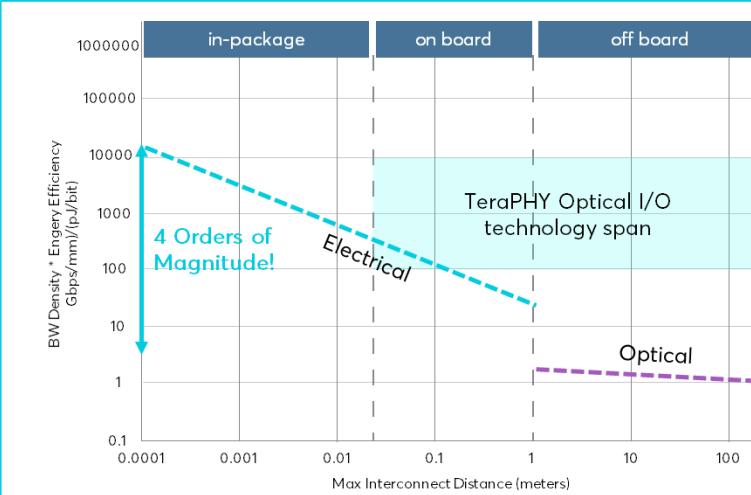


The Case for In-Package Optical I/O



Problem

- Package performance is pin limited
- Power for off-chip I/O increasing and unsustainable



Problem

- Large energy and bandwidth penalties for short distance data movement
- Restricts system architecture design flexibility

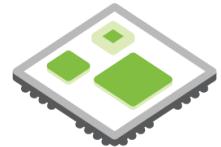
Source: Xeon Cascade Lake, Anandtech April 2019; Source: G. Keeler, DARPA ERI 2019

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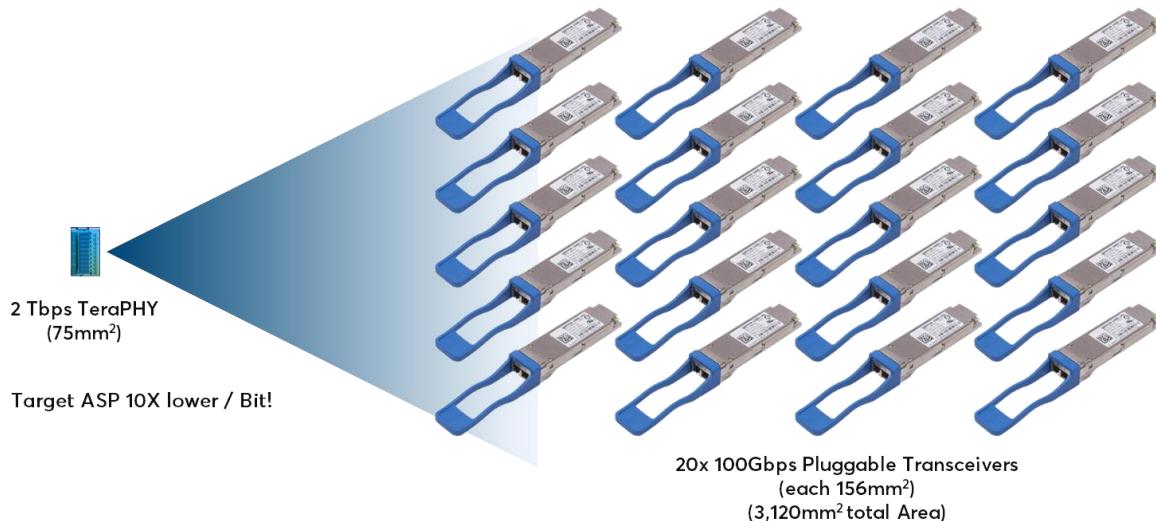
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Chiplet for Optical I/O



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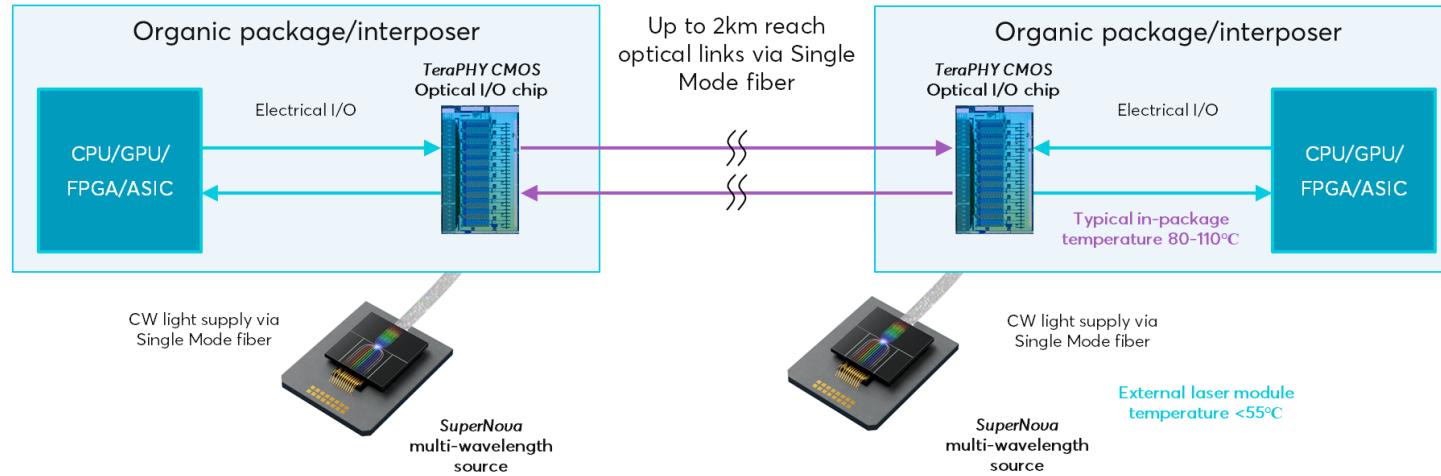
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Optical I/O requires denser, lower latency, and lower power technology than currently in the market

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Ayar Labs Optical I/O Architecture



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1000x the bandwidth density at 1/10th the power and latency of copper, and at distances of up to 2km

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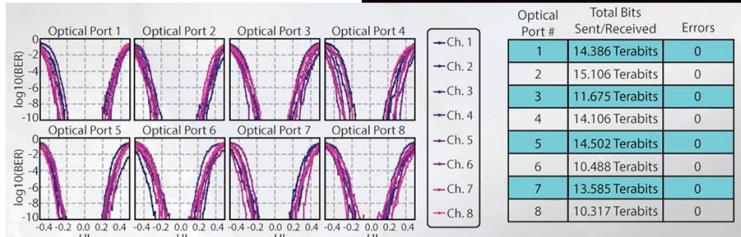
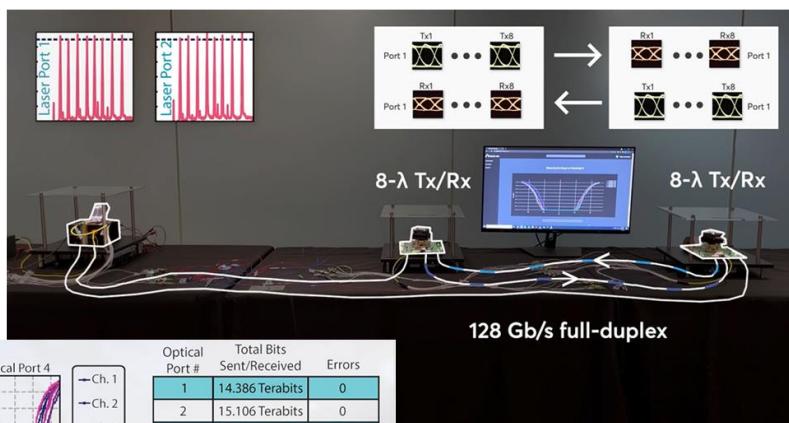
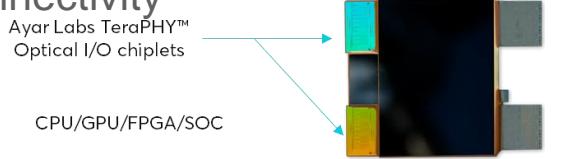




Industry First Optical Chiplet

Terabit Link Demonstration for Chip-to-Chip Connectivity

- Error free, full-duplex 128 Gb/s per optical port
- TeraPHY™ chiplet with 8 WDM optical channels per optical port
- Powered by our remote SuperNova™ light source
- Total bandwidth of 1.024 Tbps
- Less than 5 pJ/bit energy efficiency



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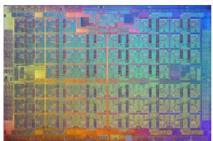
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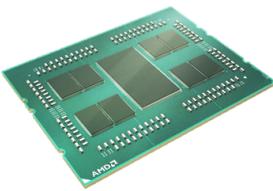
Optical I/O can Redefine the CPU “Socket”

Past



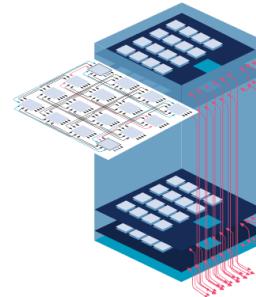
Intel® Xeon Phi
8 Billion Transistors

Present



AMD's 64-core EPYC CPU
~40 Billion Transistors

Future with Optical I/O



The Rack is the Socket
20+ Trillion Transistors

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CPU's are many compute cores and functions wrapped in a power efficient, low latency, high bandwidth interconnect. Optical I/O has these characteristics but with extended reach

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Call to Action

- ODSA/BoW meeting every Wednesday at 9:00 AM
- ODSA/BoW Spec will be released by end of the year
- Check ODSA/wiki page at
 - <https://www.opencompute.org/wiki/Server/ODSA>
 - More information please contact us
 - Bapi Vinnakotya: bapi.vinnakota@ocproject.net
 - Shahab Ardalani: shahab@ayarlabs.com

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