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Thermal consideration between Monolithic die and 2.5D/3D packages



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Thermal consideration between Monolithic die and 2.5D/3D packages

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- Background
 - As Moore's Law slows further, we begin to face many fundamental limits related to the size and layout of a chip. Designers are looking for building devices in the vertical direction, such as 2.5D and 3D IC packaging solutions.
 - Thermal management becomes critical and challenge when the power dissipation level and the level of complexity in package architectures increases. Under this circumstance, exploring the integrated thermal management from package level to the board level is needed to ensure the performance and reliability of high power components.







Introduction

 In this presentation, we will compare the thermal performance among various package options, including **monolithic die**, MCM,
2.5D, and 3D, we will also touch a little bit on the thermal solutions to help the advanced package cooling.



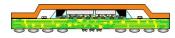
Monolithic Die МСМ 2.5 D 3D SRAM _____ AMARAM AMARAM AMARAM SRAM ASIC 0000000 65mm 65mm 17.6mm 1 29mm 20mm 20mm 17mm 20mm 17mm 17mm 17.6mm 65mm SRAM 65mm 17.6mm 36mm 5mm 36mm 38mm 29mm SRAM ASIC 36mm SRAM ASIC Î1mm Space0.1mm CF 39.2mm OPEN POSSIBILITI<mark>ES</mark>.

Package Design and Model Setup

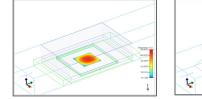
	Option 0	Option 1	Option 2	Option 3			
Package Option	Monolithic	МСМ	2.5D Interposer	3D			
Package size	65mmX65mm						
Die size	825mm2 (~29mmX29mm)	One ASIC 750mm2 (20mmX36mm) Two SRAM 300mm2 (17mmX17.6mm)					
Die thickness	720um	720um	554um	ASIC: 100 um SRAM: 100um			
Total Power	214W	ASIC: 150W, SRAM: 32W					

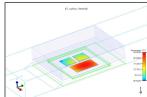


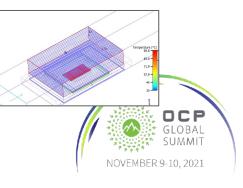
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- Ambient T = 30C
- 20 CFM volume flow rate
- same TIM and lid
- 1U aluminum fin heat sink with copper base







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Simulation Results

	Option 0	Option 1	Option 2	Option 3	
Package Design	Monolithic	МСМ	2.5D Interposer	3D	
Ratio of die to package footprint	20%	32%	32% (dies are placed closer to each other)	17%	
Tcase,center (C)	82.9	73.4	78.3	89.6	
Tj, ASIC (C)	89.1	84.3	84.5	99	
Tj, SRAM1 (C)	-	73.4	75.8	98.8	
Tj, SRAM2 (C)	-	72	74.7	98.5	



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Thermal Observations

- Tj of monolithic die is slightly higher that of MCM and 2.5D packages
- Tj of 3D "<u>stacked</u>" dies are much higher as expected
- For multi-chiplets design, Tcase, center is not always a good indicator to design the cooling solutions (MCM v.s. 2.5D interposer)
- When dies are placed closer to each other, higher power dies will heat the lower power dies. The impact gets bigger when the power difference between the ASIC and SRAM gets bigger.

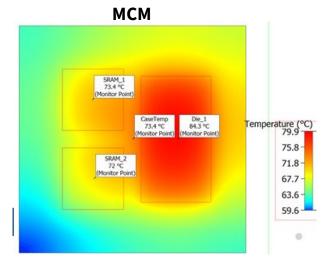
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Thermal Consideration

- Factors to be considered:
 - higher cost of monolithic silicon development
 - complex manufacturing of 3D stacked dies
 - hot spots or allowed max operation temperatures of ASIC and SRAM on MCM or 2.5D modules.
 - vapor chambers to control the temperatures





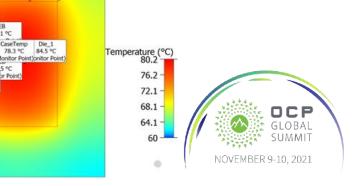
SRAM 1

75.8 % Monitor Point)E

SRAM 2

78.3 °C

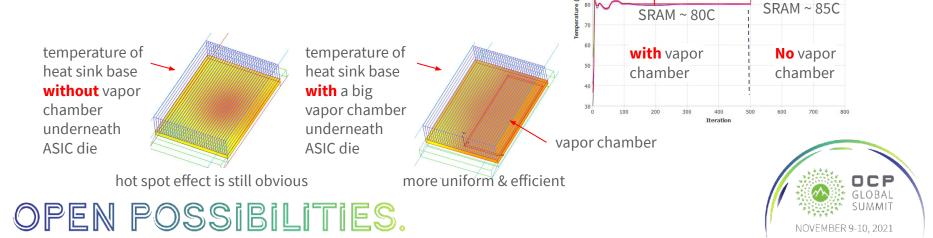
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Vapor Chamber

- A vapor chamber solution (use option 2 as example, but with ASIC power 300W, each SRAM 32W, 36 CFM volume flow rate)
- Vapor chamber is used to
 - conduct heat to outside heat sink base efficiently
 - lower overall temperatures, including hot spots
 - control temperature distribution & gradient



120

ASIC ~ 99.7C

△~20C



 $\Delta \sim 26C$

ASIC ~ 111C

Conclusion and Discussions

- MCM and 2.5D interposer package design have better thermal performance comparing to the monolithic die and the 3D package
- Use the T_case, center for early stage thermal design might be misleading without considering the differences of package design.
- Various cooling solutions can be used to mitigate the issues of hot spots such as:
 - Vapor chamber as discussed in this study already
 - lidless package although might have mechanical risk in certain packages
 - TIM material improvement such as use metal tims (Indium)



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Call to Action

- Expansion of the ODSA community
- Collaboration of companies under ODSA
- Development of power management methodologies to predict the thermal reliability of silicon
- Correlation of test and simulation
- Project wiki with latest specifications: <u>https://www.opencompute.org/wiki/Server/ODSA</u>
- Mailing list: main@OCP-All.groups.io



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Thank you!

