OCP NIC 3.0 PCI Express® Test Fixture Updates

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Agenda

• Challenges and Goals
• PCI-SIG® and OCP Ecosystem
• Test Fixtures
  • Design
  • Test and Validation
• Next Steps
• Demo
OCP PCIe® Electrical Conformance

Challenges

- Lack of standard mechanism to measure and assess electrical design margin of OCP NIC

Current Methods

- Primarily relies on functional interoperability
- Lacks visibility into quantified margins to ensure consistent and predictable performance at scale
- Custom fixtures for “FYI” assessments
Goal: Standardize PCIe Conformance for OCP

- Deterministic and standardize methodology across compute and storage platforms
- Enable interoperability across OCP NIC add-in cards and platforms
- Electrical conformance to PCIe 3.0+ technology signaling rates for interoperability
- Open sourced to OCP Community to enable independent qualification
  - System vendors
  - 3rd party labs
  - Mezzanine add-in card vendors
  - Full integration with standard industry equipment
PCI-SIG and OCP Ecosystem

- Compliance Program
PCI-SIG Compliance Program Overview

• PCIe® 4.0 Test Program Under Development
• PCIe 3.0 Integrators List testing (started April 2013)
  • Tests for 2.5, 5, 8 GT/s maximum data rates
• Card Electromechanical (CEM) form factor and “U.2” only
  • Other devices can get on Integrator’s List if tested separately as CEM w/adapter
• M.2 (Socket 3) under development
• Fixtures and tests provided through PCI-SIG
PCI-SIG Compliance Workshops

• Set of “Gold Suite” tests – both protocol and electrical plus interoperability with other attending devices
  • E.g. Transmitter and Receiver signal quality, PLL Bandwidth, Link Equalization process
  • Must pass *ALL* gold suite tests & 80% of interops
• Held at an atrium-style hotel, systems get rooms, add-in cards travel room-to-room
• Advance registration – typically closes a month ahead
PCI-SIG PCIe 4.0 16GT/s Fixtures

- **Compliance Base Board (CBB)** & **Compliance Load Board (CLB)** which “emulate” a motherboard & add-in card
- Both used for calibration then DUT replaces one
- Variable ISI Boards new with 4.0 program
OCP Fixtures

- Test fixtures
- Test procedures
Fixture Design

- Design and specification
  - CLB: PCIe 3.0 specification (low-loss) & PCIe 4.0 specification (mid-loss)
  - CBB: Single Design
- Design source files to be made available on OCP website
- Both CBB & CLB require use of PCI SIG® ISI board for PCIe 4.0 technology
Test Procedure

• How to use these fixtures for PCIe Electrical Testing with OCP platforms
Fixture Test and Verification

- Characterization data
Test Accessories

- SMP to SMA (3.5mm) Cables* (Huber+Suhner PN: 80351638 or 024E573HTCR092HTCR2.5PM1PS-STD)
- 1 meter 3.5mm coaxial Cables - **Required (Huber Suhner PN:85104455 or PCI SF126E/11PC35/11PC35/914mm)
- Female to Female 3.5mm Adaptors -optional (Maury Microwave PN: CC-A-292-FF)
- 1 foot SMP Cables* (Huber+Suhner PN: 80351639 or Minibrand L25R-12HTPM+1PS-STD)
- SMP to SMA (3.5mm) Adaptors – optional (Huber+Suhner PN: 80318038)

*These cables are supplied by the PCISIG with your PCIe 4.0 CBB/CLB Fixture Kits

**These cables must be Purchased separately
PCISIG ISI Board for 16GT/s Testing
PCle 4.0 Receiver Testing @16GT/s

16 GT/s PRBS Generator

Fixed TX EQ

Rj Source
SJ Source
Diff Interference
CM Interference
Small EW Adjust
Small EH Adjust

15 mV / .3 UI at E-12 BER

3dB Endpoint Package Model
5dB Endpoint Package Model

Post Processing Scripts:
Rx pll model
Behavioral CTLE/DFE
Behavioral CDR

PCIe 4.0 RX Calibration Eye
What Next?

• Enablement with PCI SIG Serial Working Group ongoing!
• Fixture Availability:
  • Design Files are located on the wiki:
    • Schematic/Layout Source and production files
    • Users Manual
• Procurement channel
  • UNH-IOL
    • Test Reports
Live Demo
Call to Action

- Join Server Mezzanine working group to contribute


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