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OCP NIC 3.0 PCI Express® Test Fixture Updates

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Agenda

- Challenges and Goals
- PCI-SIG® and OCP Ecosystem
- Test Fixtures
  - Design
  - Test and Validation
- Next Steps
- Demo

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OCP PCIe® Electrical Conformance

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Challenges

- Lack of standard mechanism to measure and assess electrical design margin of OCP NIC

Current Methods

- Primarily relies on functional interoperability
- Lacks visibility into quantified margins to ensure consistent and predictable performance at scale
- Custom fixtures for “FYI” assessments

Goal: Standardize PCIe Conformance for OCP

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- Deterministic and standardize methodology across compute and storage platforms
- Enable interoperability across OCP NIC add-in cards and platforms
- Electrical conformance to PCIe 3.0+ technology signaling rates for interoperability
- Open sourced to OCP Community to enable independent qualification
  - System vendors
  - 3rd party labs
  - Mezzanine add-in card vendors
- Full integration with standard industry equipment

PCI-SIG and OCP Ecosystem

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- Compliance Program

PCI-SIG Compliance Program Overview

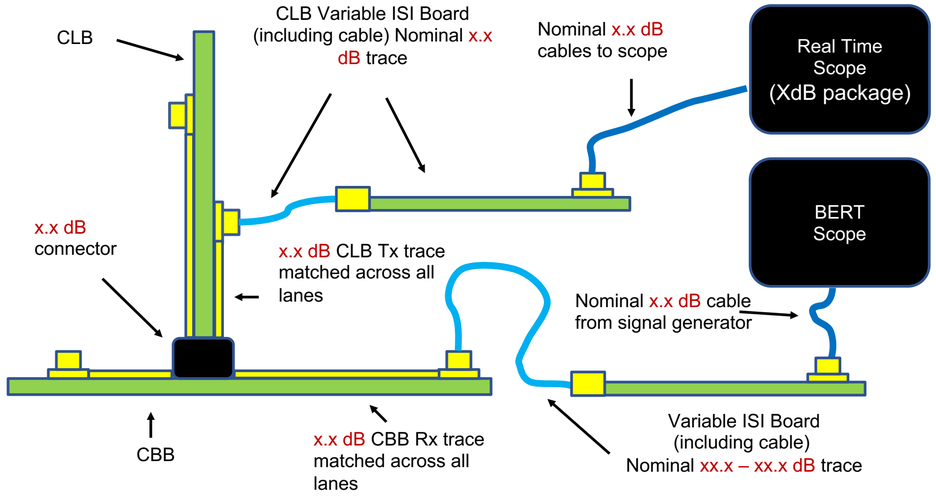
- PCIe® 4.0 Test Program Under Development
- PCIe 3.0 Integrators List testing (started April 2013)
  - Tests for 2.5, 5, 8 GT/s maximum data rates
- Card Electromechanical (CEM) form factor and “U.2” only
  - Other devices can get on Integrator’s List if tested separately as CEM w/adapter
  - M.2 (Socket 3) under development
- Fixtures and tests provided through PCI-SIG

PCI-SIG Compliance Workshops

- Set of “Gold Suite” tests – both protocol and electrical plus interoperability with other attending devices
  - E.g. Transmitter and Receiver signal quality, PLL Bandwidth, Link Equalization process
  - Must pass *ALL* gold suite tests & 80% of interops
- Held at an atrium-style hotel, systems get rooms, add-in cards travel room-to-room
- Advance registration – typically closes a month ahead

PCI-SIG PCIe 4.0 16GT/s Fixtures

- ***C***ompliance ***B***ase ***B***oard (CBB) & ***C***ompliance ***L***oad ***B***oard (CLB) which “emulate” a motherboard & add-in card
  - Both used for calibration then DUT replaces one
  - Variable ISI Boards new with 4.0 program



OCP Fixtures

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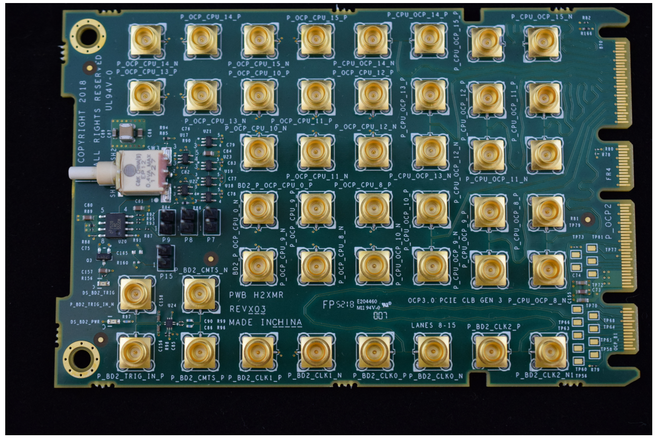
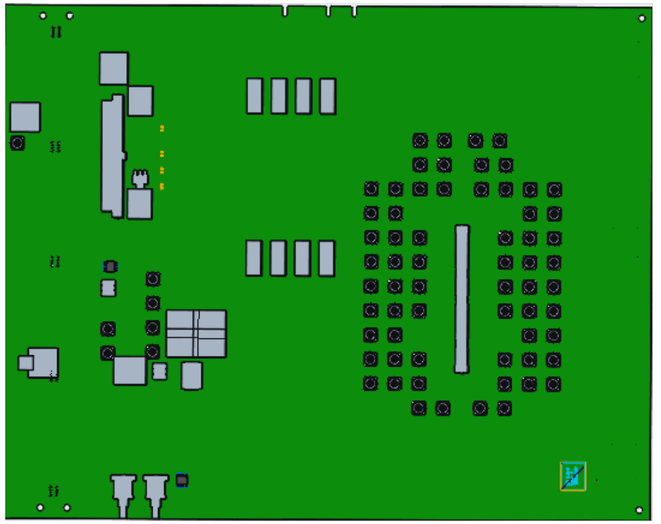
- Test fixtures
- Test procedures

Fixture Design

- Design and specification
  - CLB: PCIe 3.0 specification(low-loss) & PCIe 4.0 specification(mid-loss)
  - CBB: Single Design
  - Design source files to be made available on OCP website
  - Both CBB & CLB require use of PCI SIG® ISI board for PCIe 4.0 technology





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Test Procedure

- How to use these fixtures for PCIe Electrical Testing with OCP platforms

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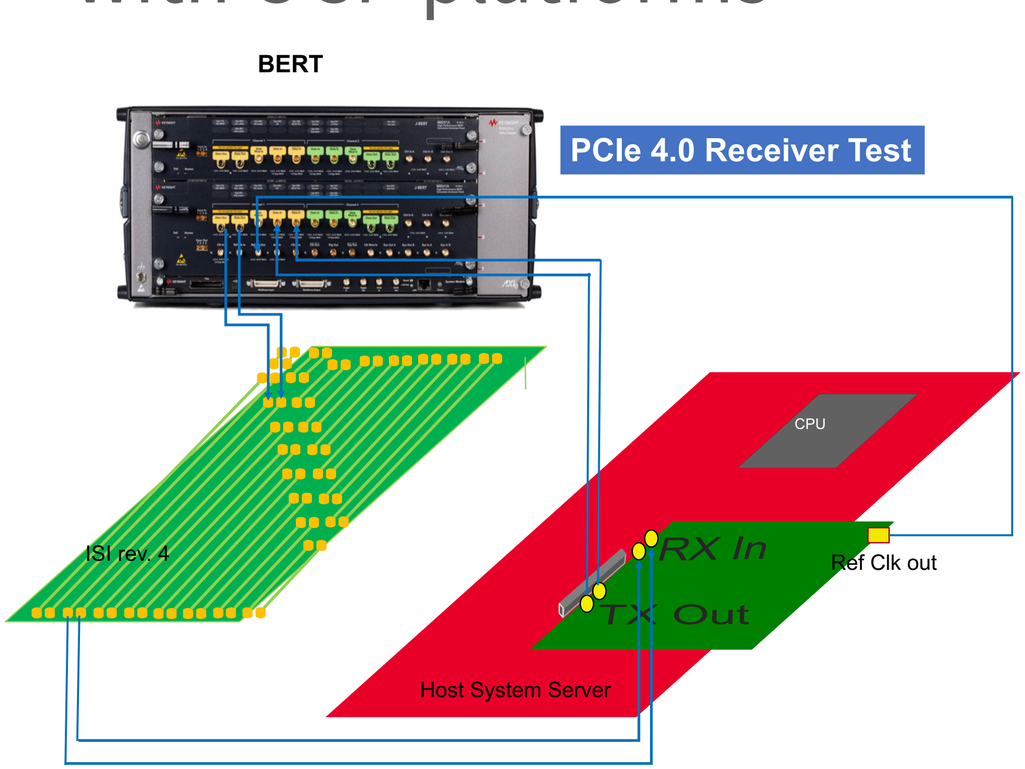

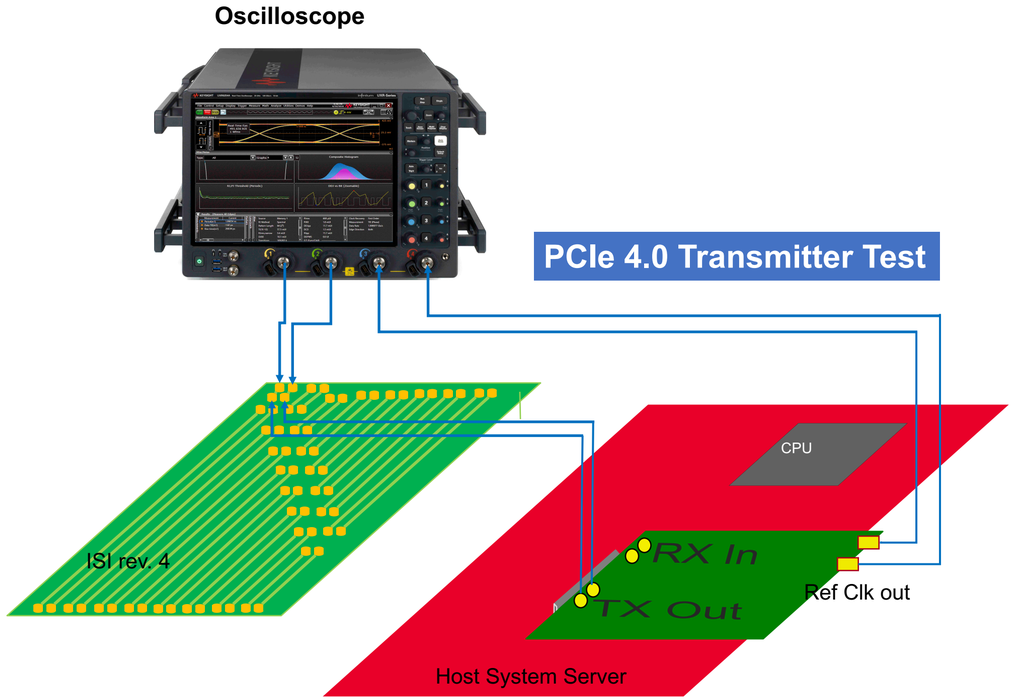

Fixture Test and Verification

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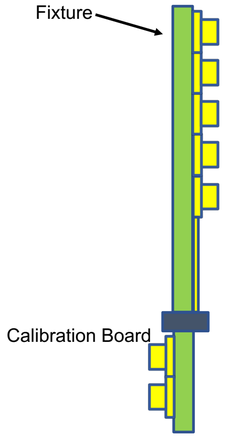
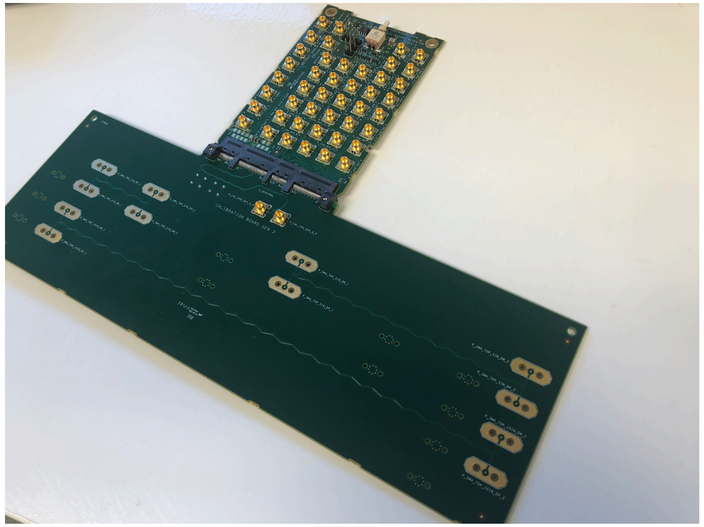
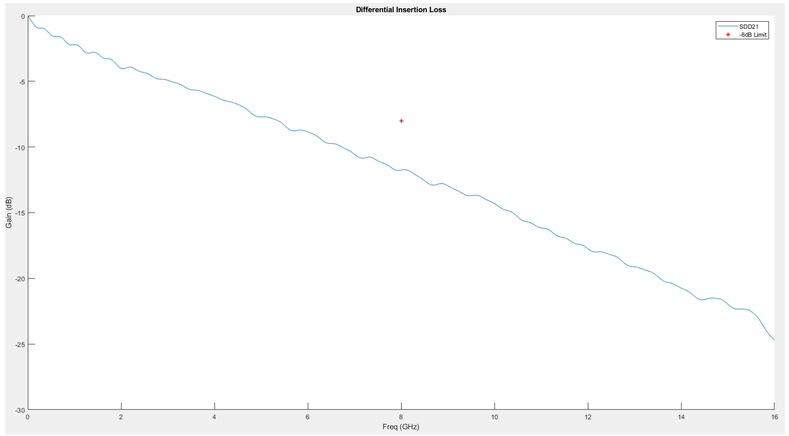
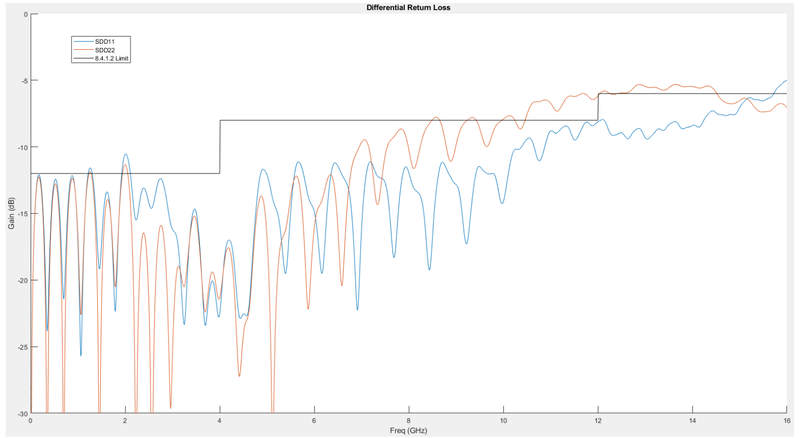
- Characterization data

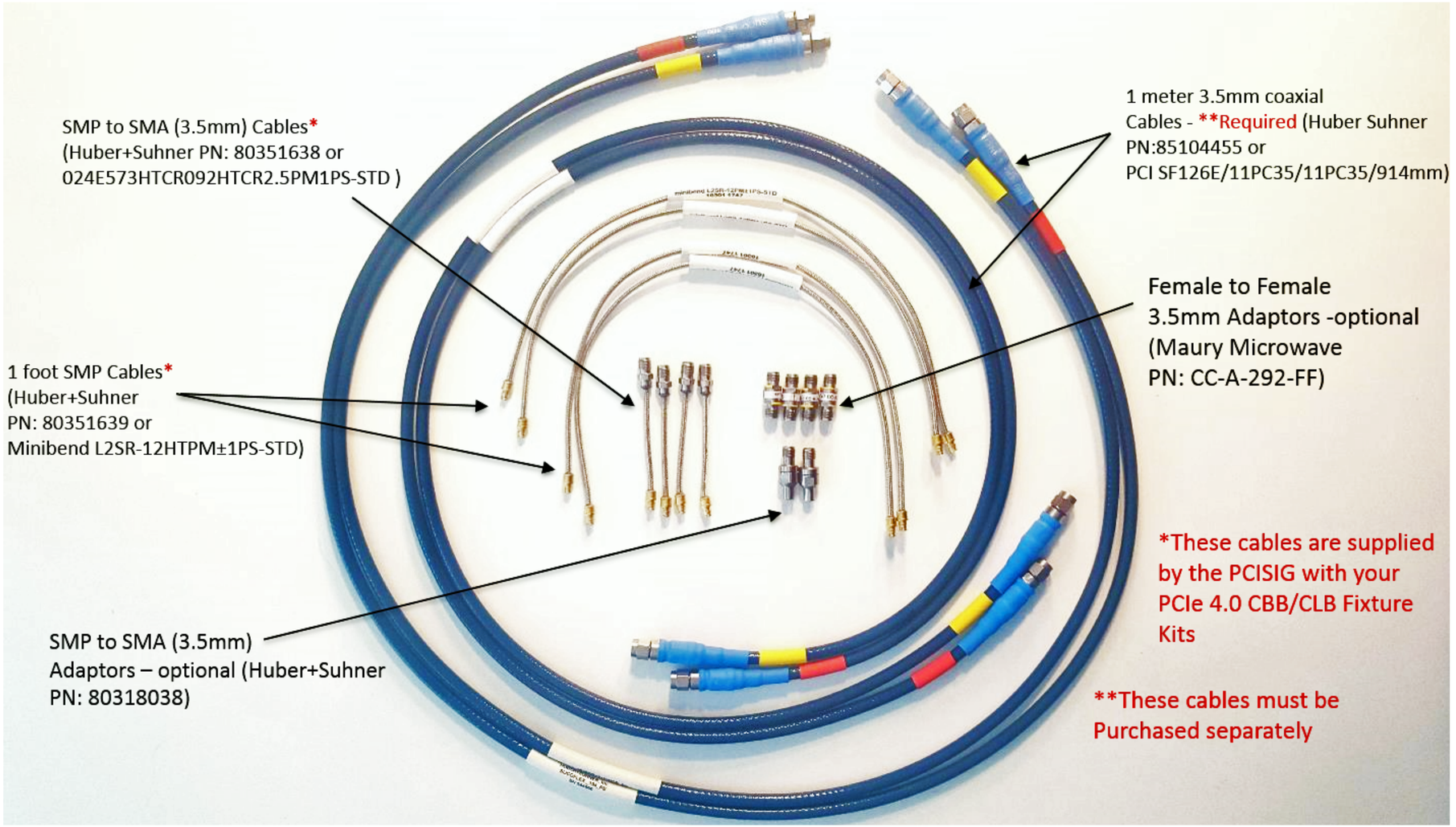




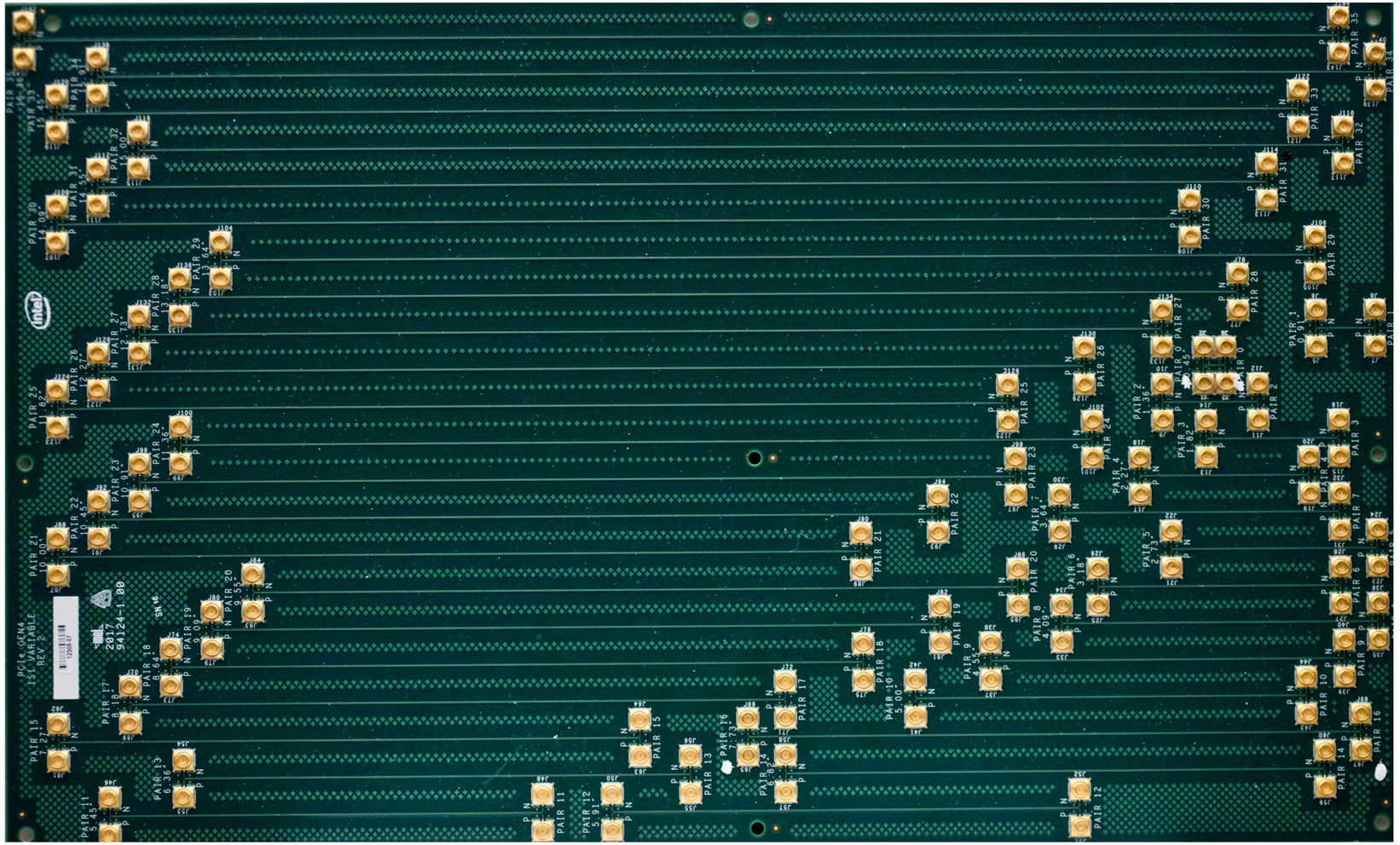




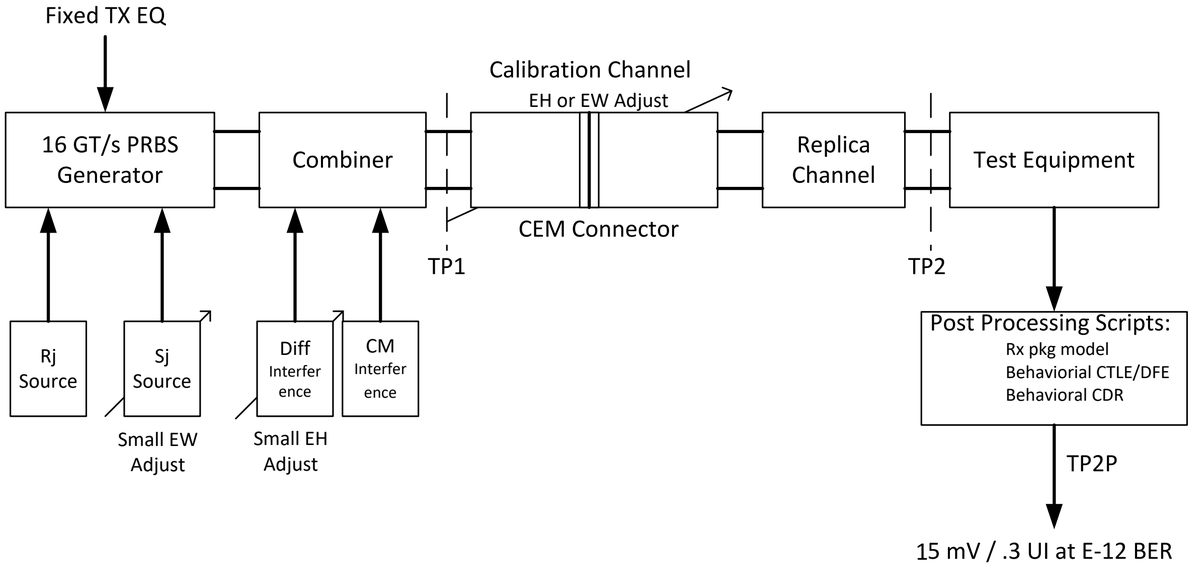
Test Accessories

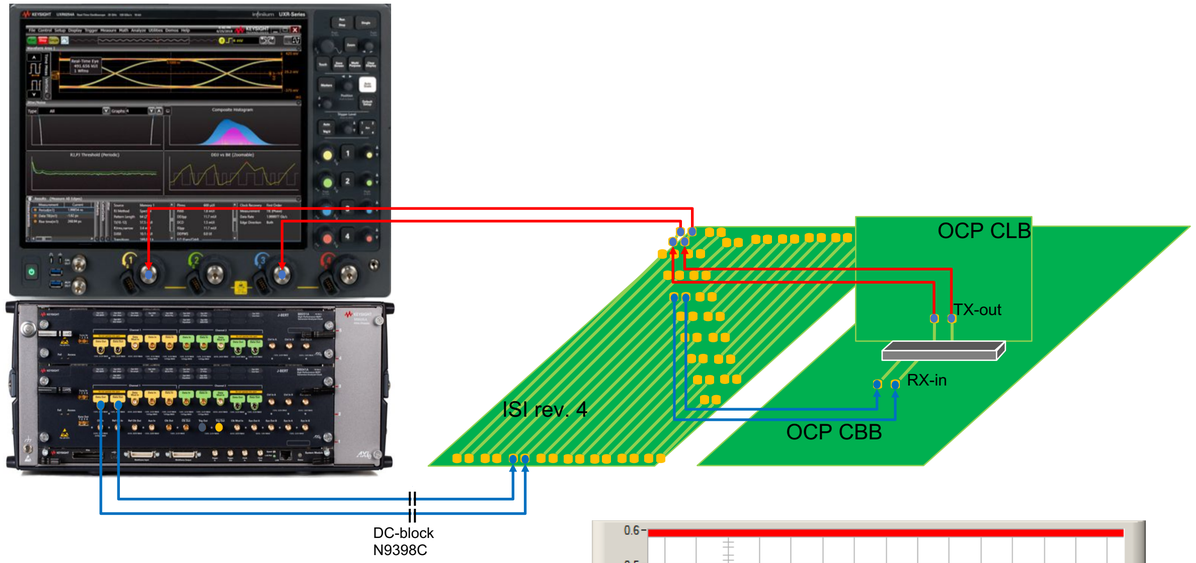


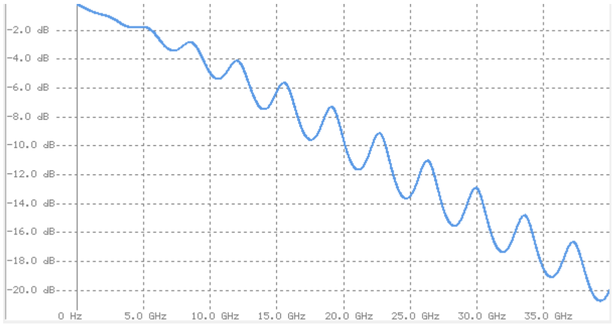
PCISIG ISI Board for 16GT/s Testing



PCIe 4.0 Receiver Testing @16GT/s

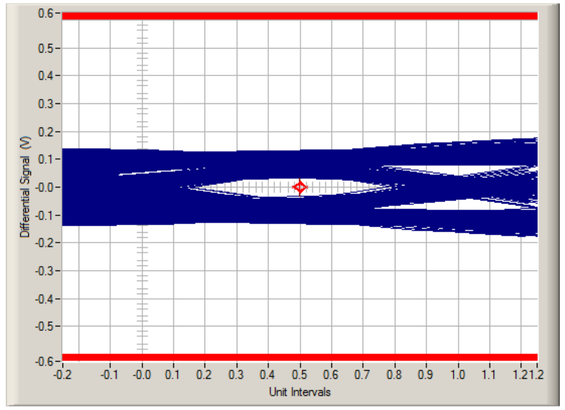






3dB Endpoint Package Model

5dB Endpoint Package Model



PCIe 4.0 RX Calibration Eye

What Next?

- Enablement with PCI SIG Serial Working Group ongoing!
- Fixture Availability:
  - Design Files are located on the wiki:
    - Schematic/Layout Source and production files
    - Users Manual
  - Procurement channel
    - UNH-IOL
      - Test Reports

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Live Demo

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Call to Action

- Join Server Mezzanine working group to contribute

Project Wiki with latest specification : http://www.opencompute.org/wiki/Server/Mezz

Mailing list: http://lists.opencompute.org/mailman/listinfo/opencompute-mezz-card


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