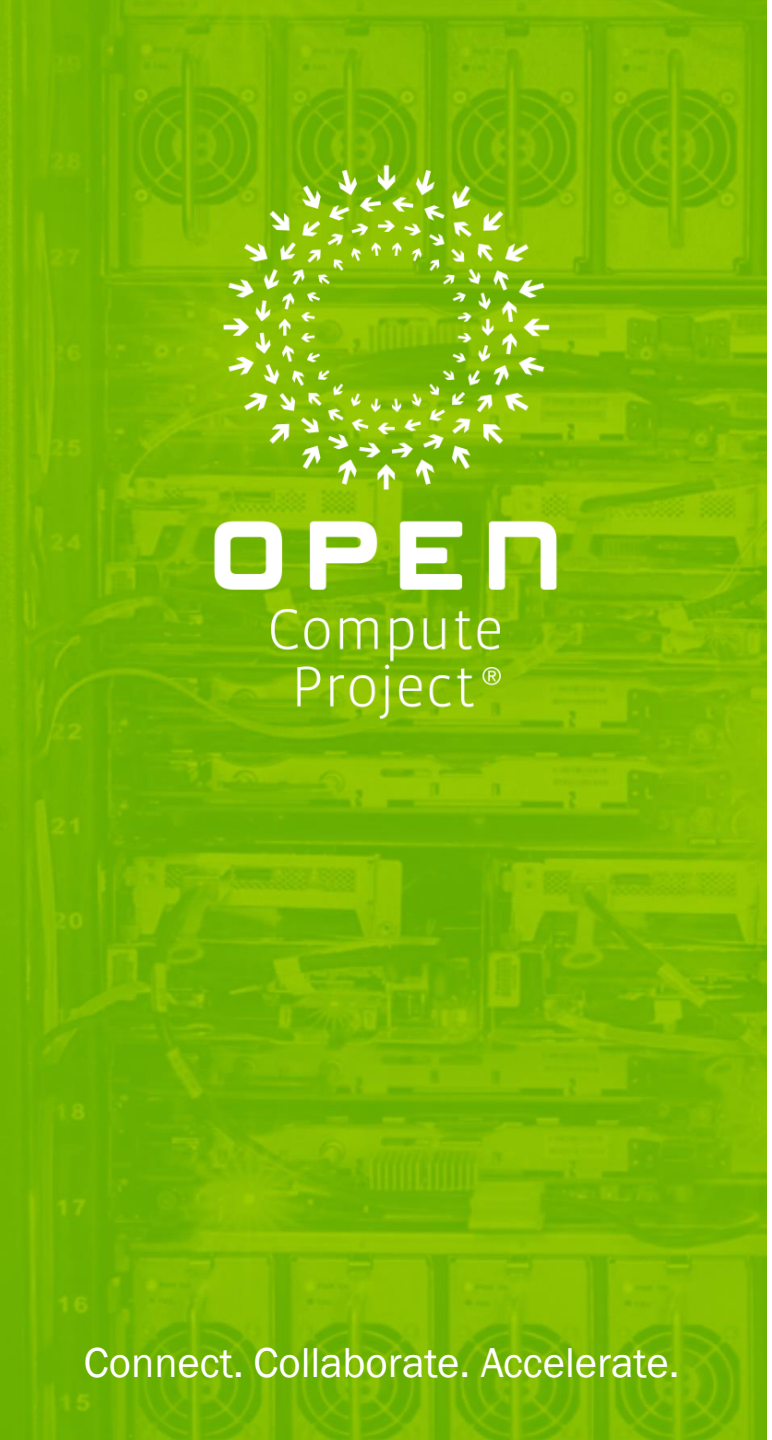
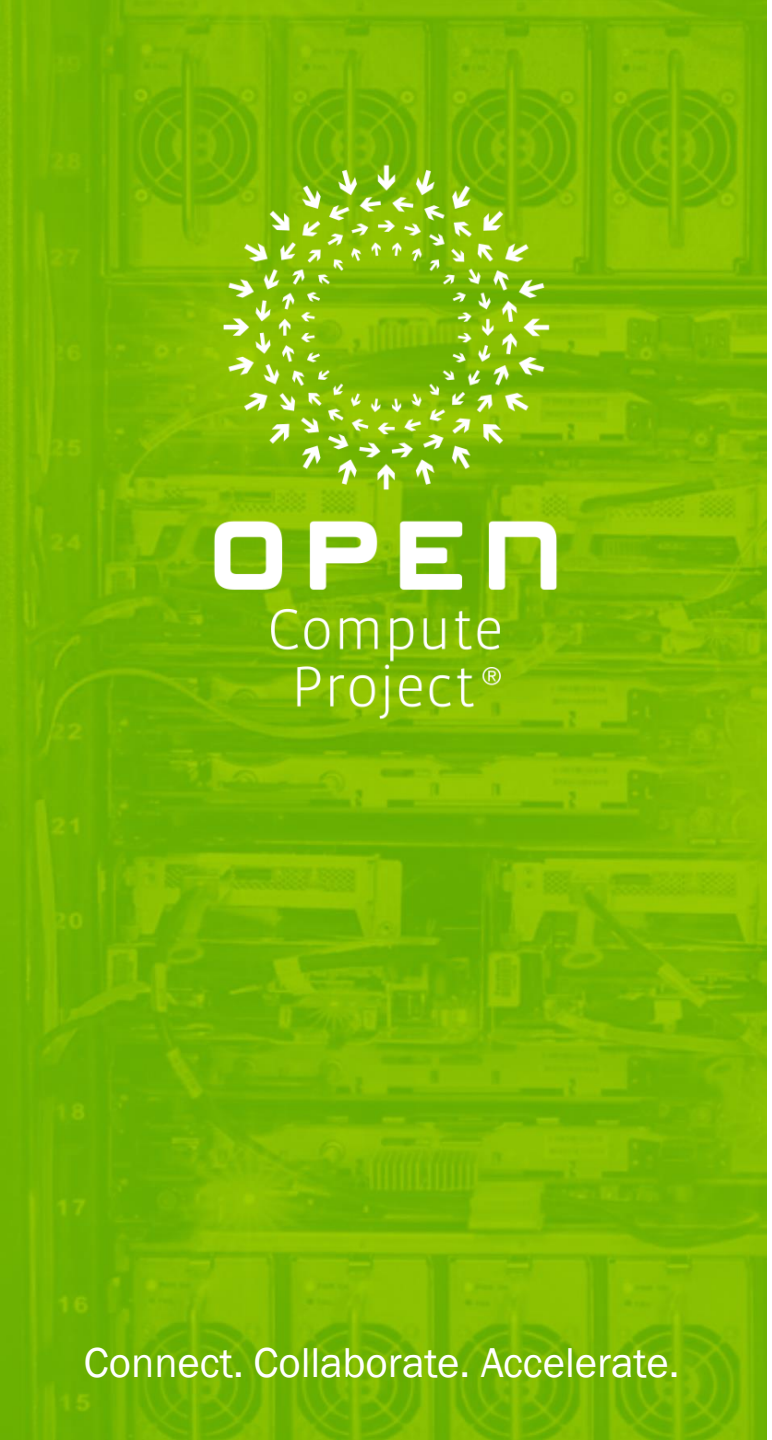


Time Appliances Project

OCP 2022 Tech Talks

TAP 2022 Tech Talks

08:30 am	OCP TAP	**Opening: TAP Vision and Updates**
09:00 am	Kevin Stanton @ Intel	**Time Sync everywhere: Wi-Fi and compute platform**
09:20 am	Dotan Levi @ NVIDIA	**Time Sync in DCs: What's Next?**
09:40 am	Julian St. James @ Meta	**Time Drive M.2**
10:00 am	Anand Ram @ Calnex	**TAP Instrumentation**
10:20 am	Lasse Johnsen @ Timebeat	**Time-as-a-Service**
10:40 am	Dhiman Chowdhury @ Trimble	**GNSS Receiver**
11:00 am	Ullas Kumar @ Rakon	**Choices for 5G DC Sync**
11:20 am	OCP TAP	**Closing: Suggestions and Opportunities**



TAP

What is it all about?

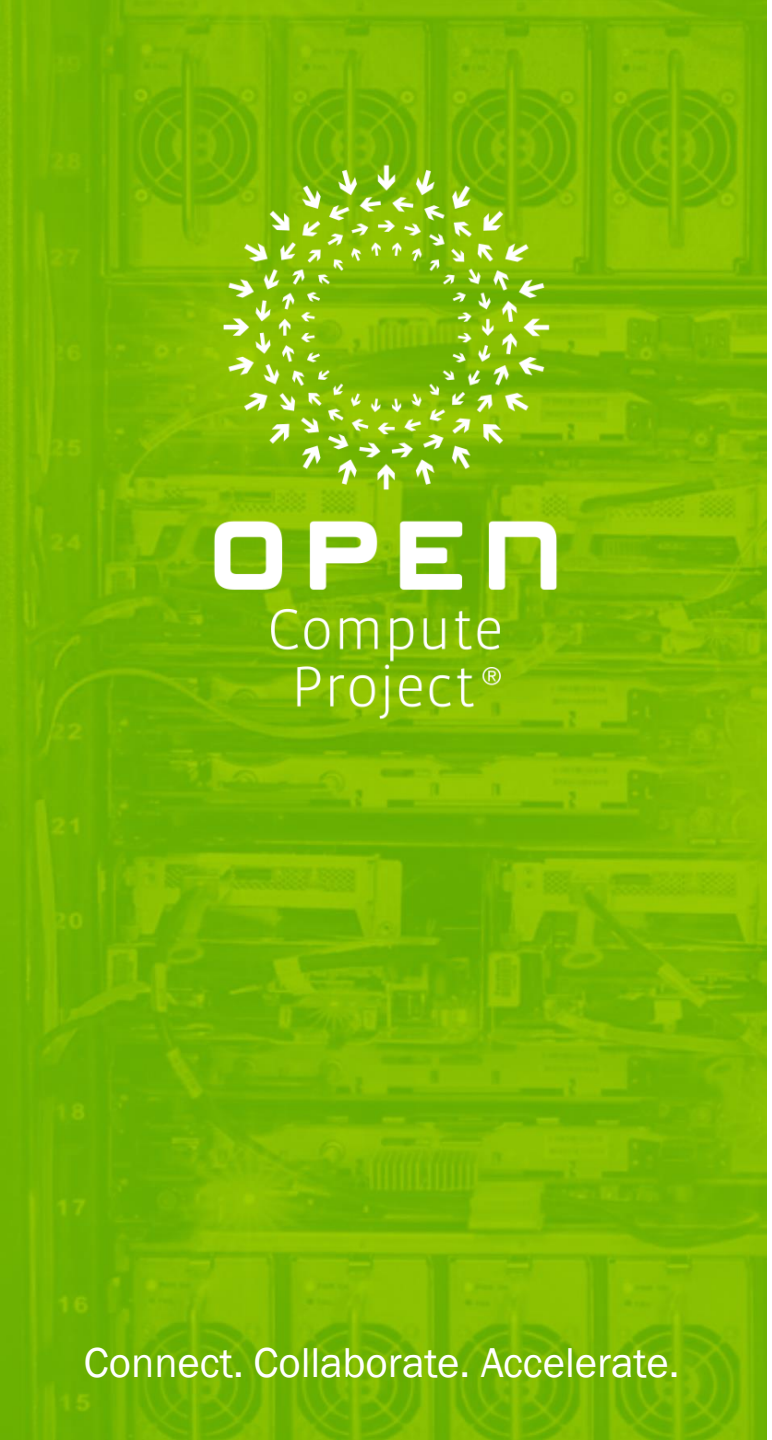
TAP Knowledge Sharing

Some examples:

Clock and Oscillator Statistics and Characterization Techniques	Marc A. Weiss, Ph.D.
Chip Scaled Atomic Clocks	John Kitching, Ph.D.
Practical Use Cases of Sync Clocks	Georgi Chalakov
White Rabbit	Maciej Lipinski, Ph.D.
Precision Time Applications	Dan Biederman
Measuring and Monitoring Options for Time Sync Infrastructures	Heiko Gerstung
Using LEO Satellites for Time Sync	Tyler Reid, Ph.D.
PCIe PTM: Timing in the Last Inch	Christopher Hall
GNSS Timing	Samuli Pietila
Computer Timekeeping and Sync	Kevin Stanton, Ph.D.
Data Center PTP Profile	Michel Ouellette

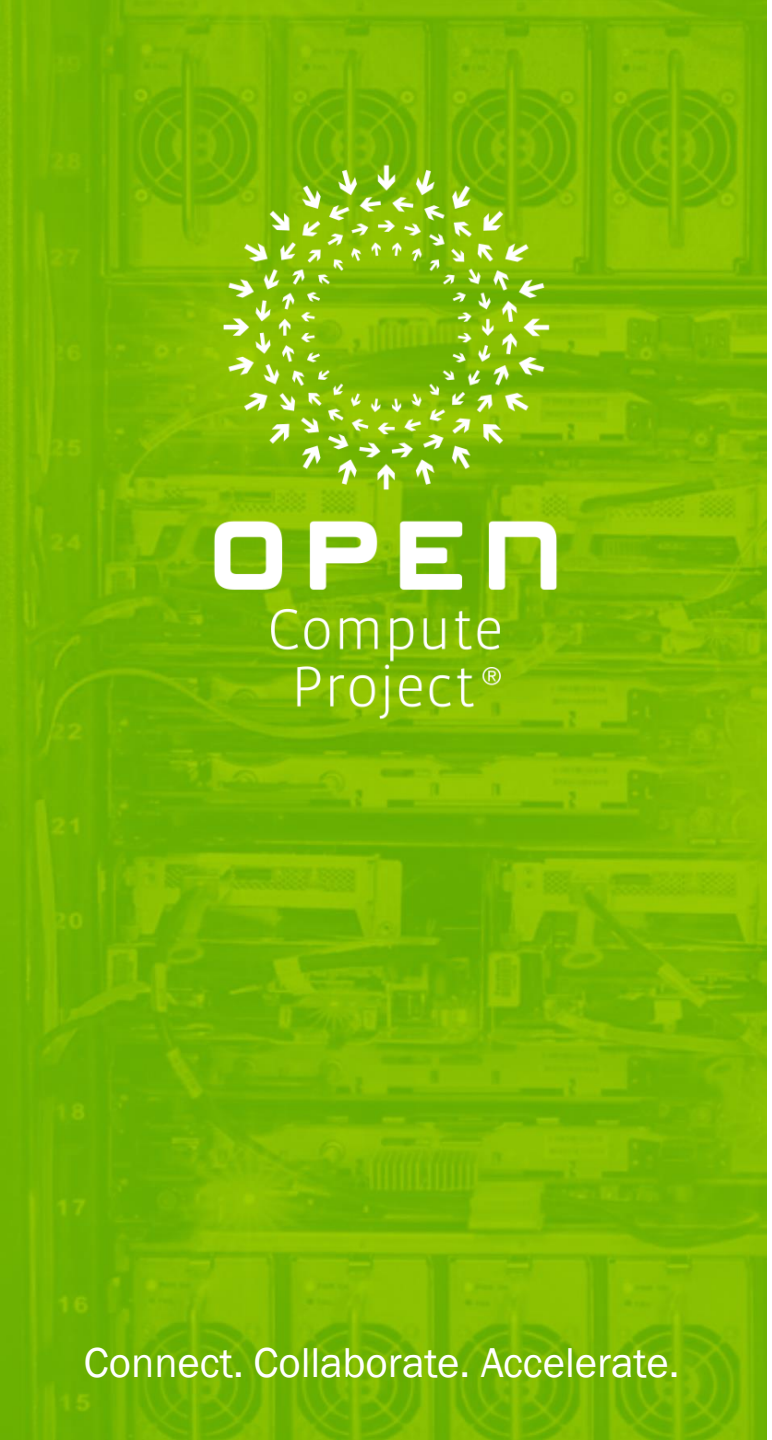
Every other Wednesday | opencompute.org/wiki/Time_Appliances_Project

Connect. Collaborate. Accelerate.



TAP

Open Specifications Reference Designs

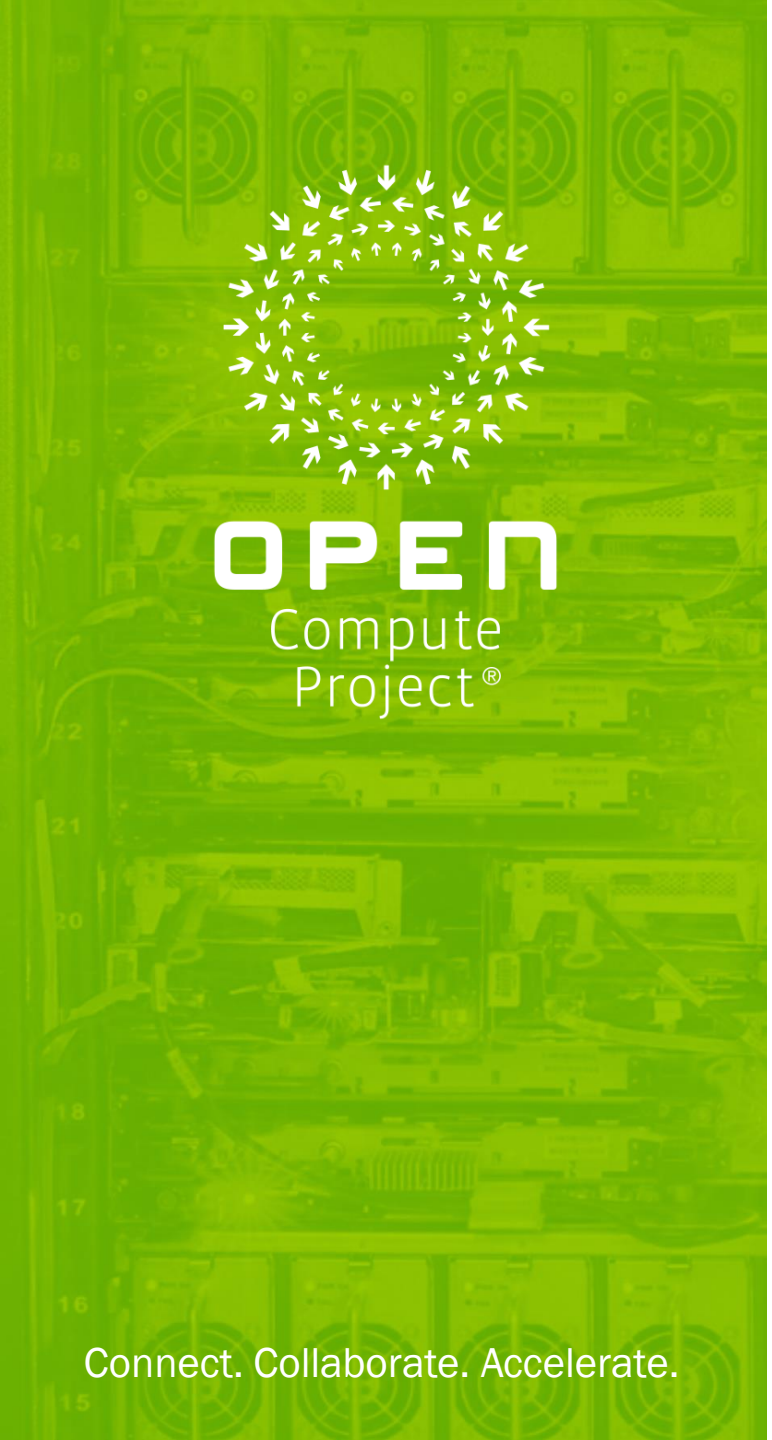


What has been done so far?

1 Open Time Server

2 DC PTP Profile

3 Oscillator Requirements



Oscillator Workstream

Goal: simplify oscillator selection for predictable PTP performance

OCP-TAP Oscillator Classes

- Performance requirements
- Test methodologies

We welcome your contribution
opencompute.org/wiki/Time_Appliances_Project

Oscillator Class G1 - Grandmaster

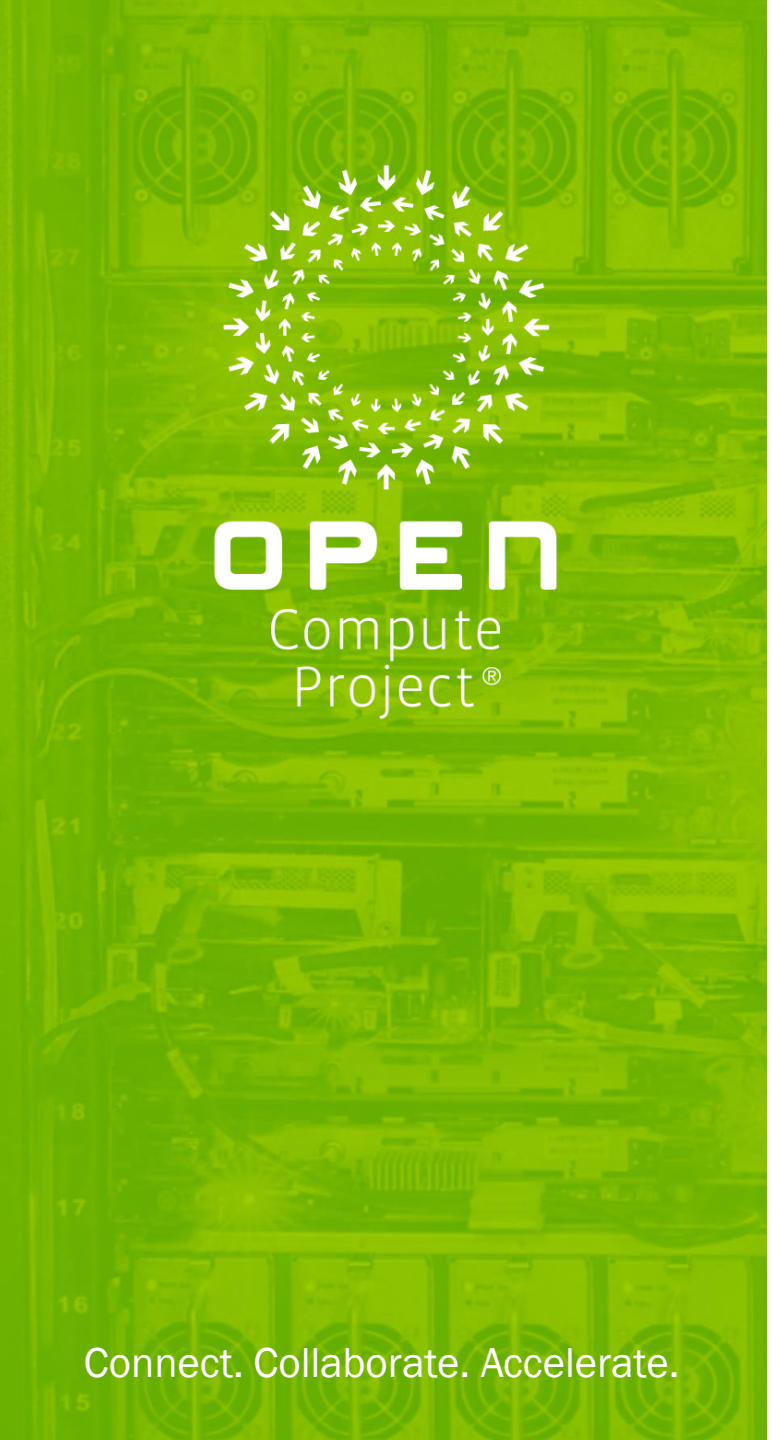
Source
Requirements Document for OCP-TAP Oscillator Classes

https://www.opencompute.org/documents/ocp-tap-oscillator-spec-jan-8-2022-docx-pdf

1 Requirements for Class G1 Oscillator, Normative

Table 1. Standard data-center environment without synchronous Ethernet, see use case GM-A

Parameter	Symbol	Requirement
Ambient temperature (pick 1)	T_a1	-10°C to 70°C
	T_a2	0°C to 45°C
g-sensitivity	F_g	< 0.5 ppb/g
Frequency stability over temperature	F_stab	≤ ±0.5 ppb[1]
Frequency stability over temperature slope	dF/dT	≤ ±7 ppt/°C[2]
Allan deviation, Tau=100s	ADEV	≤9e-12
Daily aging	F_1d	≤ ±0.035 ppb/day[3]
Training time before entering holdover	t_h	< 12 hours
24-hour holdover	F_hold_24h	≤ ±1.4 µs in 24 hr[4]
1 hour holdover	F_hold_1h	≤ ±250 ns in 1 hr[4]
Jitter	J_pp	≤ 1 ns peak-peak[5]
Additional design requirements	ADR	List manufacturer recommendations[6]



What's coming up?

4 Precision Time APIs

5 PTP Servos

6 Instrumentation & Measurement

What's Coming Up for TAP

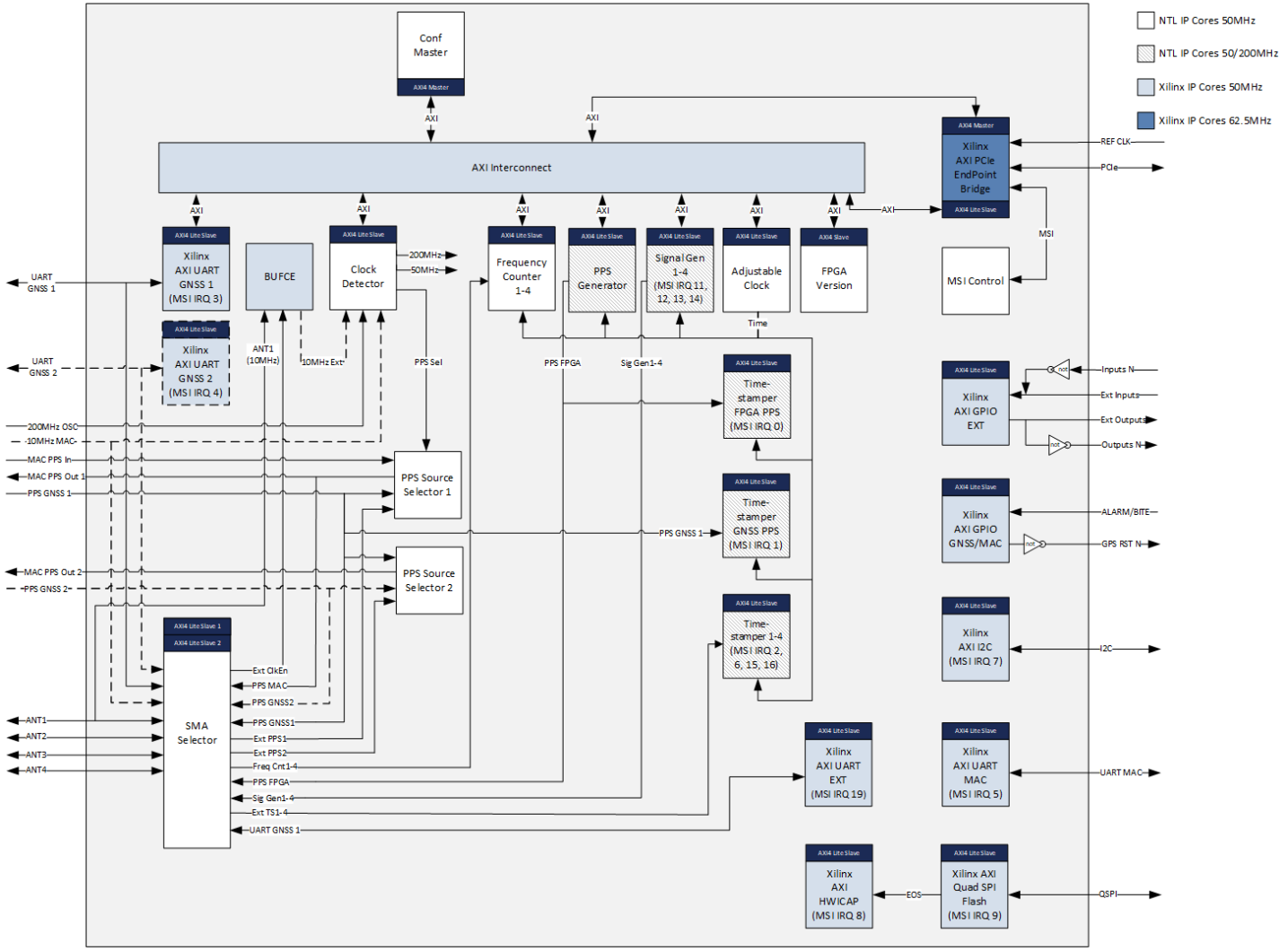
- Security, Integrity and Reliability
- Standardized Sync Database
- Precision Time in VMs
- Time aware Networks
- Time Sync in Existing DC Networks
- Improved Holdover NIC
- Fault Detection and Recovery
- Precision Time over PCIe
- Open GNSS Receiver
- Open MAC
- Precision Time over USB/Wireless
- …

What's Coming Up for TAP

1. Handling the challenges in existing DC networks
   - Noisy neighbor, Pause messages, Asymmetry in Round Trips, Route changes
   - What should be balance between oscillator performance and network fidelity
   - The future of PTP compliant NICs and Switches
2. Further Adaption of Precision Time Sync (Horizontal and Vertical)
   - More DCs, Reaching to End Users
   - Precision Time and Userland
   - Precision Time and Peripherals

Time Card

- An update of the latest open-source effort
- Open sourcing of the time keeping logic commenced



Open-Source Time Card FPGA

1st version of Time Card FPGA *

- ❑ Not an Open-Source design
- ❑ Binaries can be used free of charge

Base-system FPGA **

Open-Source design

- ❑ Open-Source NetTimeLogic IP cores
- ❑ Documentation on GIT for
  - each IP core
  - the overall design
- ❑ *.tcl* scripts for
  - project creation
  - project implementation
  - binaries generation

Extended Base-system FPGA

- ❑ Open-Source design incl. PPS and ToD
- ❑ FPGA can be synchronized to GNSS input, w/o software dependence

* https://github.com/opencomputeproject/Time-Appliance-Project/tree/master/Time-Card/FPGA/Binary

** https://github.com/opencomputeproject/Time-Appliance-Project/tree/master/Time-Card/FPGA/Open-Source

NetTimeLogic GmbH - contact@nettimelogic.com

Time Card Duo

- Dual source and independent GNSS, establishing footprint for evaluation of GNSS solutions
- Placement of MAC towards center of mass
- Improved signal integrity on Input/Output connectors
- Added dual PPS In/Out
- Added PMOD connector for debugging and auxiliary connections