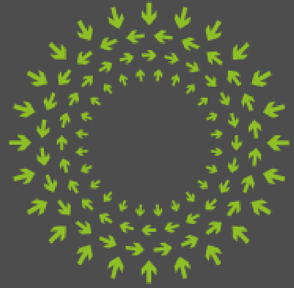
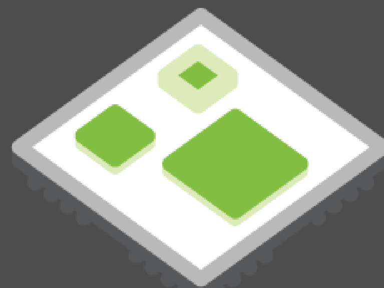


Chiplet Workflow Experience Panel

ODSA Meeting

6/10/2019

Consume. Collaborate. Contribute.



Participants

Alex Wright-Gladstein,
Chief Strategy Officer and Co-Founder
Ayar Labs

Brian Holden
VP of Standards
Kandou Bus

Halil Cirit
High Speed Expert
Facebook

Wolfgang Sauter
Distinguished Engineer, Package Integration
Avera Silicon

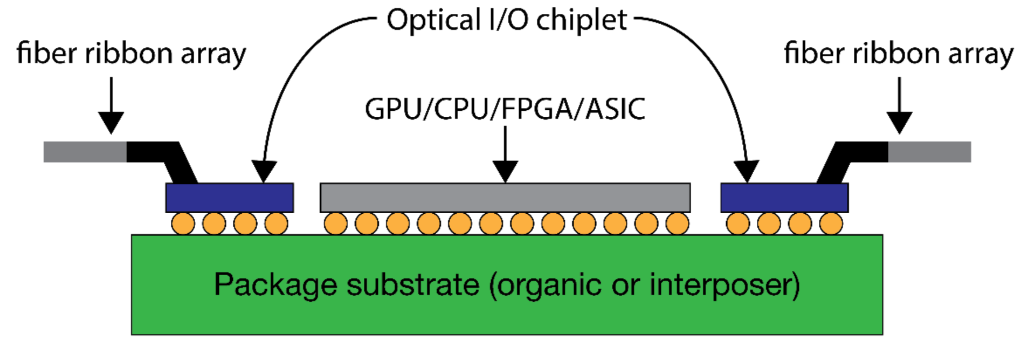
Vamshi Kandalla
Exec VP and GM
Granite River Labs

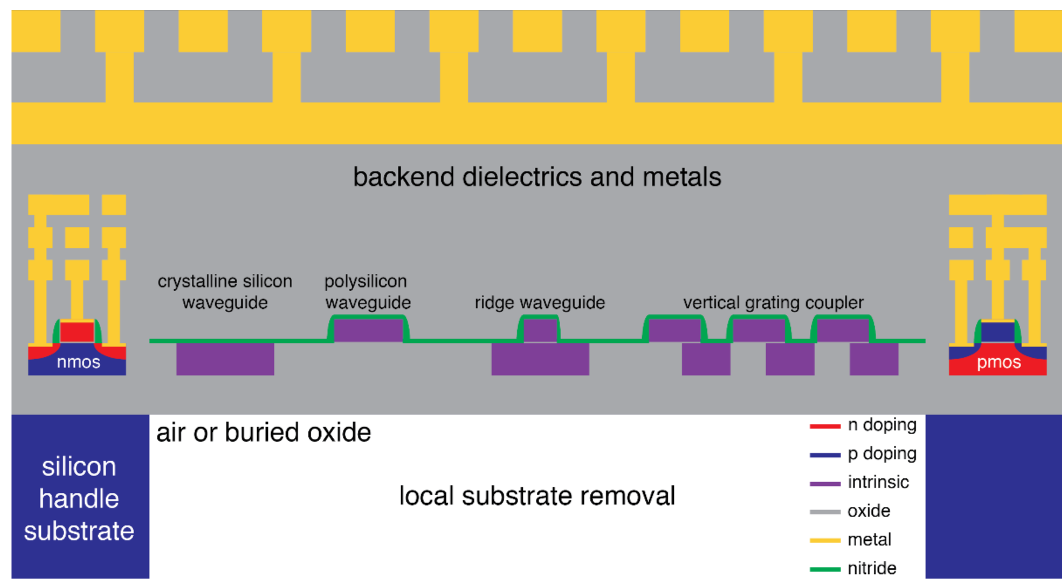
Sam Fuller
Director of Marketing
NXP Semiconductors

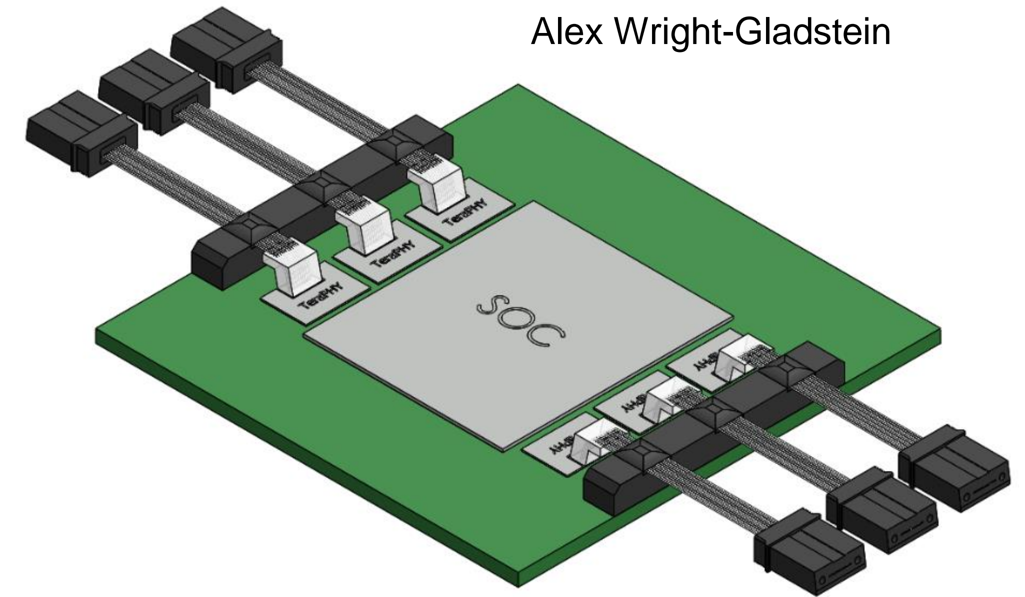
Moderator

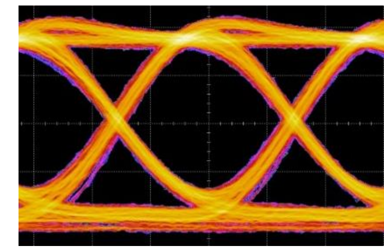
Ayar Labs

Alex Wright-Gladstein

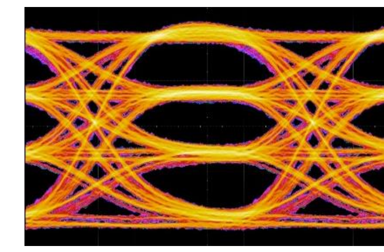




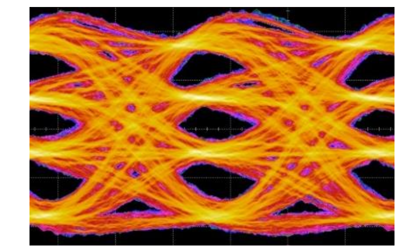




40Gbps NRZ



50Gbps PAM4



100Gbps PAM4

- Monolithic electronic-photonic integration
- GlobalFoundries 45nm process

Technology targets

- Bandwidth density: >500 Gbps/mm^2, >1 Tbps/mm
- Latency: <10 ns
- Power: <5 pJ/b

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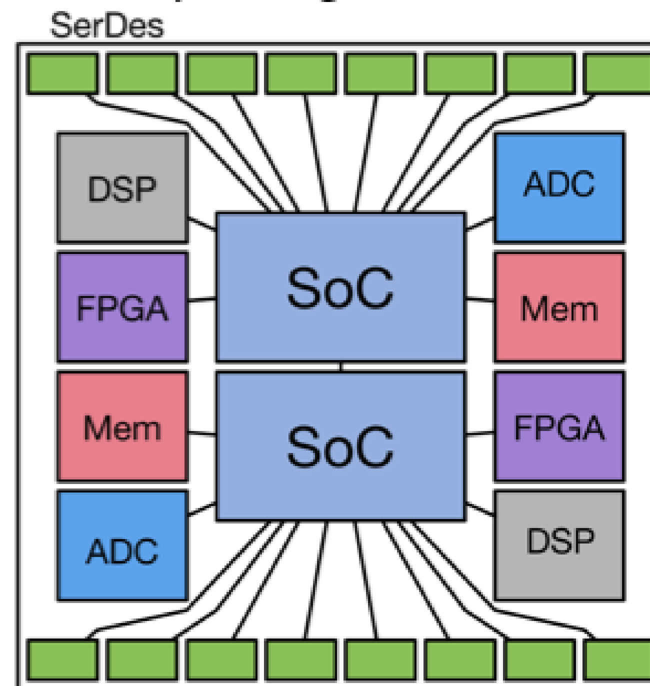
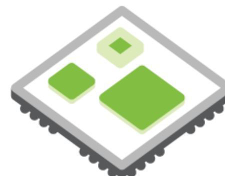
Chiplet Application – I/O Chiplets

- A trend in IC technology is to more away from monolithic chips toward the use of chiplets tied together on an MCM
- Chiplets allow the:
  - Combination of many dies into large packages
  - **Improvement in yield and cost** because of a smaller central die(s) – a major factor
  - Distribution of heat away from a single die
  - Use of the best semiconductor process for each die
  - Enabling of multi-vendor ecosystems
  - **I/O subsystem dies containing SerDes to be placed around the perimeter, creating smaller virtual packages**

Big, 70mm packages are routine

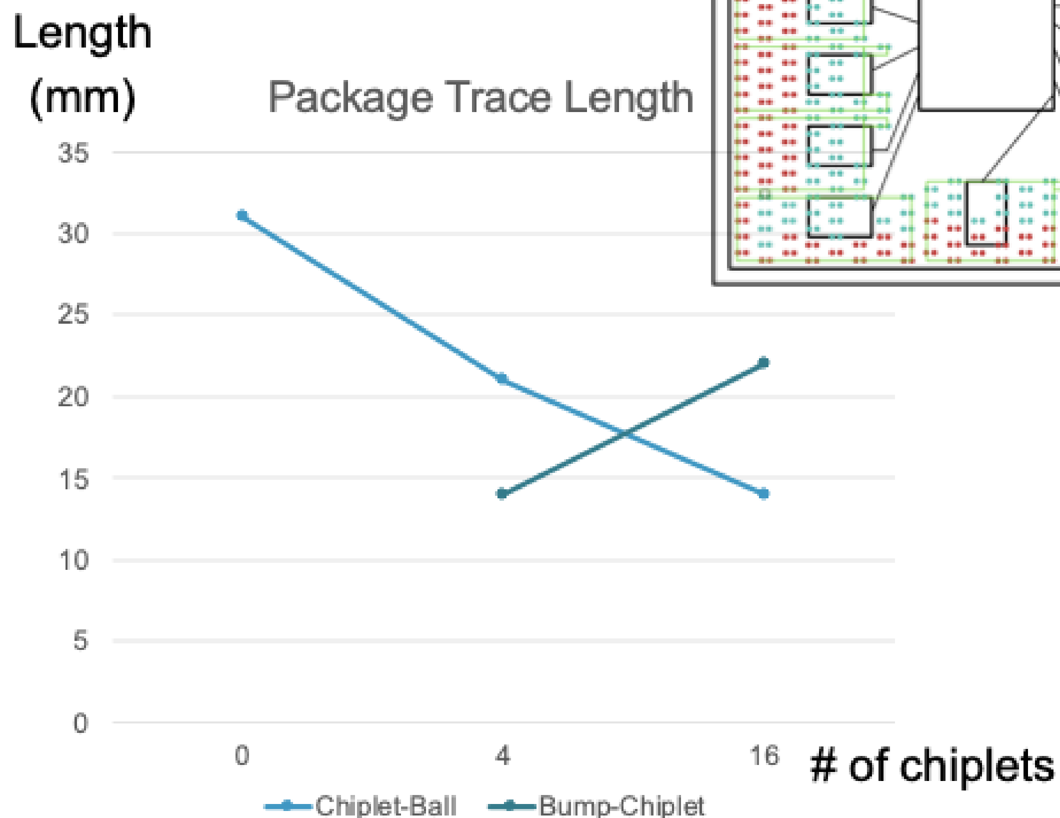


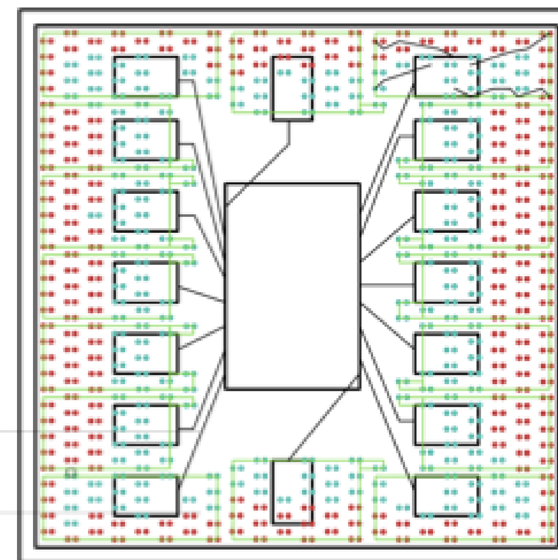
Non-interposer MCMs can easily use 20 or more dies

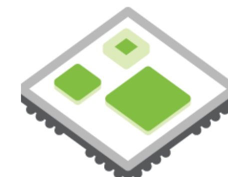


Benefit of using I/O sub-system chiplets with a large Ethernet switch core

- The on-package loss for 100 Gb/s (CEI-112G) serial links is excessive and limits performance
- This graphs the max. electrical package trace length vs. the number of chiplets
  - Chiplet-Ball in blue
    - Switch to chiplet for 0 chiplet case
  - Bump-Chiplet in green
- Major reduction in max length & thus loss when using chiplets
  - ~2 dBs at each end



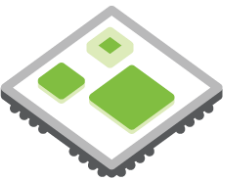




Halil Cirit, Facebook, High Speed Interface

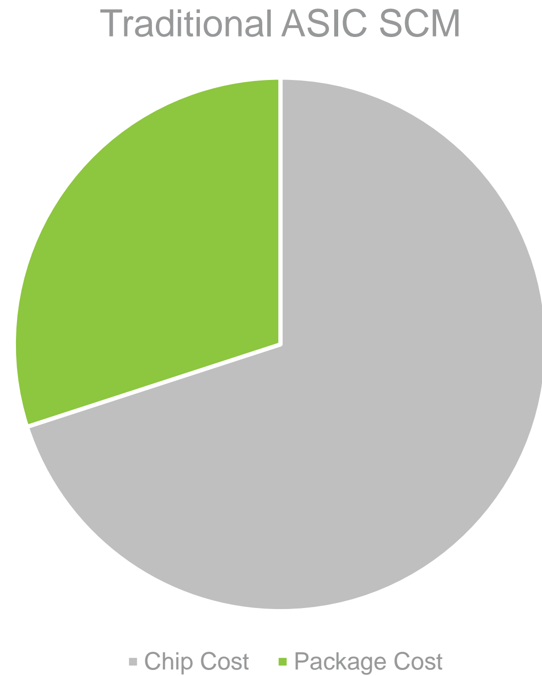
- For different IP’s, the most optimum power/performance/area (PPA) might not be at the same technology node.
  - Chiplets will enable flexibility in selecting IP’s over PPA while not being bounded by the transistor node.
- If less advanced technology, already silicon proven nodes can be utilized, chiplets may reduce the cost and accelerate time to market for design.
  - We would not need to wait for high speed interfaces to be ported to advanced nodes and then be validated, since existing chiplets may already exist.
- Disaggregated devices may improve yield and simplify / relax design requirements
  - Integrating 256 high speed SerDes on a Chip may cause massive area growth which may move design to the non-linear portion of the yield curve
  - If we want to keep the yield high on a single massive device, we may need to tighten the design requirements, this could increase the power and area and dramatically increase the design completion time.

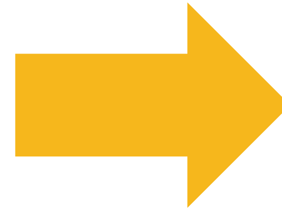
The Tail of the Dog

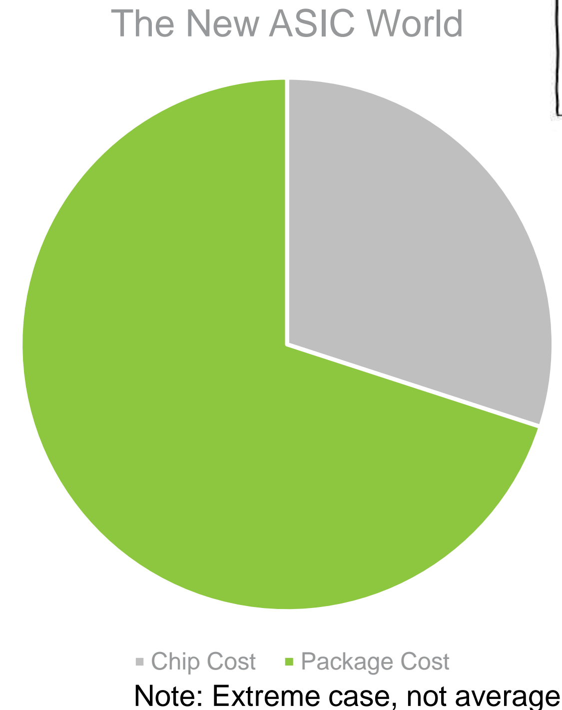


Consume. Collaborate. Contribute.

Cost-Evolution of Chip vs. Package

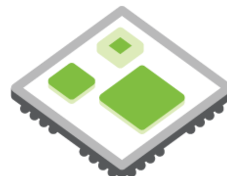




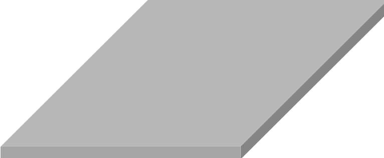


Note: Extreme case, not average

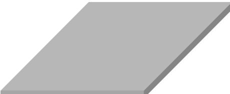
- Complex Package Integration is required for many future (7nm & beyond) ASIC products
  - Driven by multi-component integration (chiplets, memory, etc)
- Product cost of these complex ASIC products is now often driven by package technology
- Interface definition is what drives one package technology (and cost) vs. another



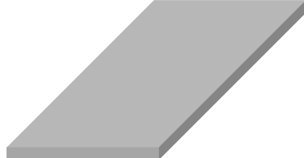
Who wants to own this?



Supplier A: $100

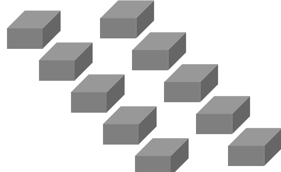


Supplier B: $10



Supplier C: $30

Supplier D: $40



OSAT & Substrate: $120

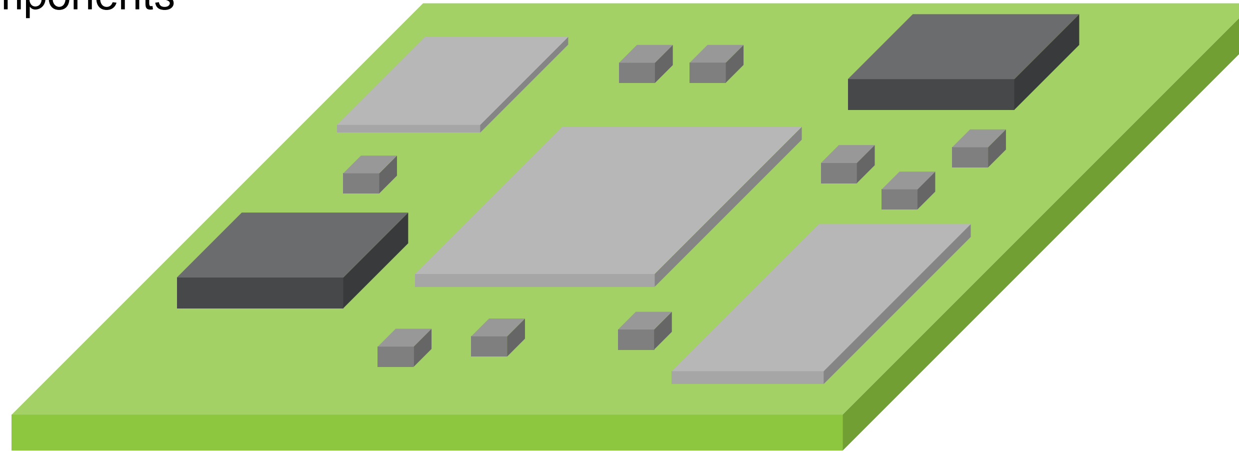
BOM: $300

Who wants to own this?

Suppliers A, B, C & D expect their typical profit margin
➔ But high margin stacking will not work

OSAT does not want to buy all these components

Can the end customer own this?

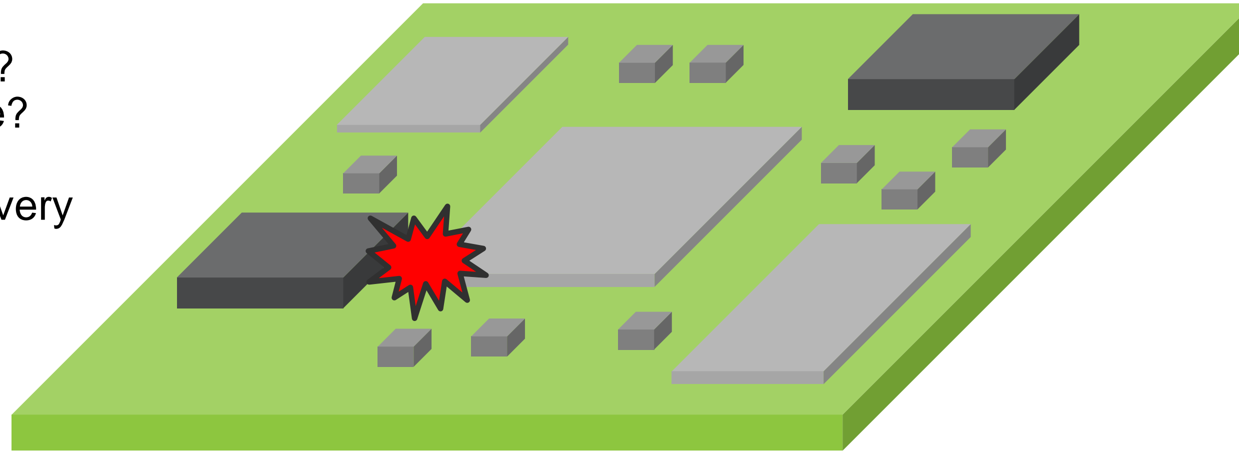


BOM: $300

Who wants to own this?

Fails will occur, but whose fault are they?
Supplier A, Supplier B, OSAT? Laminate?

➔ Complex fault isolation and cost recovery



BOM: $300

Form Factor / Qualification / Sourcing / …

- Most “same” components are not actually the “same”
  - E.g.: standard memories today are slightly different in x, y, z
- Memory layout needs to “envelope” all possible components
  - Hard to do, and even harder to optimize
- Assembly results will differ based on materials, surface, cleanliness, etc.
- Reliability results may differ based on selected component

- ➔ all this will drive complexity in qualification, sourcing, yield, and ownership

THANK YOU

Questions you'd like me to ask

- What surprised you as easier than expected?
- What surprised you as harder than expected?
- What do you think is the biggest barrier to chiplet adoption?
- Can you share an example of:
  - Practical workflow experience with chiplets
  - Key deltas from "standard" workflows
- How do we best drive the needed changes - existing players, new vendors?
- How does Chiplet workflow change the relationship between Fab, OSATs, and Tool/IP vendors?