Wide Parallel LED-Based Optical Links for Chip-to-Chip Applications

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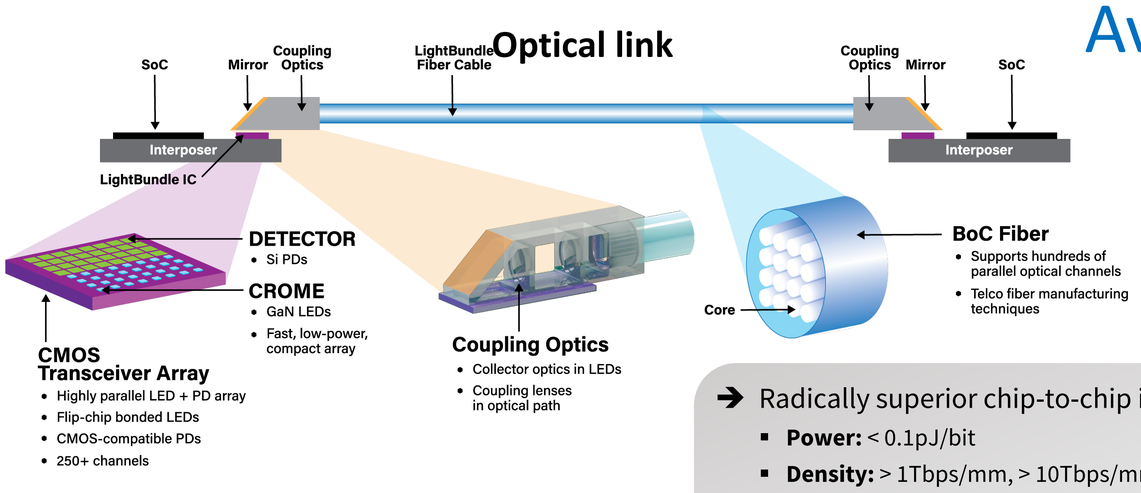
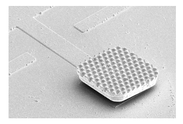


➔ Radically superior chip-to-chip interconnects
- **Power:** < 0.1pJ/bit
- **Density:** > 1Tbps/mm, > 10Tbps/mm^2

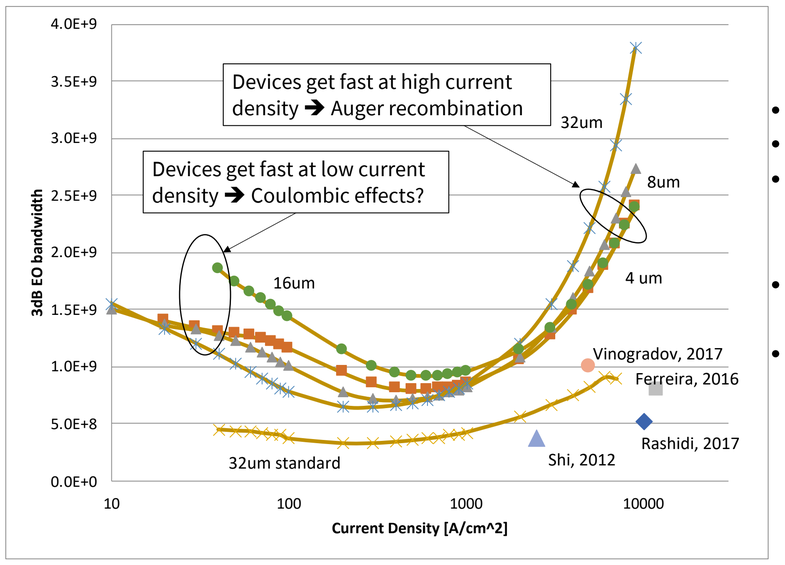
➔ Highly differentiated and defensible IP

➔ Leverages massive IC & display mfg ecosystems for fast volume ramp and low cost

Key Points



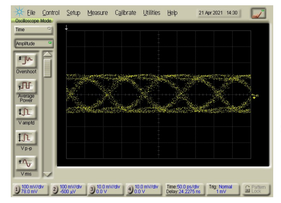
- **CROME^{TM}** (Cavity-Reinforced Optical Micro-Emitter): Optimized GaN LED enables 10Gbps/lane using blue light (λ ~ 430nm)
- **Si PDs:** Great in the blue: very short absorption length enables very low C CMOS-compatible detectors
- **BoC^{TM}** (Bunch of Cores) **fiber**: Hundreds of multimode cores (~50um core diameter) in ~1mm diameter fiber
- **Highly parallel links:** Typical is 256 lanes x 4Gbps/lane = 1Tbps
- **Relaxed packaging alignment:** Tolerances ~ +/-5um support passive alignment



Transmitters using CROMEs

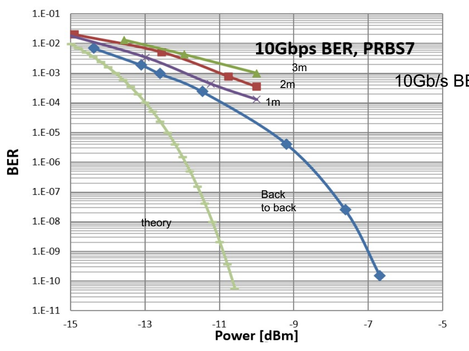
- World's fastest LEDs!
- Data rates up to 10Gb/s so far (with 6dB equalization)
- Devices are fast at high current density (J > 1kA/cm^2) due to increased non-radiative recombination (e.g. Auger)
- In high-quality epi, also can be fast in low current density (< 100A/cm^2) regime
- Can trade off efficiency and modulation BW
  - Lighting LEDs can be 90% efficient so lots of efficiency to give …

Link Performance

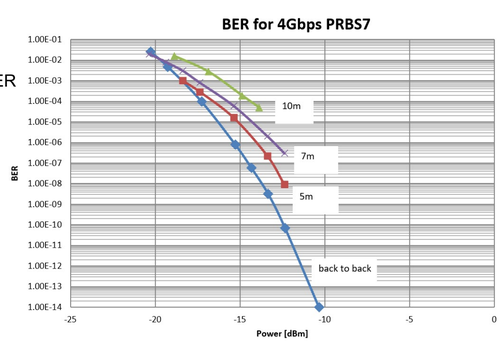


10Gb/s eye (~6dB equalization)

- No error floors down to BER < 1e-15
- Dispersion
  - Modal and chromatic dispersion contributions
  - 10Gb/s, 3 meters: 3dB penalty
  - 4Gb/s, 10 meters: 3dB penalty

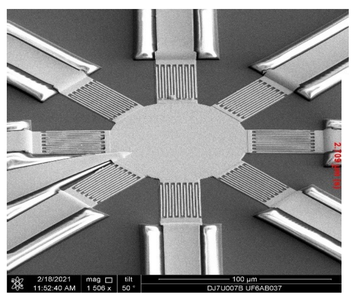


10Gb/s BER



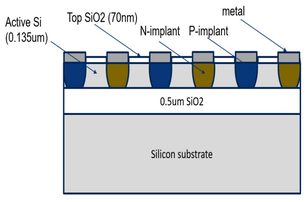
Excellent Blue PDs in Silicon

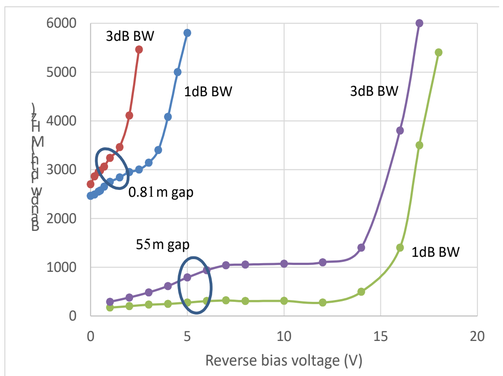
- Blue light is absorbed very fast in silicon – allows large, low capacitance detectors
- Interdigitated structure can be made CMOS-compatible



8-element PD array using interdigitated p-i-n structure

CMOS-compatible PD structure

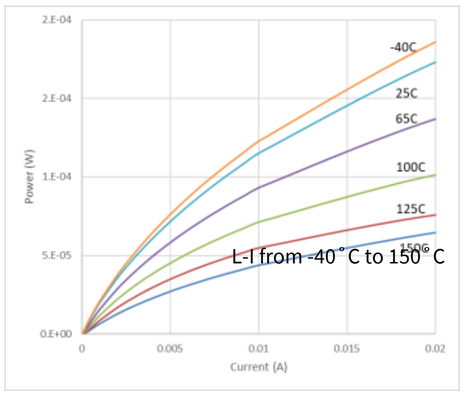


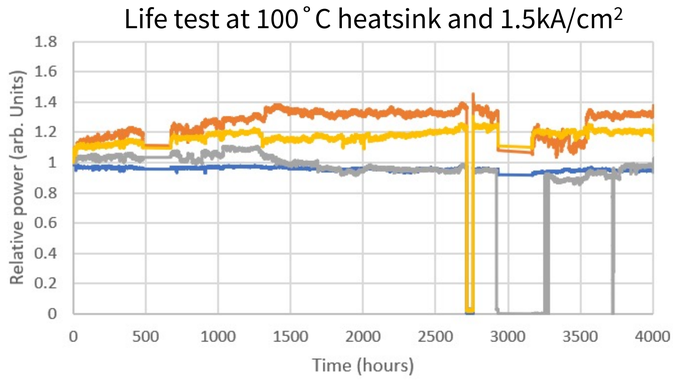


S21 detector measurements
- Speed limited by 6GHz instrument
- Estimate C < 10fF for 30µm diameter

Temperature Performance and Initial Reliability

- Much less sensitive to temperature than lasers
- Initial life test of handful of devices looks OK





Multicore "Bunch of Cores" Fiber

- Based on "imaging" fiber with thousands of cores ➔ each optical lane can be carried in multiple cores
- Fiber optimized for LightBundle links needs only a few hundred cores ➔ 1 core per lane

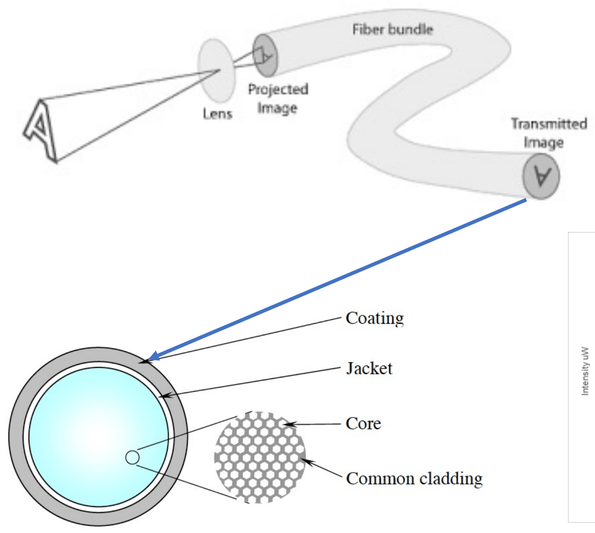
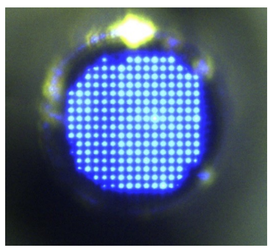
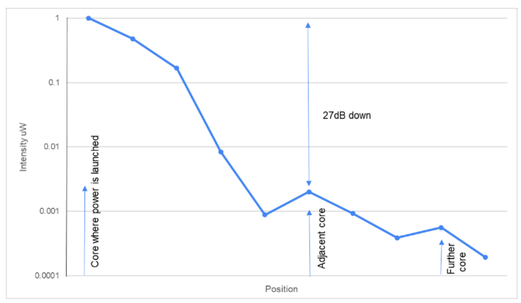


Image of output facet of the fiber



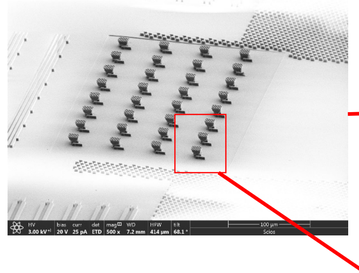
Measured crosstalk between adjacent cores < -27dB



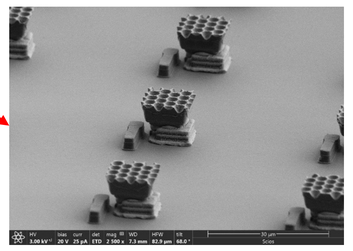
ASIC integration

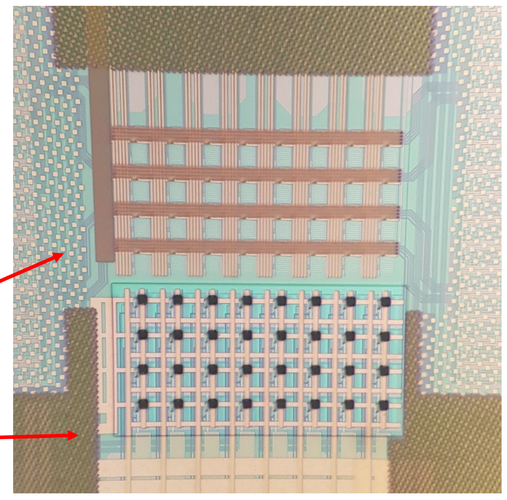
- Testing ASIC with various arrays up to 128 Tx + 128 Rx x 2Gbps (130nm CMOS)
- Arrays of CROMEs transferred to ASIC using laser lift-off
- Developing higher performance product ASIC for in 16nm CMOS
- Working with supply chain partners on volume manufacturing of CROMEs, BoC fiber, packaging

32 element CROME array on CMOS



32 element PD array





Lifted-off devices on ASIC