CHIPLET CREATION PLATFORM - ACCELERATED DESIGN EXECUTION AND CROSS COMPLIANCE

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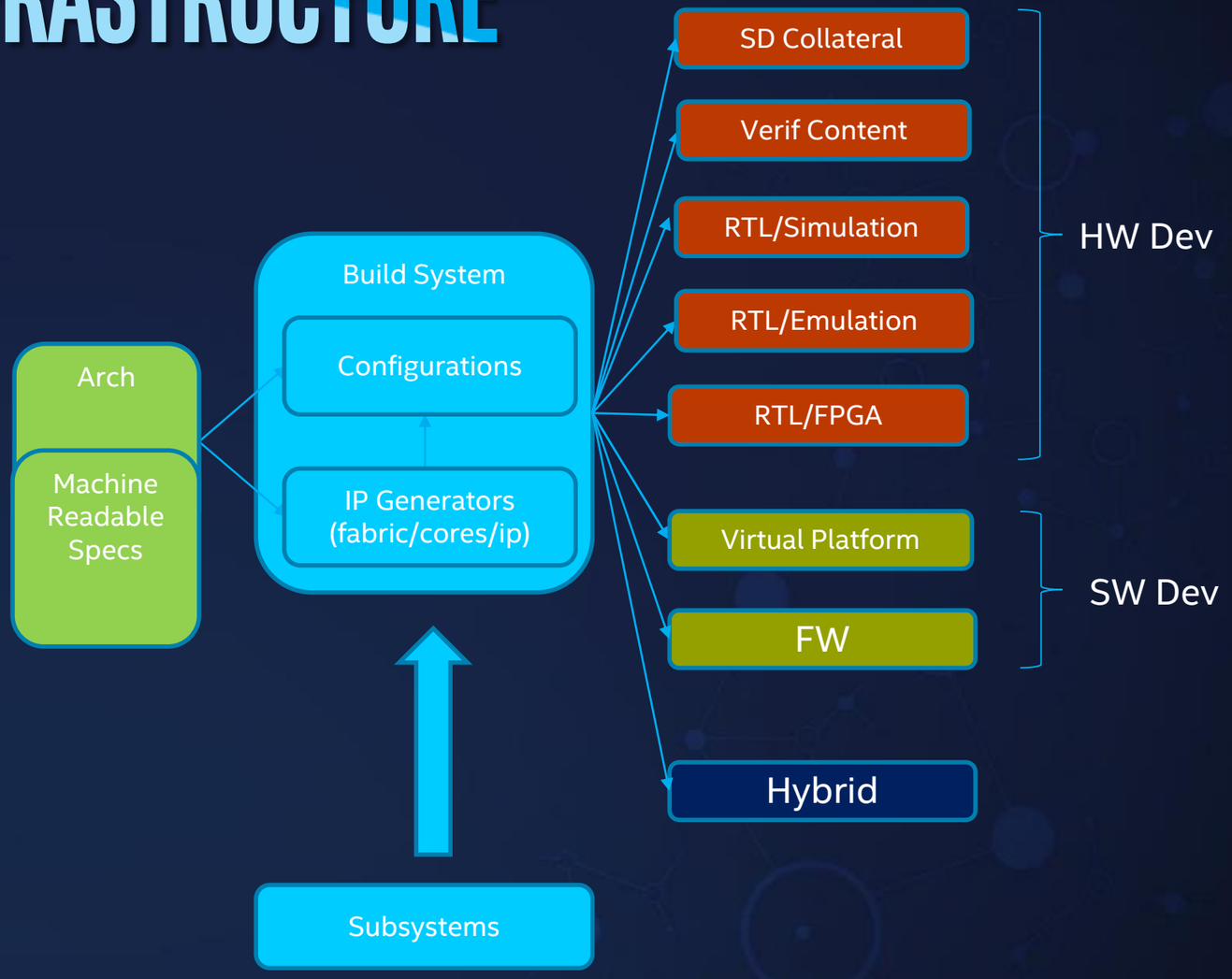
GOALS

- Accelerated Creation
- Abstract away/package I/O (chiplet2chiplet) interface
- Enable “reasoning” about how to integrate value add ip “subsystems” into a standard “chassis” that include the C2C
- Chiplet packaging and IO treated as constraints
- Easy Composability and Validation of chiplet-based design
- Not limited to just design – needed for all domains required to build chiplet – front end + back end HW design, SW sim environment, ported Sys FW/SW

… DELIVER DELIGHT TO CUSTOMER

DESIGN INFRASTRUCTURE

- Architecture + Machine readable Specs Input to the system
- Collection of Subsystems
  - N “Chassis” Subsystems are always present
  - IP Subsystem(s)
- Enables Consistent HW and SW Model and Collateral Output
- Hybrid Capabilities enable cross-product mix-match of VP/EMU/FPGA



WHAT'S A SUBSYSTEM

- A Subsystem abstracts the logical components that are required for an architectural function and packages them for a correct and complete integration for all aspects required to build/design the final SoC
  - Example: Controller IP + PHY, Clocking, Primary Fabric
- All of the pieces needed for all aspects of integration are included in the Subsystem Package:
  - Example: Register Descriptions; Compilation Instructions; Power Intent (UPF); Syn collateral
- C2C interface becomes a Subsystem "on the shelf". Standardizes on interface to enabled value-add IP to concentrate on its value-add

VIRTUAL PLATFORM

SW Accurate SystemC IP Models

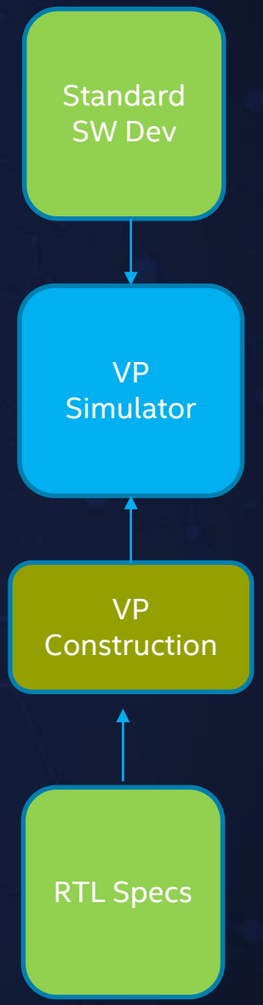
Interconnect and Memory Map Model

Core Instruction Set Sim

Virtual Platform

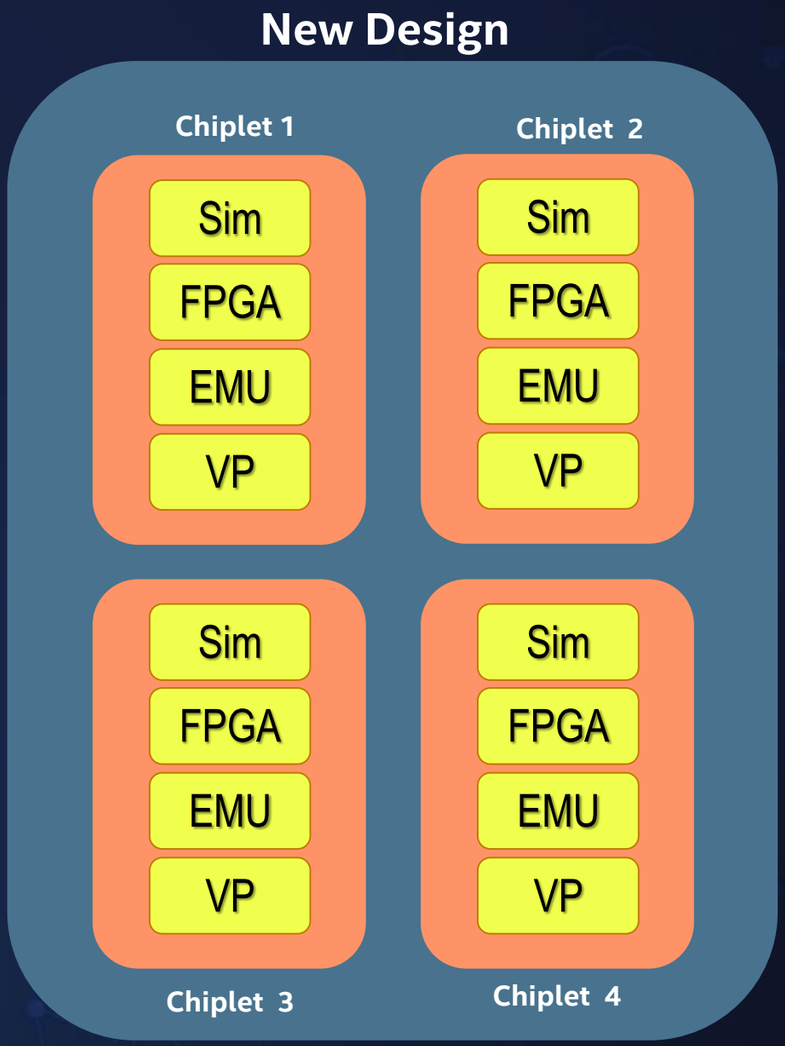
CONSISTENT VIRTUAL PLATFORM (VP)

- Automatically assembled to ensure RTL and VP are consistent by construction
  - VP Model and System FW assembled/generated by system
- Provides same debug environment as final FPGA/SOC ensuring consistency of SW dev/debug
- Deliverable to customers for integration testing and early development of SW/FW
- Easy path to Hybrid (VP +EMU/FPGA) Sim environments



CHIPLET COMPOSABILITY

- New Design is composed of new and existing Chiplets
- Design Infrastructure gives ability to design and verify new Chiplet
- Also need to design/verify the composed design before we spend $$$ and time
  - New VP + existing VPs enable early SW dev and lost cost dev vehicle
  - New VP + existing EMU/FPGA in hybrid
  - New FPGA/EMU + existing FPGA/EMU



SUMMARY & CONCLUSION

CONSISTENT VP – ENABLE EARLY MODELING

CROSS COMPLIANCE – ROBUST AND TRUSTED VALIDATION

PROVEN SUCCESS OF CHASSIS INTEGRATION AND EXECUTION

STANDARD TFM – REDUCED TTM -> CUSTOMER SUCCESS

CALL TO ACTION -> ADOPTION OF STANDARDS – KEY TO SCALE AND SUCCESS