



January 24 - 26, 2023
DoubleTree by Hilton San Jose
ChipletSummit.com

OCP – ODSA Project

Open Platform Development for BoW PHY Interoperability Testing

Jayaprakash Balachandran

Cisco inc





January 24 - 26, 2023
DoubleTree by Hilton San Jose
ChipletSummit.com

Acknowledgements

Namhoon Kim , Google

Dr. Elad Alon, Blue Cheetah Analog

Anand Dixit , Blue Cheetah Analog

Wen-sin Liew, dMatrix

Irene Quek, dMatrix

Prof Shalab Gupta, IIT Bombay, India

Geedimatla Shekar, IIT Bombay, India

Ishan Mishra, IIT Bombay, India

Bapi Vinnakota, OCP

Mike Bartley, Tessolve

Janga Venkata Naresh, Tessolve

Praveen Kumar, Tessolve

Meenaskhi Ramanathan, Tessolve

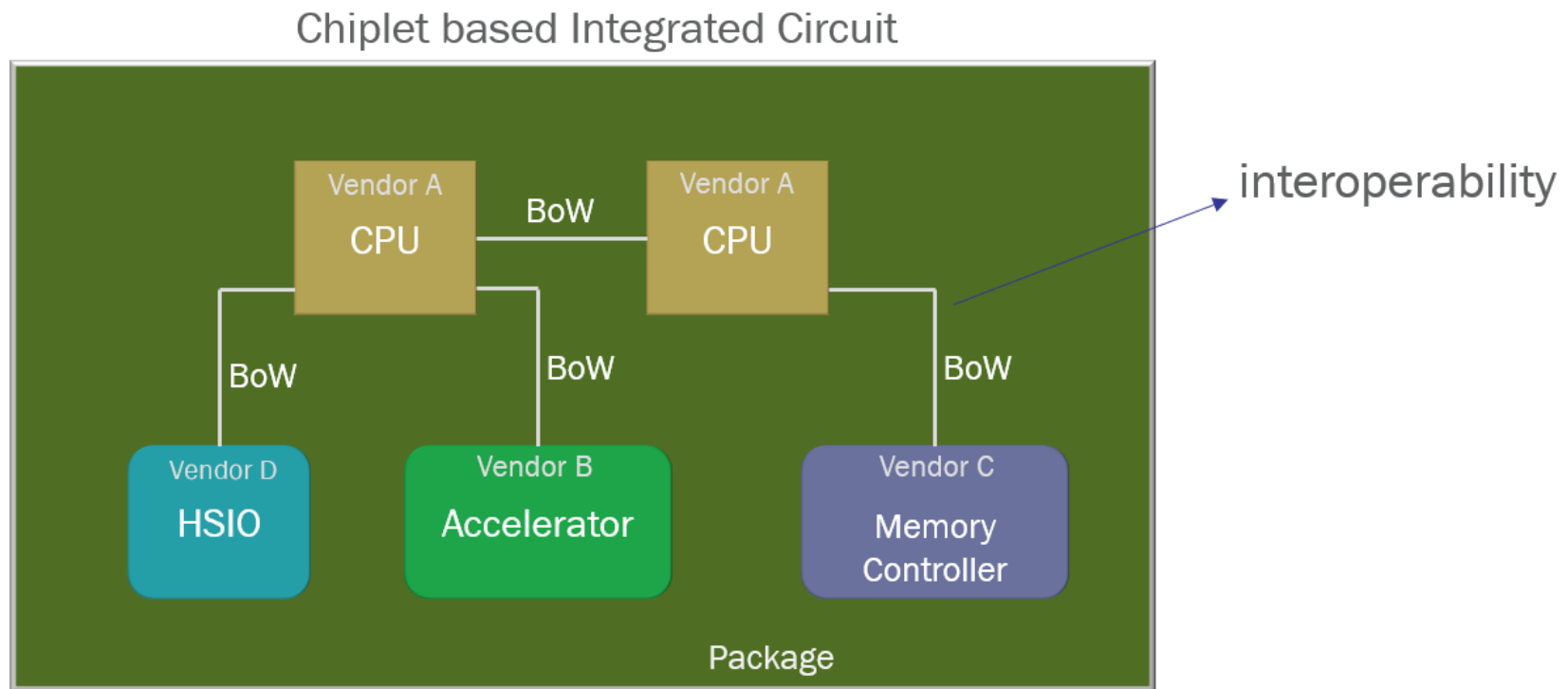
Prasad Swaminathan, JCET

Dr. Ouyang Eric, JCET

Dharmesh Jani, Meta

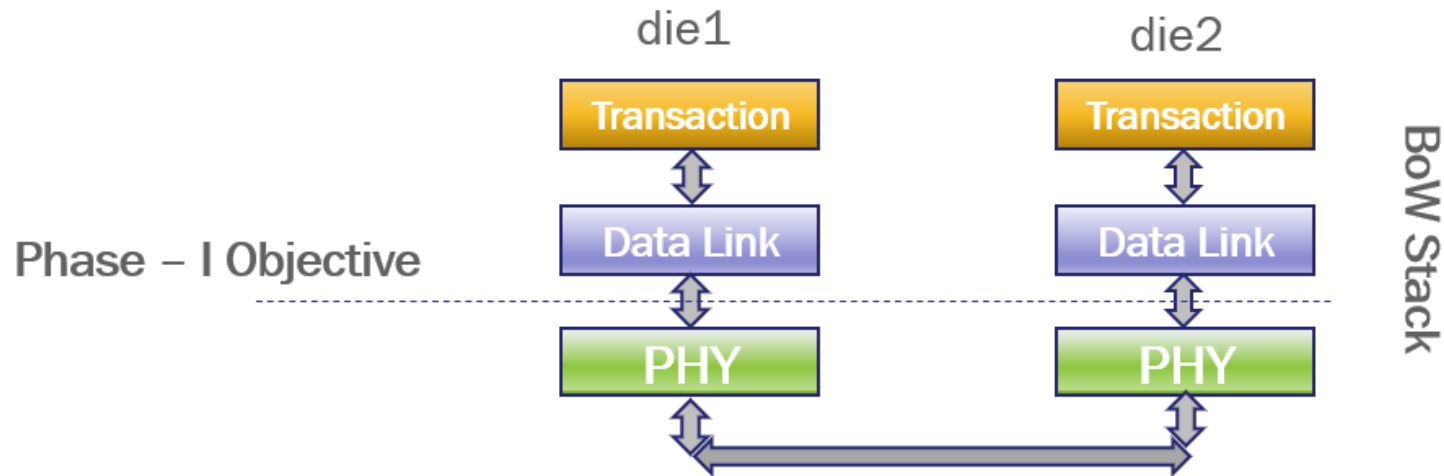


Interoperability Key for Chiplet based IC Designs



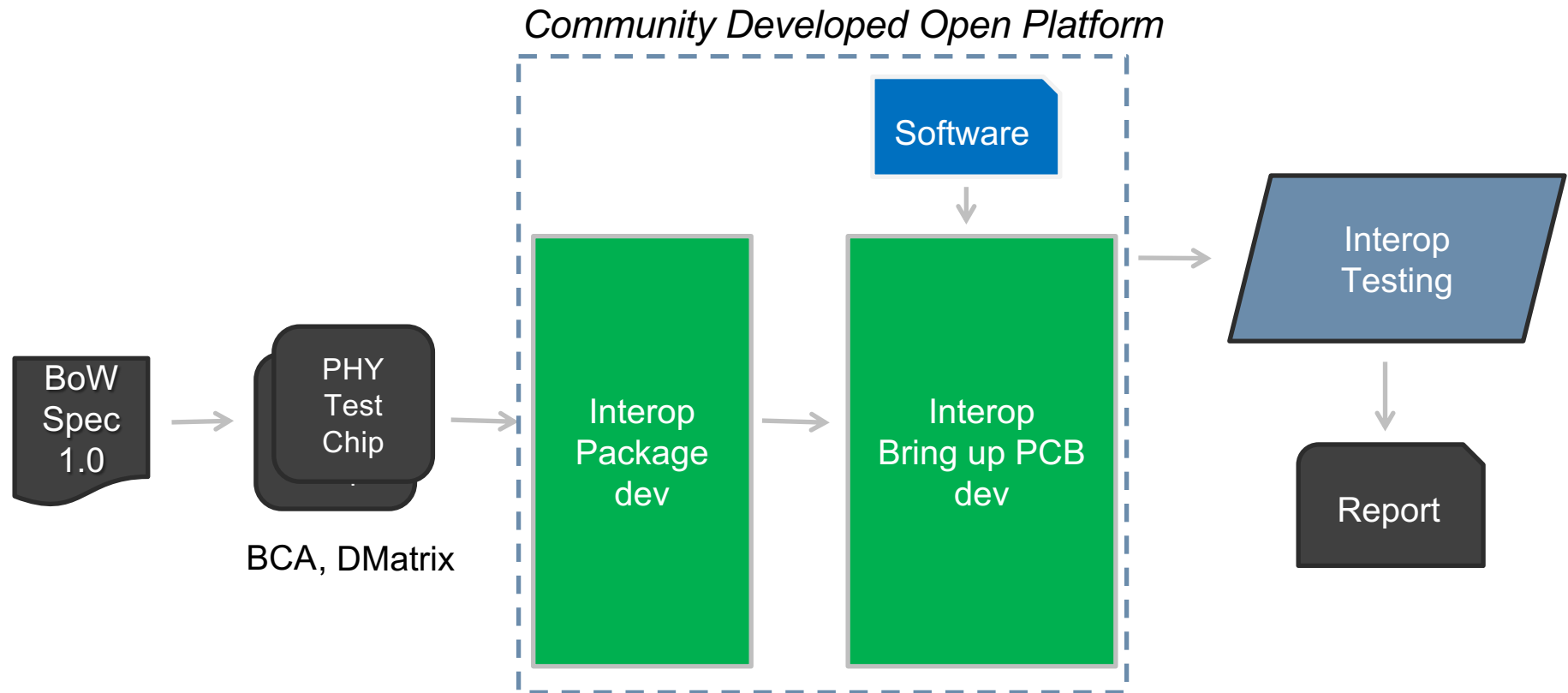
Interop Objective

- Demonstrate interoperability between two independent PHY implementations based on BoW spec 1.0



- Bring confidence to adopters

BoW Interop Platform



BoW Interop Community



IIT Bombay



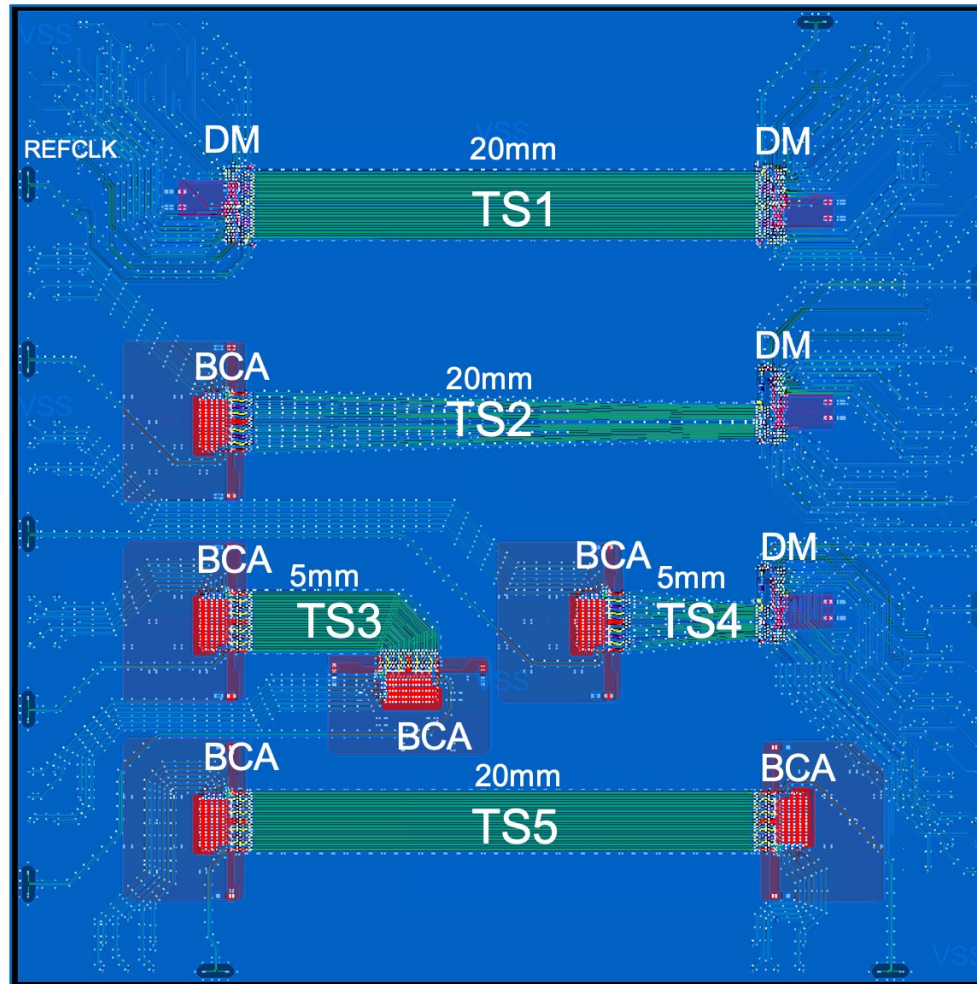
BLUE CHEETAH
ANALOG DESIGN



January 24 - 26, 2023
DoubleTree by Hilton San Jose
ChipletSummit.com



BoW Interop Substrate

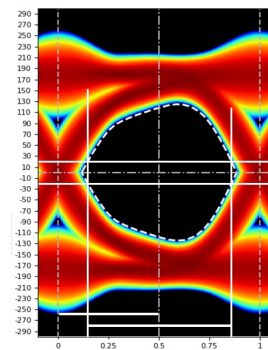
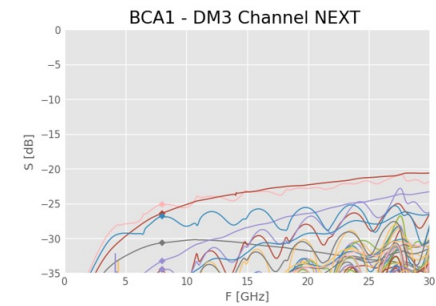
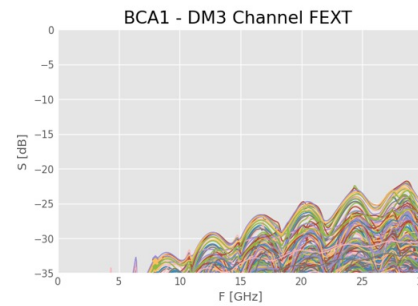
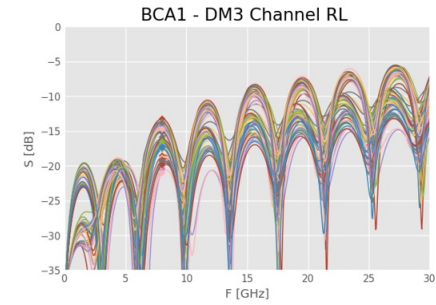
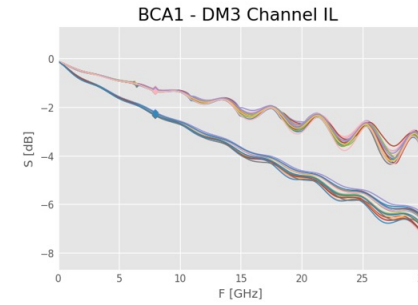
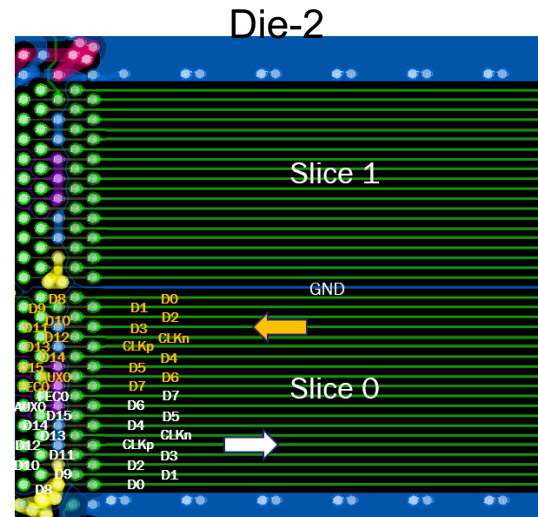
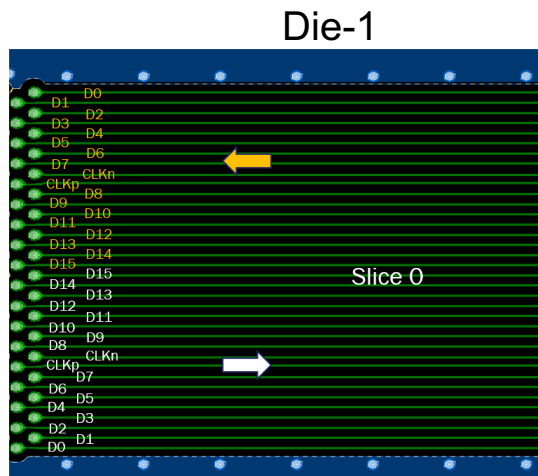


*5 Test Structures
10 dies
16 Gbps D2D data rate*

BoW Interop Substrate

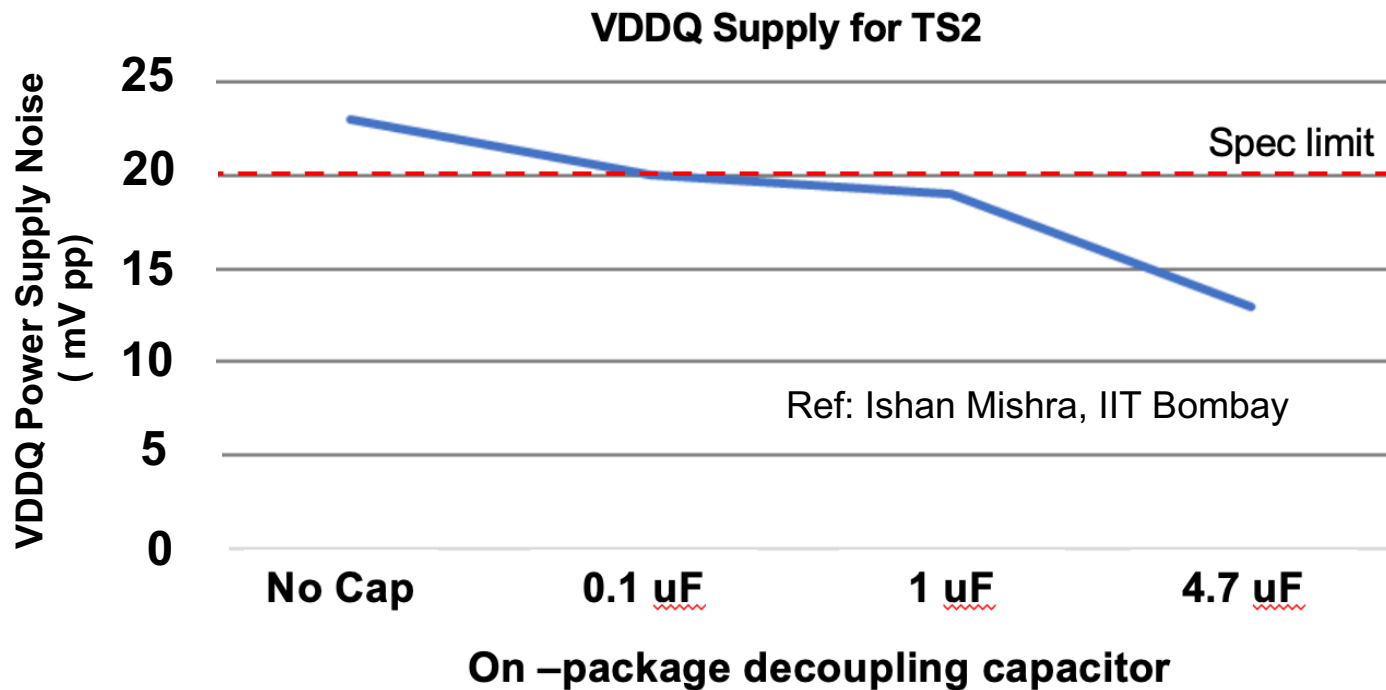
Package Design Attribute	Value
# dies per package	10 (BCA – 6, dMatrix – 4)
Package size	40 x 40 mm FCBGA
Layer count	5-2-5
Bump pitch	130 um
BGA Ball Pitch	1 mm
Package build up dielectric	GL102
# Test Sites	5 .L – 20 mm long trace .S – 5 mm short trace

Interop PKG Layout Meets BoW SI Requirements



40 mV sensitivity,
EW = 72 % @ 1e-15 BER

Interop PKG meets Power Integrity Specs



Power Integrity Specs met for all power supply rails in all test structures

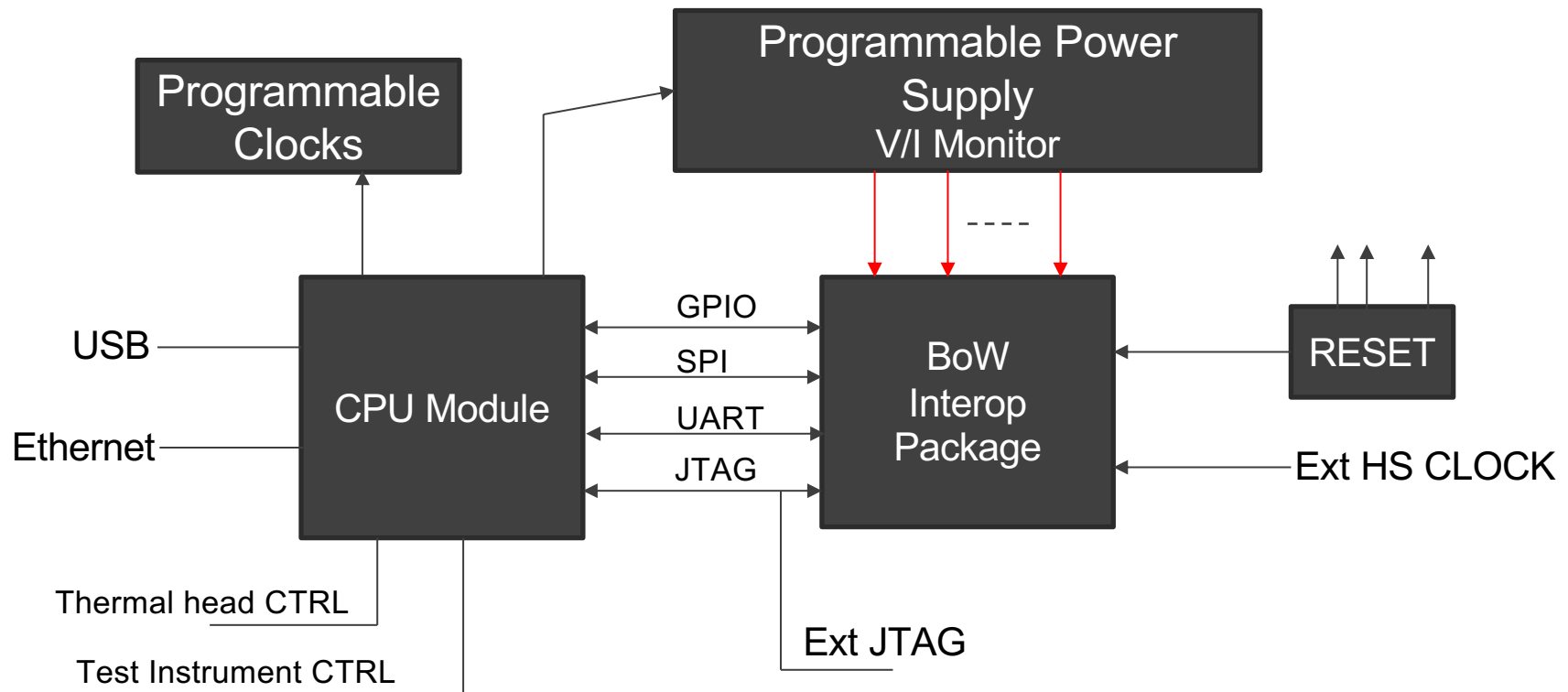
Successfully Addressed Power Integrity Challenges

- High PDN loop inductance
- S-parameter Convergence
- Noise aliasing
- Chip-Package resonance

SI Simulation Challenges

- Extending BoW to 32 Gbps data rates
- Crosstalk – a limiter for performance
- Need better simulation methodologies
 - Excessive EM simulation time for 32 Gbps data rates
 - Include Power bumps as return path in the sim

PCB Platform for Interop Testing



Future Directions

- Fabricate Interop Package and PCB
- Interop Testing and Publish results
- Establish feasibility of 32 Gbps
- New Simulation Techniques for BoW link SI Simulations

Summary

- Facilitate BoW Deployments in commercial products through Interop Testing and Validation
 - First of its kind for chiplets
- Open Interop Platform dev in Progress
- Join us and drive chiplet innovation
 - Weekly Meetings : Wed, 10 – 11 AM



January 24 - 26, 2023
DoubleTree by Hilton San Jose
ChipletSummit.com





January 24 - 26, 2023
DoubleTree by Hilton San Jose
ChipletSummit.com

Thank you !