OCP – ODSA Project

Open Platform Development for BoW PHY Interoperability Testing

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Interoperability Key for Chiplet based IC Designs

Chiplet based Integrated Circuit

Vendor A CPU

Vendor A CPU

Vendor D HSIO

Vendor B Accelerator

Vendor C Memory Controller

Package

interoperability
Interop Objective

- Demonstrate interoperability between two independent PHY implementations based on BoW spec 1.0

- Bring confidence to adopters
BoW Interop Platform

Community Developed Open Platform

BoW Spec 1.0 → PHY Test Chip → Interop Package dev → Interop Bring up PCB dev → Software → Interop Testing

BCA, DMatrix

Report
BoW Interop Community
BoW Interop Substrate

5 Test Structures
10 dies
16 Gbps D2D data rate
### BoW Interop Substrate

<table>
<thead>
<tr>
<th>Package Design Attribute</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td># dies per package</td>
<td>10 (BCA – 6, dMatrix – 4)</td>
</tr>
<tr>
<td>Package size</td>
<td>40 x 40 mm FCBGA</td>
</tr>
<tr>
<td>Layer count</td>
<td>5-2-5</td>
</tr>
<tr>
<td>Bump pitch</td>
<td>130 um</td>
</tr>
<tr>
<td>BGA Ball Pitch</td>
<td>1 mm</td>
</tr>
<tr>
<td>Package build up dielectric</td>
<td>GL102</td>
</tr>
<tr>
<td># Test Sites</td>
<td>5 .L – 20 mm long trace .S – 5 mm short trace</td>
</tr>
</tbody>
</table>
Interop PKG Layout Meets BoW SI Requirements
Interop PKG meets Power Integrity Specs

Power Integrity Specs met for all power supply rails in all test structures

Ref: Ishan Mishra, IIT Bombay

VDDQ Supply for TS2

VDDQ Power Supply Noise (mV pp)

Spec limit

No Cap  0.1 uF  1 uF  4.7 uF
On-package decoupling capacitor
Successfully Addressed Power Integrity Challenges

- High PDN loop inductance
- S-parameter Convergence
- Noise aliasing
- Chip-Package resonance
SI Simulation Challenges

- Extending BoW to 32 Gbps data rates
- Crosstalk – a limiter for performance
- Need better simulation methodologies
  - Excessive EM simulation time for 32 Gbps data rates
  - Include Power bumps as return path in the sim
PCB Platform for Interop Testing

- Programmable Clocks
- Programmable Power Supply
- V/I Monitor
- RESET
- CPU Module
- USB
- Ethernet
- GPIO
- SPI
- UART
- JTAG
- BoW Interop Package
- Ext JTAG
- Ext HS CLOCK
- Thermal head CTRL
- Test Instrument CTRL
- RESET
Future Directions

- Fabricate Interop Package and PCB
- Interop Testing and Publish results
- Establish feasibility of 32 Gbps
- New Simulation Techniques for BoW link SI Simulations
Summary

- Facilitate BoW Deployments in commercial products through Interop Testing and Validation
  - First of its kind for chiplets
- Open Interop Platform dev in Progress
- Join us and drive chiplet innovation
  - Weekly Meetings : Wed, 10 – 11 AM
Thank you!