

SERDES at 224 GBps and Beyond

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I. 112 GBps to 224 GBps, and trend to 448 GBps

A Summary for CEI-112G IAs

Parameter	XSR	XSR+	VSR	MR	LR
Data Rate (Gbps)	72 -116	72 -116	72 -116	72 -116	72 -116
BER (max)	1E-15	1E-15	1E-15	1E-15	1E-15
Distance (max)	50 mm	60+ mm	220 mm	500 mm	1000 mm
Interconnect	PCB+ 0 connector	PCB+ 1 connector	PCB + 1 connector	PCB + 1 connector	PCB + 2 connectors
Insertion Loss (dB) (at f_N)	10	13	16	20	28
Modulation	PAM4	PAM4	PAM4	PAM4	PAM4
Sys Power Target (pJ/b)	1	1.5	1.75	3.5	4.9
FEC	Y	Y	Y	Y	Y

Power estimate assuming 7 nm or equivalent

- PAM4 common modulation cross all the reaches.
- Compatibility and lower cost/power for the ecosystem

A Summary CEI-224G IAs and Characteristics (As of Oct, 2024)

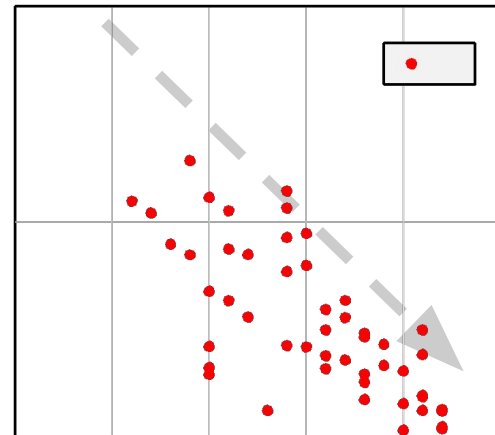
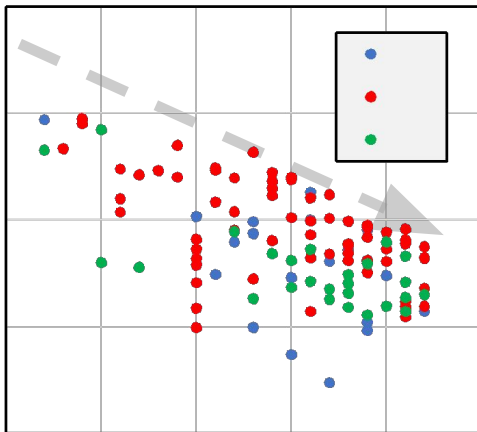
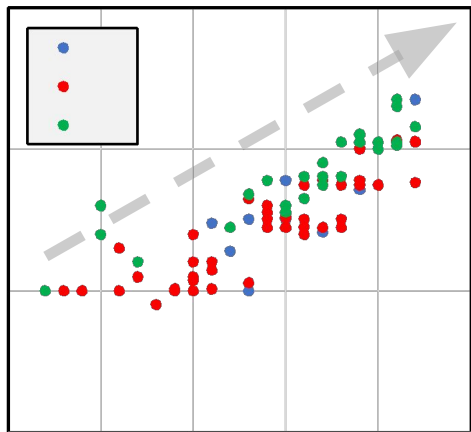
Parameter	XSR	VSR	MR	LR
Data Rate (Gbps)	144 - 232	144 -232	144 -232	144 -232
BER (max)	1E-15	1E-15	1E-15	1E-15
Distance (max)	50 mm	220 mm	500 mm	1000 mm
Interconnect	PCB+ 0 connector	PCB + 1 connector	PCB + 1 connector	PCB + 2 connectors
Insertion Loss (dB) (at f_N , bump-bump)	~15	32	35	40
Modulation	PAM4	PAM4	PAM4	PAM4
Sys Power Target (pJ/b)	0.7	1.2	2.5	3.5
FEC	Y	Y	Y	Y

Power estimates assumes process technology in 2024-2025 (e.g., N3, N2, 18A)

- Common modulation cross all the reaches enables compatibility and lower cost/power for the ecosystem

CMOS Electrical Links in the Past 20 Years

- Both speed and efficiency have scaled by $>20\times$ in the past 20 years!
- The trend is expected to continue



From ISSCC/VLSI (2002-2022)

Paths to 448 Gbps?

Back to the Basics: Shannon's Law

Data Rate R [bps] must be smaller than Capacity C [bps] to

work

$$C = W \cdot \log_2 \left(1 + \frac{S}{N} \right)$$

What can we do to get as close as possible to the capacity?

What can we do in order to get the channel better? (better BW&S/N)

Higher Order Modulation

Coding/FEC

Improve Ch/Pkg BW & Noise

- PAM_n, or QAM? or DMT?
- Can improve the capacity utilization, but does not increase the limit

How fast and how big the Improvement can be?

III. 448 GBps Modulation and Application Desirability

448 Gbps Modulation Scheme and Applications

- Currently, PAM4 is used in 53/106/212 Gbps Ethernet and OIF-CEI-56/112/224G
- Naturally, it is highly desired to continue using PAM4 to the 448 Gbps, considering
 - Backward compatibility
 - Electrical to optical compatibility
 - 448 Gbps-PAM4 optics feasible
 - Testing methodology and equipment maturity and availability

PAMn Modulation Considerations for 448 Gbps

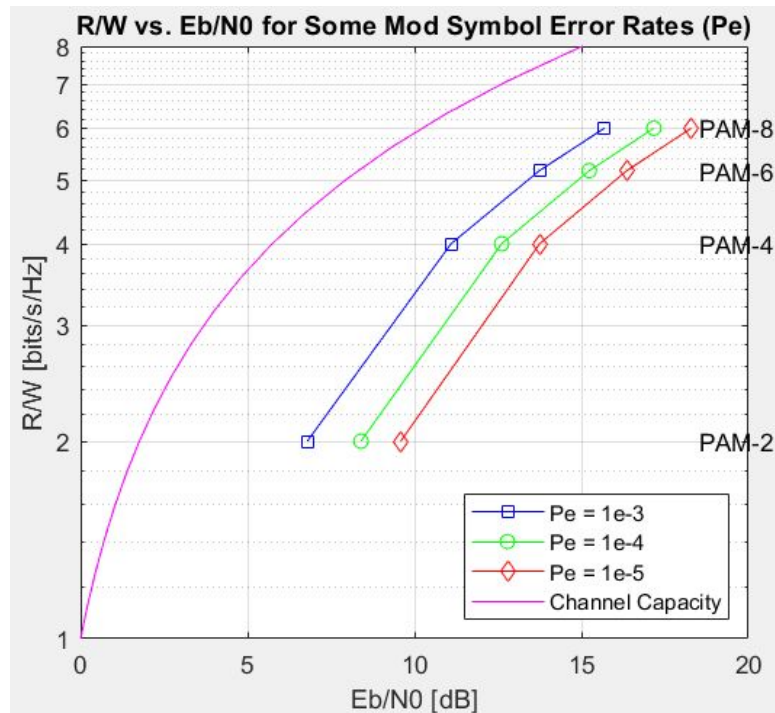
- To continue using PAM4 for 448 Gbps implies
 - SERDES:
 - 2X symbol rate, 2X bandwidth (BW) for AFE, 2X reduction in jitter/noise spectrum density compared with 224 Gbps PAM4.
 - Channel
 - End-to-end channel (including package, break-out, PCB/cable, and connectors) performance needs to improve such that the IL at its Nyquist will be kept at the close vicinity of those for 224 Gbps-PAM4.

Comparisons of 448 Gbps PAM_n Modulations

Data Rate (GB/s)	448	448	448	448	448	448
PAM _n Levels	4	5	6	7	8	16
Bit per symbol	2.00	2.32	2.58	2.81	3.00	4.00
Symbol Rate (GS/s)	224.00	192.94	173.31	159.58	149.33	112.00
UI (ps)	4.46	5.18	5.77	6.27	6.70	8.93
Nyquist Freq (GHz)	112.00	96.47	86.66	79.79	74.67	56.00
SNR Delta (dB)	0.00	-2.50	-4.44	-6.02	-7.36	-13.98

PAMn on BW Efficiency Plane

- Different trajectory of different modulation on Bandwidth Efficiency Plane
- PAMn and their distance from channel capacity are the focus
 - Each PAMn location on BW Efficiency Plane depends on its symbol error probability (P_e)
 - Higher order PAMn of the same P_e requires larger E_b/N_0 for a given peak (or peak-to-peak) voltage and noise level
 - The lower E_b/N_0 , the closer to channel capacity and the higher P_e
 - The closer to channel capacity, the more complex and longer latency FECs are required for reliable communication, which is not liked by AI/ML



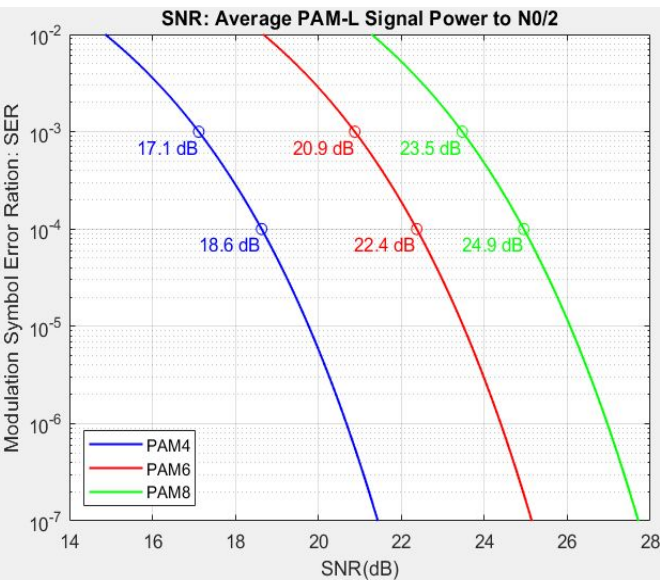
III. 448 Gbps PAM_n vs FEC

RS(l,k,t) over GF(2^m) with PAMn

- **Each PAMn modulation symbol (1 UI) carries $\log_2(n)$ bits**
 - PAMn UIs required to send each FEC symbol summarized in the table below
 - PAM2 (NRZ) uses 10 UIs, PAM4 uses 5 UIs, ...
 - FEC with higher order PAMn would suffer more from burst error

PAMn	$\log_2(n)$	Mod_Symb/FEC_Symb
2	1	10
4	2	5
6	$2.58 \approx 2.5$	4
8	3	$3.33 \approx 4$

Error Probabilities and FEC Performance

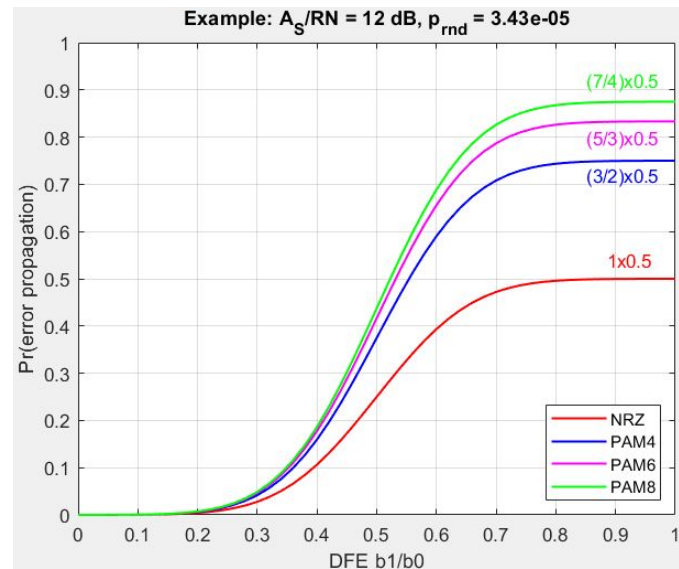


Random Error
Probability

Burst Error
Probability

Two-State Error Model

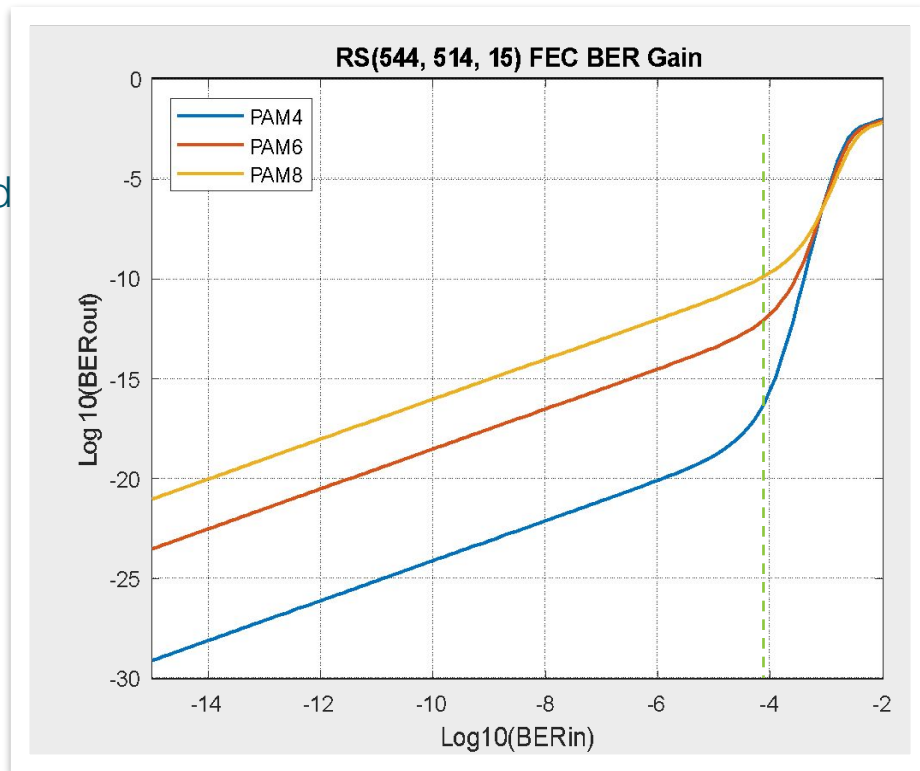
FEC Performance Model
(pre-FEC BER vs. post-FEC FER)



discussed in the following slides

Example KP FEC Performance vs. PAM-4/6/8

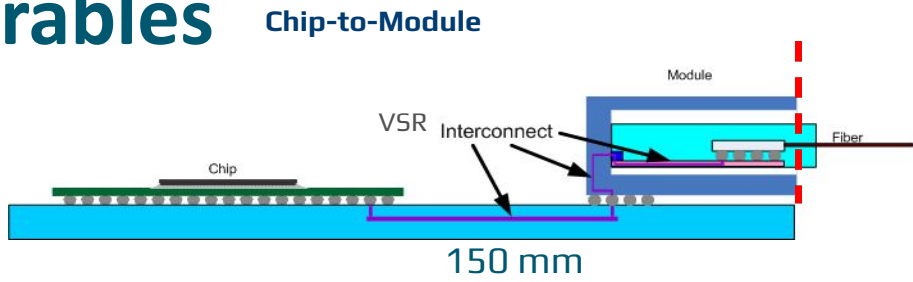
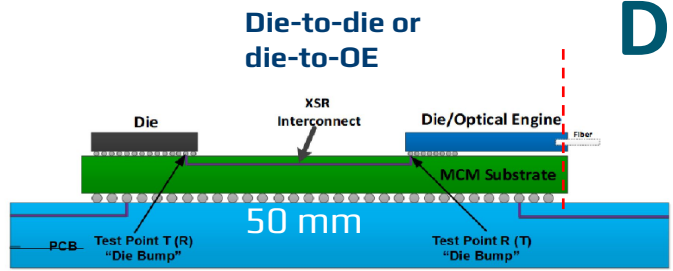
- FEC performance model
 - Obtained by combining FEC structure and two-state error model
- If max pre-FEC BER is 10^{-4}
 - PAM4 can achieve post-FEC BER $< 10^{-15}$
 - PAM6 and PAM8 would require stronger FEC to achieve post-FEC BER $< 10^{-15}$



IV. 448 Gbps Chip-to-Module Electrical Interfaces

448 GBps Chip-to-OE/Module Ecosystem

Desirables



	e-XSR	e-VSR	o-DR	Notes
224G	PAM4	PAM4	PAM4	
448G	PAM4 (feasible/desirable)	PAM4 (feasible*/desirable)	PAM4 (feasible**/desirable)	vs n>4 PAMn • backward comp • e-o comp • lower power/cost/TCO • better perf/latency
		*Assuming the connector IL is < ~10 dB at Nyquist	**Private conversations/demos	

448 Gbps SERDES

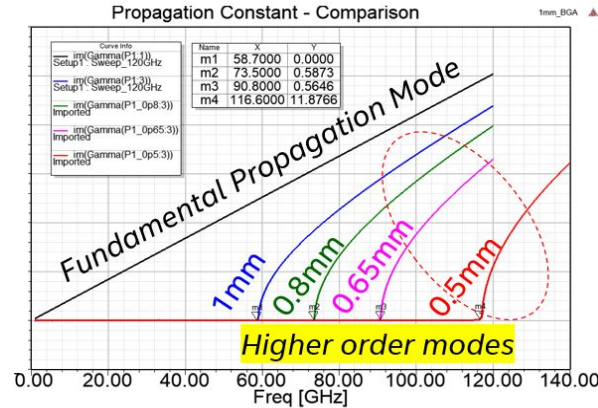
- With
 - advanced architecture, including advanced digital-to-analog converter (DAC)-based transmitter (TX), analog-to-digital converter (ADC)- based receiver (RX), advanced Analog Front End (AFE)
 - Efficient SNR-oriented calibration of ADC
 - Efficient convergence and adaptation algorithms
 - Advanced process nodes (e.g., $\leq N2$, $\leq 18A$)
- 448G-PAM4/PAM6 SERDES are feasible

448 Gbps Package

❑ Package BW depends on ball pitch

- 112G (PAM4): $\leq 1\text{mm}$
- 224G (PAM4): $\leq 0.8\text{mm}$
- 448G (PAM4): $\leq 0.5\text{mm}$

❑ Package ball pitch of $\leq 0.5\text{ mm}$ is available today !



Cut-off frequency of BGA ball pitch

BGA pitch	1.0mm	0.8mm	0.65mm	0.5mm
Cutoff Frequency	58GHz	72GHz	90GHz	115GHz

	224G		448G			
Modulation	PAM4	PAM6	PAM4	PAM6	PAM8	PAM16
Nyquist Freq, GHz	56 GHz	44.8 GHz	112 GHz	89.6 GHz	74.67 GHz	56 GHz

- PKG can support 448Gbps-PAM4 signaling, with $< 0.5\text{ mm}$ pitch, ball structure, advanced materials/stack ups (e.g., skip layer)

448 Gbps Chip-to-Module Channel Considerations

- PCB IL ~ 1.7 dB/in at 112 GHz
- Fly-over cable IL ~ 0.45 dB/in at 112 GHz
- If connector IL < 10 dB at 112 GHz



- Bump-bump IL < 40 dB at 112 GHz



- Bump-bump IL < 30 dB at 112 GHz
- C2M channel supporting 448Gbps-PAM4 signaling feasible with either PCB or fly-over medium

V. Summary

- PAM4 had served well for OIF CEI-56/112/224G, Ethernet 53/106/212G, and had been the dominate modulation for the ecosystem since 56 Gbps
- SERDES continues playing a critical role at 448 Gbps, and 448 Gbps-PAM4/6 SERDES are feasible with advanced process nodes (e.g., $\leq N2$, $\leq 18A$)
- Advanced package can support 448 Gbps-PAM4 signaling with a pitch < 0.5 mm, along with advanced materials, ball structure, and stack-ups (e.g., skip-layer)
- C2M channel can be designed to be < 40 dB at Nyquist if the connector IL is < 10 dB, which can be supported by a 448Gbps-PAM4 SERDES
- Benefits (critical to AI/ML) of 448 Gbps-PAM4 for C2M I/O over other higher order PAMn (e.g., PAM6/8) include
 - backward compatibility
 - e-o compatibility
 - lower power/cost/TCO
 - better perf/latency

Thank you!



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