Protocols over Die-to-Die Interfaces

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Two Broad Use Cases

Package Level Integration

SOC Disaggregation

*Use cases drive protocols!*
Protocols for Two Broad Use Cases

Package Level Integration
• Commonly attached to CPU
• Currently PCIe boards
• Developers want a coherent memory model
• Examples: CXL*, CCIX*, OpenCAPI*
• Consortium already in place here

SoC Die Disaggregation
• Currently on die module-to-module
• ASIC developers like their AXI*-style lightweight protocols
• Examples: AXI* Streaming, AXI4* (Memory Mapped)
Package Integration Protocols

**Application**
- Firmware Infrastructure for: Accelerator Use, Host Integration

**Transport**
- Coherent Protocol (CCIX or TileLink or...)
- Instruction-Driven Transfer (ISF Transport Layer)
- DMA

**Network**
- Routing (To Be Developed From ISF Routing Layer)

**Link**
- Inter-Chiplet (e.g., PCIe, TileLink or new Link Layer)
- Intra-Chiplet (From ISF Link Layer)

**PHY**
- PCIe2 PHY
- XSR2
- USR SerDes
- Bunch of Wires (BOW), AIB

**Substrate**
- Organic Substrate Packaging + Interconnect

**Chiplet**
- NFP
- RISC2
- FPGA
- ML ASIC
- SerDes

*Source: ODSA*
Package Integration Protocols

Firmware Infrastructure for:
Accelerator Use, Host Integration

Transport
- PCIe*
- CXL*
- CCIX*
- TileLink*

Network
- PCIe PIPE
- PHY
  - PCIe² PHY
  - XSR²
  - USR SerDes
  - Bunch of Wires (BOW), AIB

Link
- Organic Substrate Packaging + Interconnect

Substrate
- Chiplet
  - NFP
  - RISC²
  - FPGA
  - ML ASIC
  - SerDes

Source: ODSA
Package Integration Protocols

Source: ODSA

Bunch of Wires (BOW), AIB

Source: Intel, “PHY Interface for the PCI Express, SATA, USB 3.1, DisplayPort and Converged IO Architectures”

Source: ODSA
# Package Integration Protocols

<table>
<thead>
<tr>
<th>Application</th>
<th>Transport</th>
<th>Network</th>
<th>Link</th>
<th>Substrate</th>
<th>Chiplet</th>
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</thead>
<tbody>
<tr>
<td>PCIe*</td>
<td>PCIe Adapter*</td>
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<td>CXL*</td>
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<td>PCI Express Packaging* + Interconnect</td>
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<td>CCIx*</td>
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<td></td>
<td></td>
<td>NFP</td>
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<tr>
<td>TileLink*</td>
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<td>Bunch of Wires (BOW), AIB</td>
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<td>FPGA</td>
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<tr>
<td>PCI Express, CCIX, CXL</td>
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<td>ML ASIC</td>
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</tbody>
</table>

- **Firmware Infrastructure for:** Accelerator Use, Host Integration
- **Standard PIPE Interface follows PIPE Specification**
- **Adapter converts PIPE to native PHY interface (e.g. AIB, BoW, SERDES).**
- **Often PHY provider creates the PIPE adapter code.**
- **Upper stack to PIPE (PCI Express, CCIX, CXL) can be used as is!**

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**Sources:**
- ODSA, “Package Integration Protocols: The Future of Chiplet Design and Heterogeneous Integration”
- Intel, “PHY Interface for the PCI Express, SATA, USB 3.1, DisplayPort and Converged IO Architectures”
SoC Die Disaggregation Protocols

Strong preference towards using existing protocols
• Examples: AXI4, ACE, CXS, AXI Streaming

Evaluation Criteria
• Functional Requirements
  • E.g. Transaction ordering, Virtual channels, Error detection or correction, Data rates
• Throughput & Efficiency
• Latency
• Implementation Complexity
  • E.g. Flow control, retry/replay, CRC
• Adoptability (Current Usage)
SoC Die Disaggregation Protocols

Ideal protocol characteristics:
• Transfer rate linked to the sample rate (common clock reference), no gearboxing
• Data arrives every clock
• Low latency
• Simple convention on samples within a flit

Ideal protocol characteristics:
• Looks like AXI4 (Memory Mapped) to my SoC
• Efficiently multiplexes my SoC’s reads & writes
• Low latency
• Memory clock asynchronous to the transfer clock

→ SoC die disaggregation needs more than one protocol!
Two Different Stacks

Package Level Integration
• PIPE gives us a low-level interface that can support multiple existing protocols that have adopted PIPE
• With PIPE, we get PCIe*, CXL*, CCIX* Gen-Z*, SATA* – provide plug and play integration

SoC Disaggregation
• Innovation here is at the PHY: AIB, BoW, XSR
• Near-monolithic performance (close to on-die module to module) is critical: low latency, high bandwidth, low power

Package Level Integration and SoC Disaggregation need different protocols
### Protocols

#### Package Level Integration

- **Protocols**
  - Often incorporate a CPU
  - Common PIPE interface

#### SoC Disaggregation

- **Protocols**
  - Protocol Link Layer adapter to the PHY
  - Protocol Link Adapters have different features matching the applications

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**Package Level Integration**

**SoC Disaggregation**

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  - FPGA
  - ML ASIC
  - SerDes
  - ...
Protocols

Package Level Integration Protocols
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SoC Disaggregation Protocols
- Protocol Link Layer adapter to the PHY
- Protocol Link Adapters have different features matching the applications
Summary

“ODSA aims to define an open interface such that chiplets from multiple vendors that support the interface can be assembled into domain-specific products.” – Bapi Vinnakota

• ODSA is tackling protocols for chiplets
• Contact us if you’d like to contribute!
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