DCP FUTURE TECHNOLOGIES SYMPOSIUM

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A Path for 224Gb/s Solution for Intra-Data Center Interconnect

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Outline

- Introduction
- Electrical testbed
 - SNR vs Link
- Optical testbed
 - SNR vs channel loss and chromatic dispersion
- Conclusion



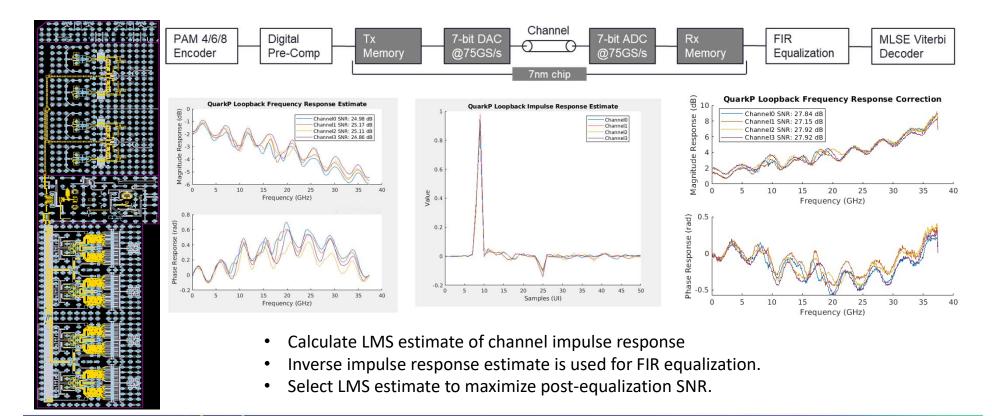
Introduction

- Ever-increasing internet data traffic is driving the modern data centers (DCs) into the so-called "Zettabyte Era".
- An estimated 71% of DC traffic stays within the DC, demand for more capacity across short distances is increasing fast and IM/DD is preferable for transmission reach up to 10 km of SMF.
- Silicon photonic (SiP): small footprint, low power consumption, and compatibility with CMOS circuits allows best price-performance ratio.
- Transceivers based on silicon photonics (SiP) are now estimated to account for >25% of products for short reach.
- For the next generation Ethernet targeting 800 GbE and 1.6 TbE over short reach distances, 200 Gbps/ λ is thus an important milestone.

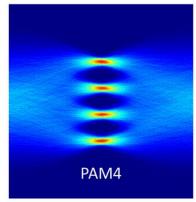
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Electrical Testbed

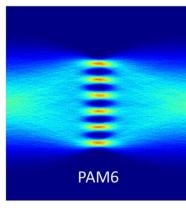
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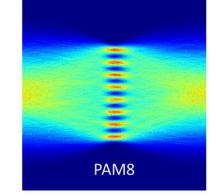
Electrical Testbed Results



150Gb/s, BW=37.5GHz, PWR=4.6pJ/bit, SER=0



195Gb/s, BW=37.5GHz, PWR= 3.6pJ/bit, SER=9.3e-6



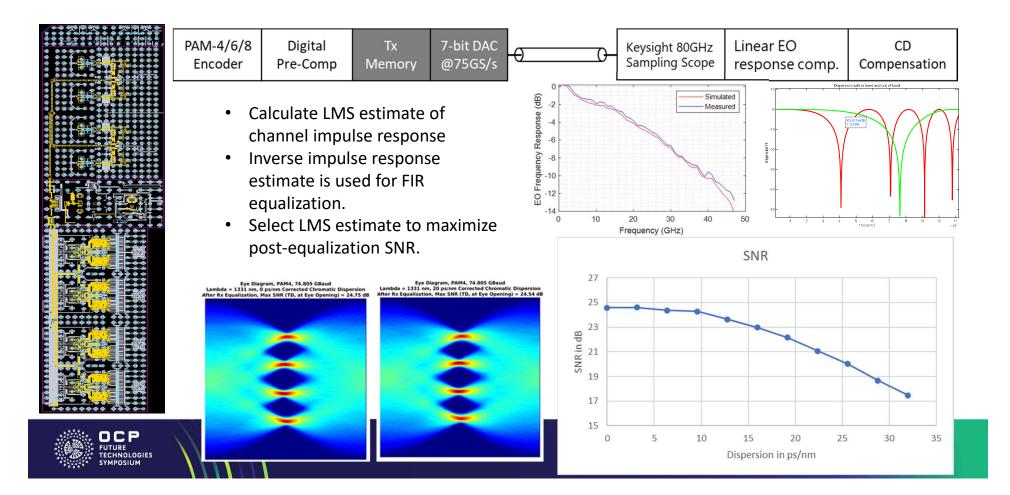
225Gb/s, BW=37.5GHz, PWR= 3.1pJ/bit, SER=6.3e-4

Residual Attenuation	PAM Order	Average SNR [dB]	BER (MLSE M=0)	BER (MLSE M=1)
8	4	24.6	0	0
8	6	24.4	5.7E-06	1.2E-06
8	8	24.5	4.3E-04	1.3E-04
13	4	21.7	7.6E-08	7.6E-08
13	6	21.3	6.0E-04	4.0E-04
13	8	21.3	1.0E-02	8.6E-03
18	4	15.6	4.9E-03	4.0E-03
18	6	15.2	7.6E-02	7.1E-02
18	8	15.0	1.9E-01	1.9E-01
NID and DED regults for different regidual abannel logs				

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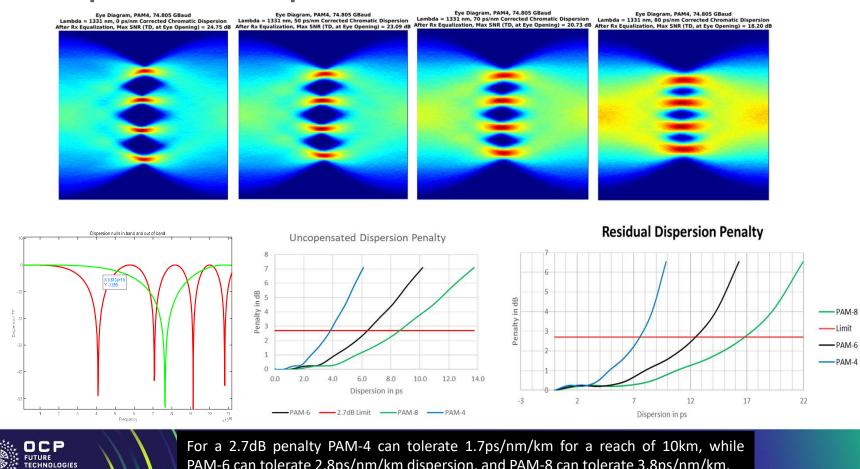
SNR and BER results for different residual channel loss

Optical Testbed



Dispersion impact

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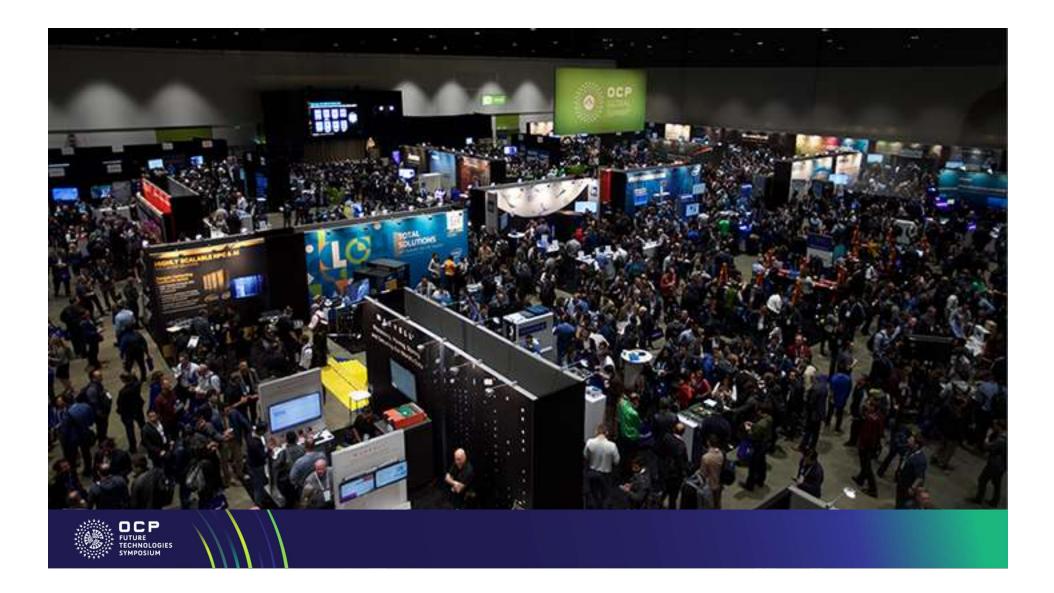


PAM-6 can tolerate 2.8ps/nm/km dispersion, and PAM-8 can tolerate 3.8ps/nm/km.

Conclusion

- A 224Gbps electrical links is feasible at VSR power target
- FFE and MLSE can improve the reach of 224Gbp to an LR link
- An LR electrical Serdes can address the requirements 200 Gbps/ λ IMDD
- FFE and MLSE can address the requirements for E/O channel compensation and chromatic dispersion mitigation for up to 10km link
- The performance of PAM4, 6, and 8 were assessed and we demonstrated a potential path for delivering the performance and power targets to enable the 1.6Tbps front panel plug at 10pJ/bit.







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