OCP SAI/SONiC
Workshop

# SONiC Powered by Programmable Data Planes

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# Data Plane Programmability Building Blocks

1. Open programming language & Community
2. Compiler & Chip Simulation Model
3. Visualization Tools
4. Flexible / Auto-generated APIs
5. Fully Programmable ASIC

**End-user Accessible**

# P4 Community and Ecosystem

**Strong community**

3000+ developers

5 active working groups

100+ member organizations

Growing Projects & Product

SONiC, ONF, OPENDAYLIGHT, ARISTA, cisco, CableLabs, vmware, Google, Alibaba Group, .io The Universal Dataplane, OvS Open vSwitch, STRATUM, HUAWEI, BAREFOOT NETWORKS an Intel company, NETCOPE TECHNOLOGIES, intel, AT&T, UCLOUD, T

# Barefoot Ecosystem

OEM | Brite Box | White Box

## Software

ARISTA, Ruijie, cisco, H3C

SONiC

ipinfusion SONiC

kaloom, STRATUM

NoviFlow, stateless

## Systems

ARISTA, Ruijie, cisco, H3C

ARISTA, cisco

Edge-corE NETWORKS, Accton, STORDIS

ufiSpace, FOXCONN, DELTA

英業達 Inventec, 恒为科技 EmbedWay

Celestica, Lanner, WNC Wistron NeWeb Corp.

## ASICs

6.4 Tb/s

3.2 Tb/s

2.4 Tb/s

2.0 Tb/s

1.8 Tb/s

12.8 Tb/s

8.0 Tb/s

6.4 Tb/s

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# Barefoot Intel Progress with SONiC in 2019

- Expand set of **supported platforms**
  - Tofino2 White box
  - Stordis OCP Accepted Switches
- **Testing & Hardening**
  - Multiple testbeds enabling CI/CD with SONiC and P4 data plane
  - Passing SONiC community test suite
  - Daily SONiC testing
- Continuous upstreaming of changes to **support latest SAI / SONiC releases** and **features**
  - SAI 1.5.1 support
  - High-scale VXLAN tunneling
  - Warm reboot

# P4-Programmable OCP Switches

OPEN ACCEPTED™

STORDIS

Advanced Programmable Switches
with Built-in Time Synchronization

**BF6064X-T**
**64x100G Switch**

**BF2556X-1T**
**48x10/25+8x100G**
**Switch**

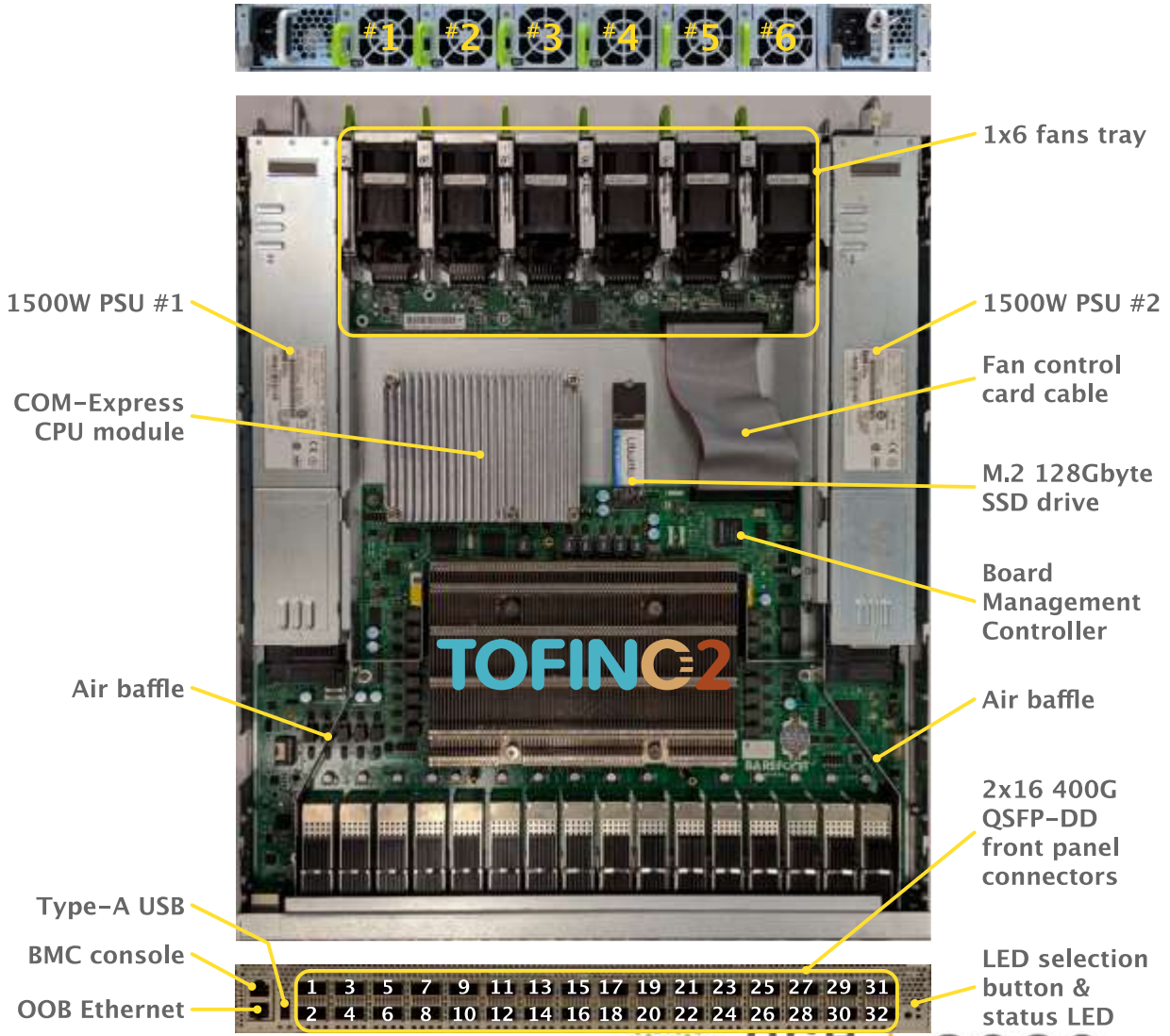
OPEN INSPIRED™

Edge-corE® NETWORKS

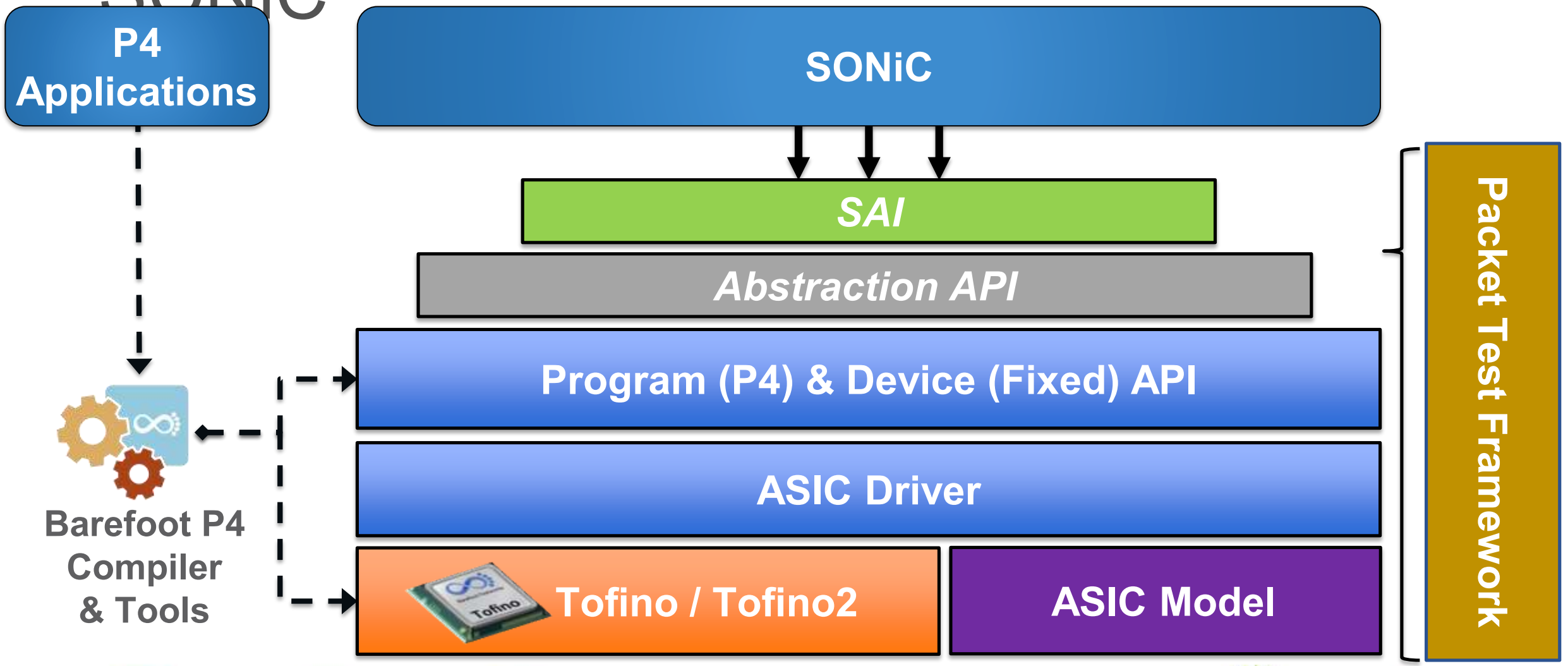
英業達 Inventec

# AS9516-32D – Tofino™ 2 Whitebox

- Now supports SONiC!
  - Same SDE / SAI as Tofino
  - P4 program with higher table scale
- System specifications
  - 1 RU
  - 32x400GE QSFP-DD ports (2x1 stacked QSFP-DD cages)
  - Intel® Xeon-D COM-Express CPU module

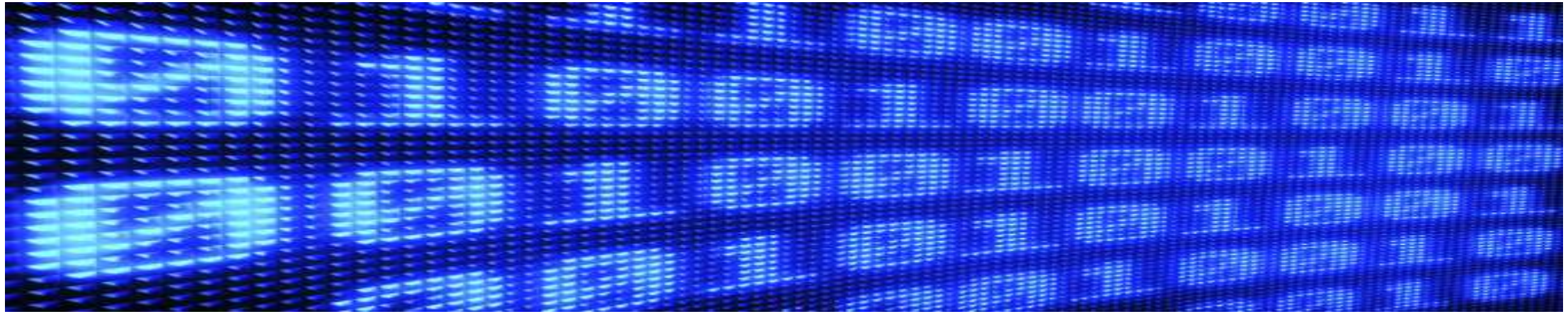


# Barefoot Intel Software Support for SONiC



# Barefoot Intel SONiC Delivery

| Option | Scenario |
| --- | --- |
| **Binary file on SONiC community page** | **Quick start with SONiC supported features** |
| Binary files provided by Barefoot support | Quick start with features not upstreamed |
| Compile from P4 Studio SDE | Data plane / SAI implementation change |



# Barefoot Intel SONiC Strategy

1. Validation of  SONIC master (specific ref point) with each GA release of P4 Studio SDE
2. Pass community tests with all P4 Studio SDE releases and coupled SONiC release / ref point
3. Maintain a SDE + SONiC combination for community test baseline


# Intel & Keysight Partnership

## Intel SONiC Hardening

- Double # of testbeds
- 100% of tests passed
- Daily SONiC validation
- Latest SAI / SONiC with every SDE release
- 70+ PRs submitted in 2019

SONiC
Microsoft
KEYSIGHT TECHNOLOGIES
BAREFOOT NETWORKS | an Intel company
intel

## Keysight SONiC Validation

- Contribute test methodologies
- UHD100T32 test platform
- Scalable, cost-effective & dev-ops friendly
- Keysight test leadership + Barefoot programmability

# Switching Between Different P4 Data Planes

1. In SONiC, edit /etc/sonic/config_db.json to include the p4_profile attribute:

```
…
"DEVICE_METADATA": { "localhost": {
…
"p4_profile": "<P4 program name"}}
```

2. Load the updated config_db.json:

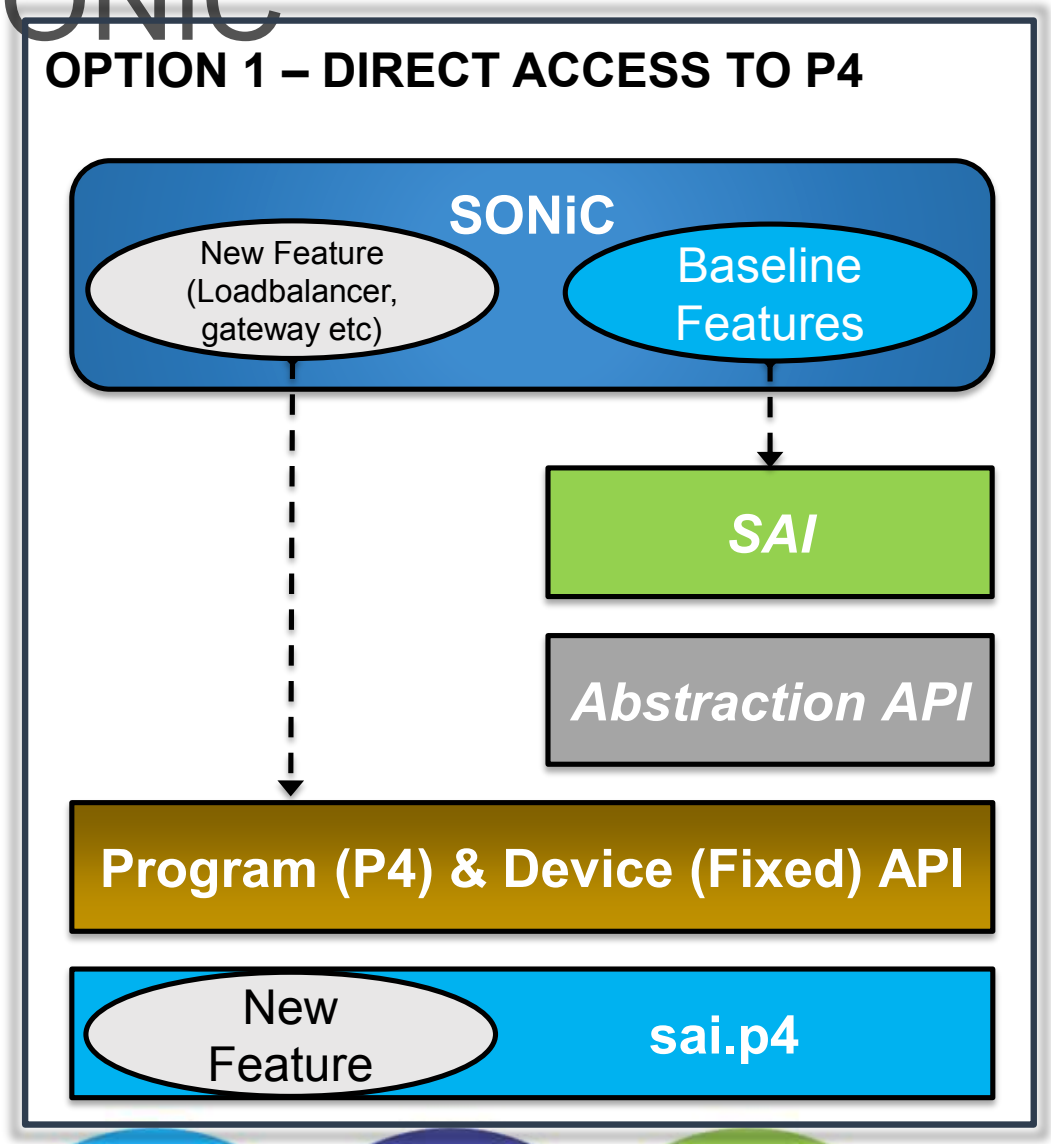
```
sudo config load -y
```

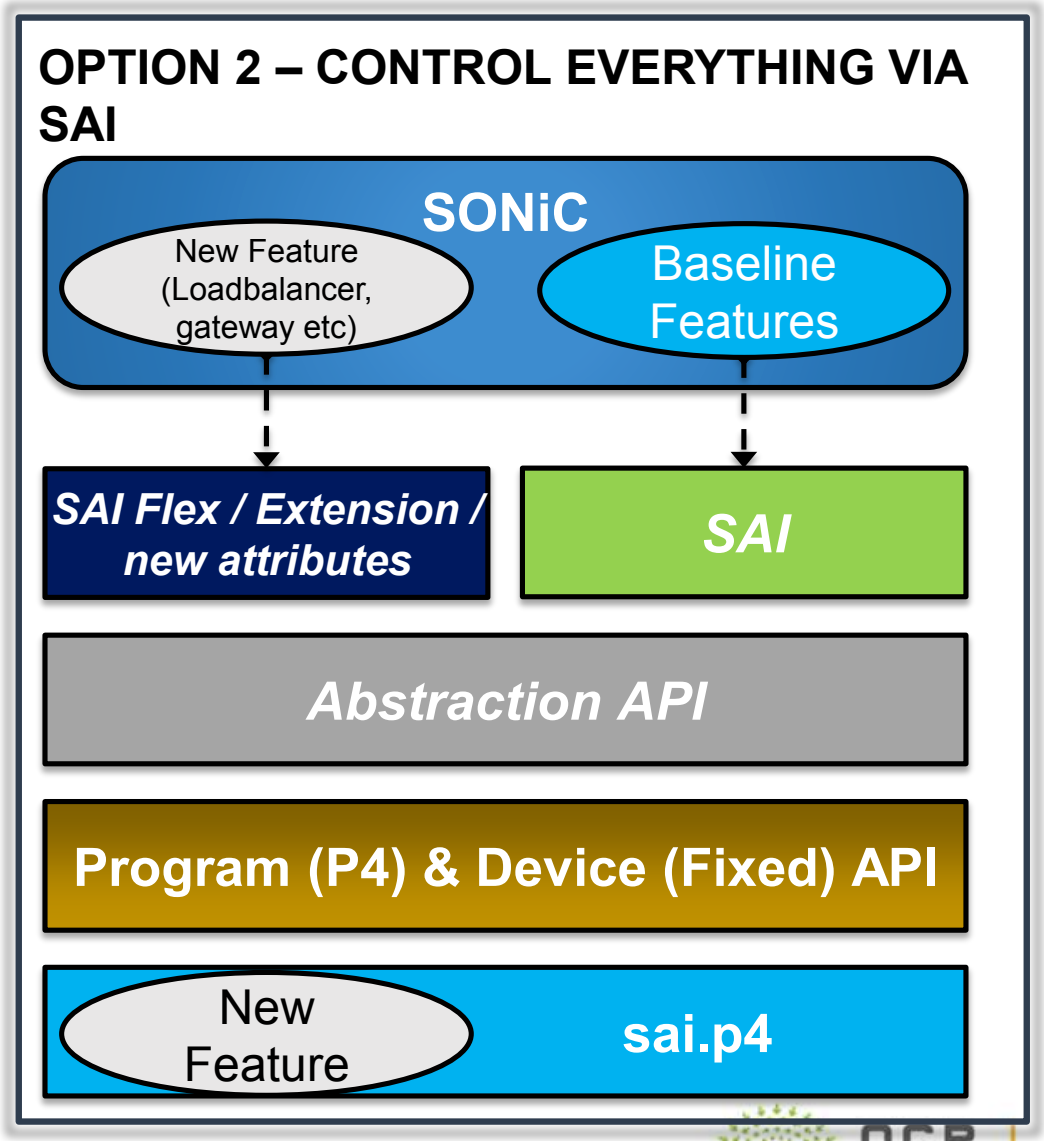
3. Reboot for the new data plane to take effect

Embedded P4 programs:

- **A_PROFILE**
  - Tofino Foundational Features + **Dataplane telemetry**
- **B_PROFILE**
  - Tofino Foundational Features + **High Scale tunneling**
- **C_PROFILE**
  - Tofino2 Foundational Features

# Custom Data Plane Integration Options with SONiC



# Use-case: SONiC and Table Scale

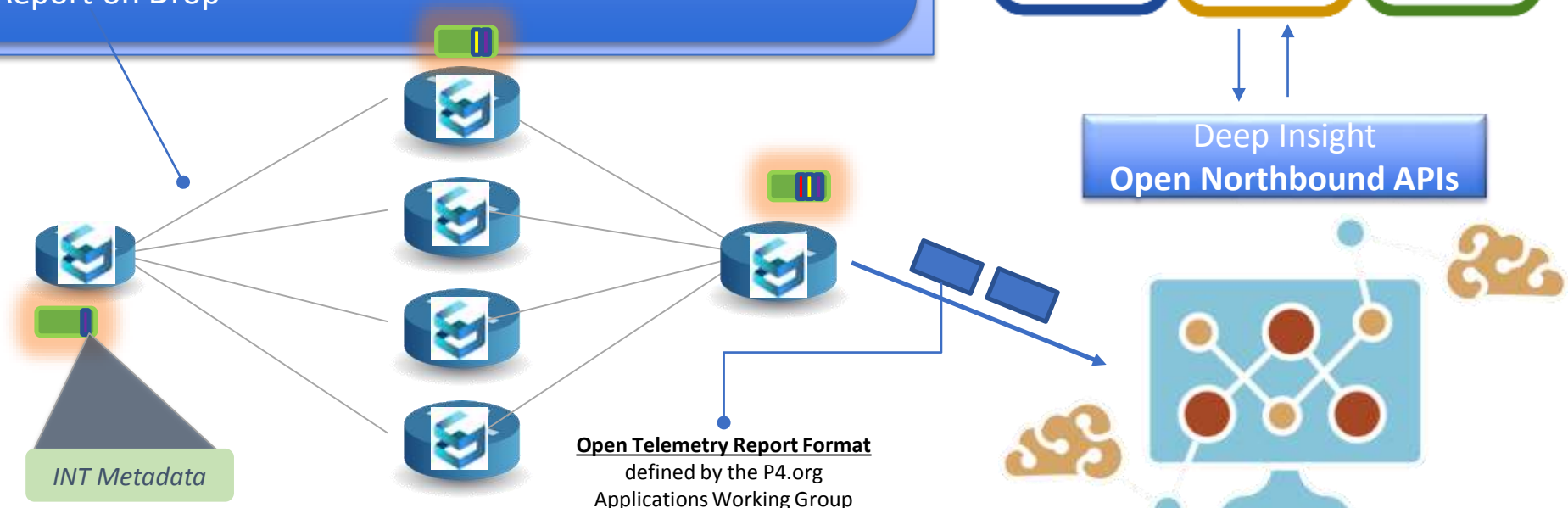
- Different table sizes for leaf and spine
- Different table sizes for different deployments
- Example: IPv4 vs IPv6 heavy fabric

| **Parameter** | **Scenario 1** | **Scenario 2** |
|---|---|---|
| IPv4 Host Local | High | Low |
| IPv4 LPM | Medium | Low |
| IPv6 Host | Low | High |
| IPv6 LPM | Low | Medium |

# Use-case: SONiC & Data-Plane Telemetry

**Barefoot Data-Plane Telemetry**

- In-Band Network Telemetry (INT)
- Intelligent Deduplication and Triggers
- Path & Latency Change Detection
- Microburst detection
- Report on Drop

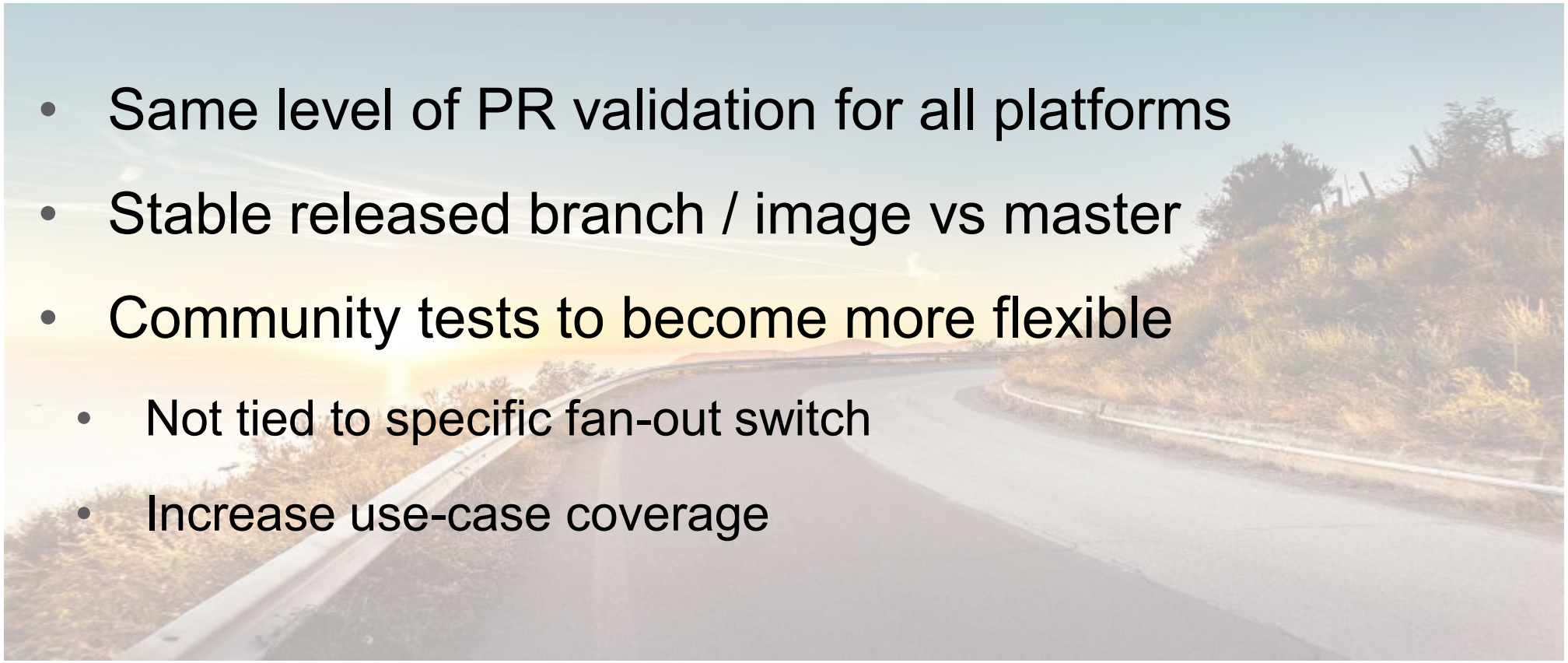



**Open Telemetry Report Format**
defined by the P4.org
Applications Working Group

**3rd Party Network Management Solutions**

Deep Insight
**Open Northbound APIs**

# Addressing SONIC Growing Pains Together



- Same level of PR validation for all platforms
- Stable released branch / image vs master
- Community tests to become more flexible
  - Not tied to specific fan-out switch
  - Increase use-case coverage