

Open Access Silicon Photonics Foundry

Dr Callum G Littlejohns
University of Southampton, UK

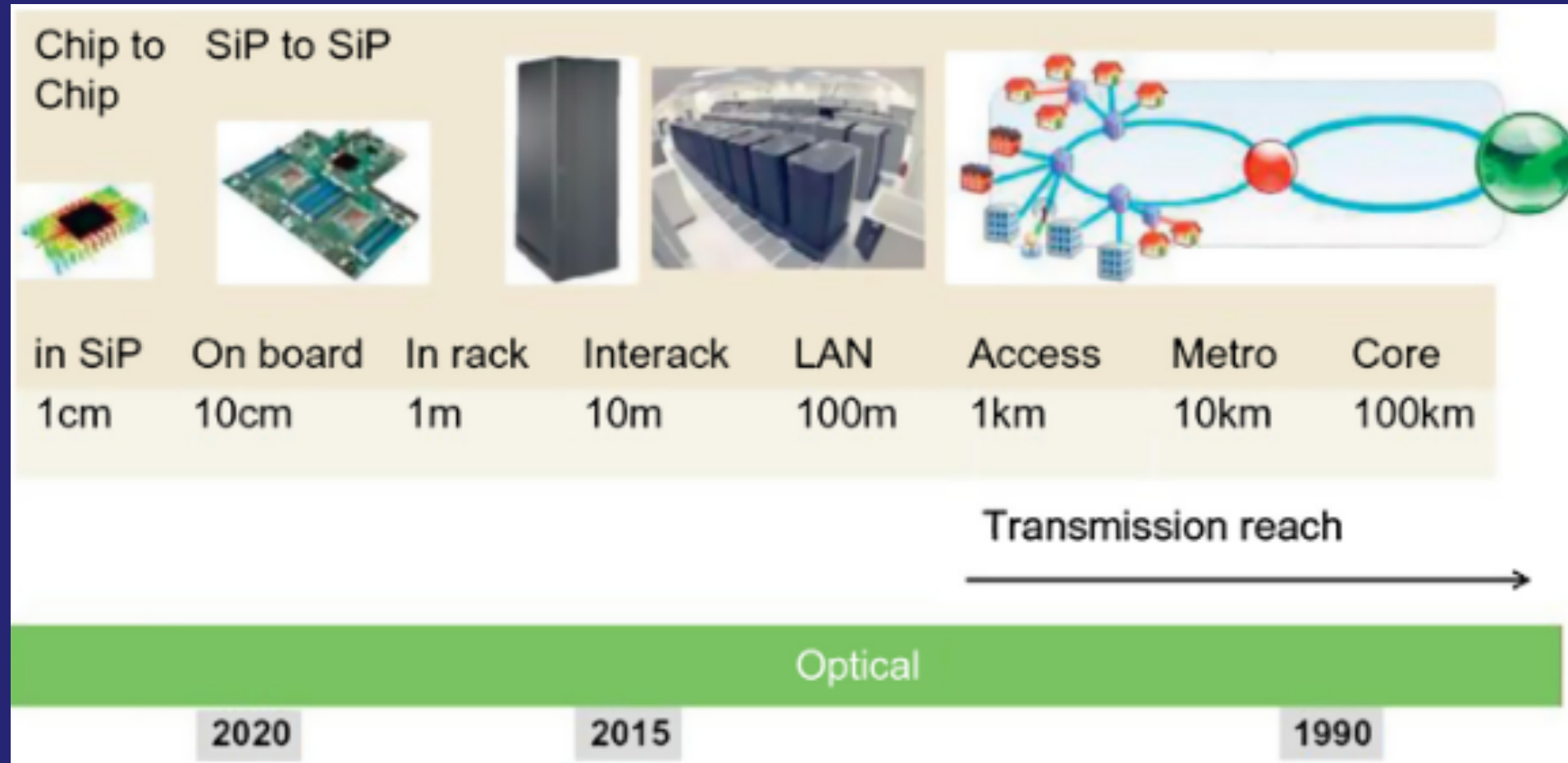
Open. Together.



OCP
REGIONAL
SUMMIT

Authors: Y. Hu, D. T. Tran, H. Du, M. Banakar, X. Yan, M. Sorel, J. England, H. Chong, F. Y. Gardes, D. J. Thomson, G. Z. Mashanovich, and G. T. Reed

Evolution of optics



M. Duranton et al., Optical Interconnects for Data Centers, 2017

Adoption of on-chip optical interconnects

- More Gbps per cm^2
- Less pJ per byte
- Less \$ per Gbps

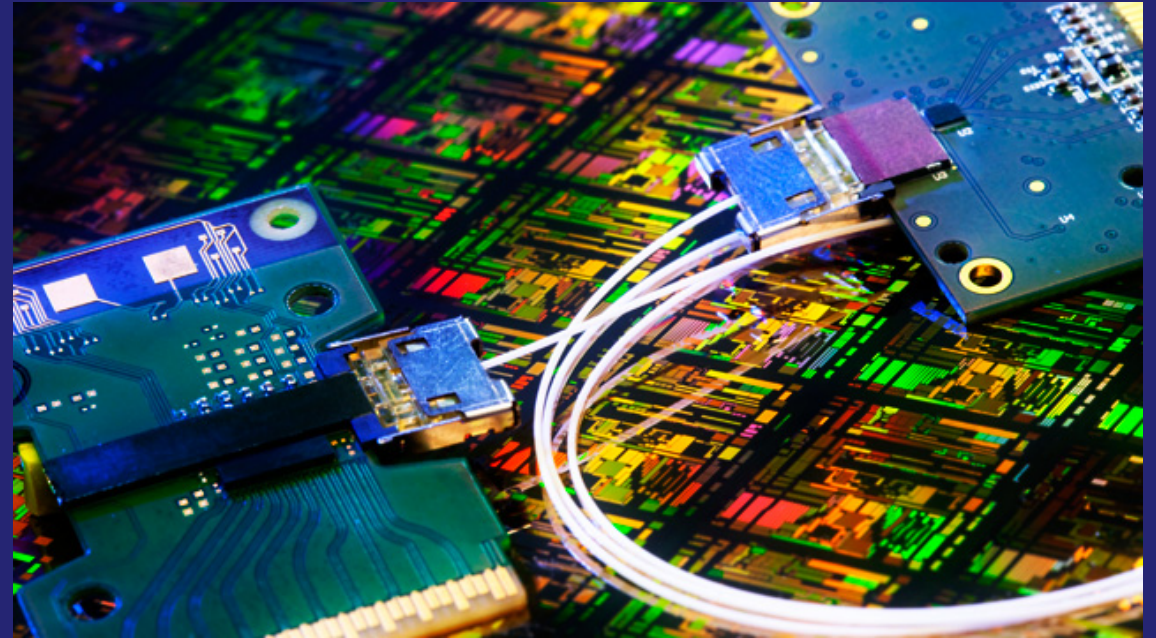
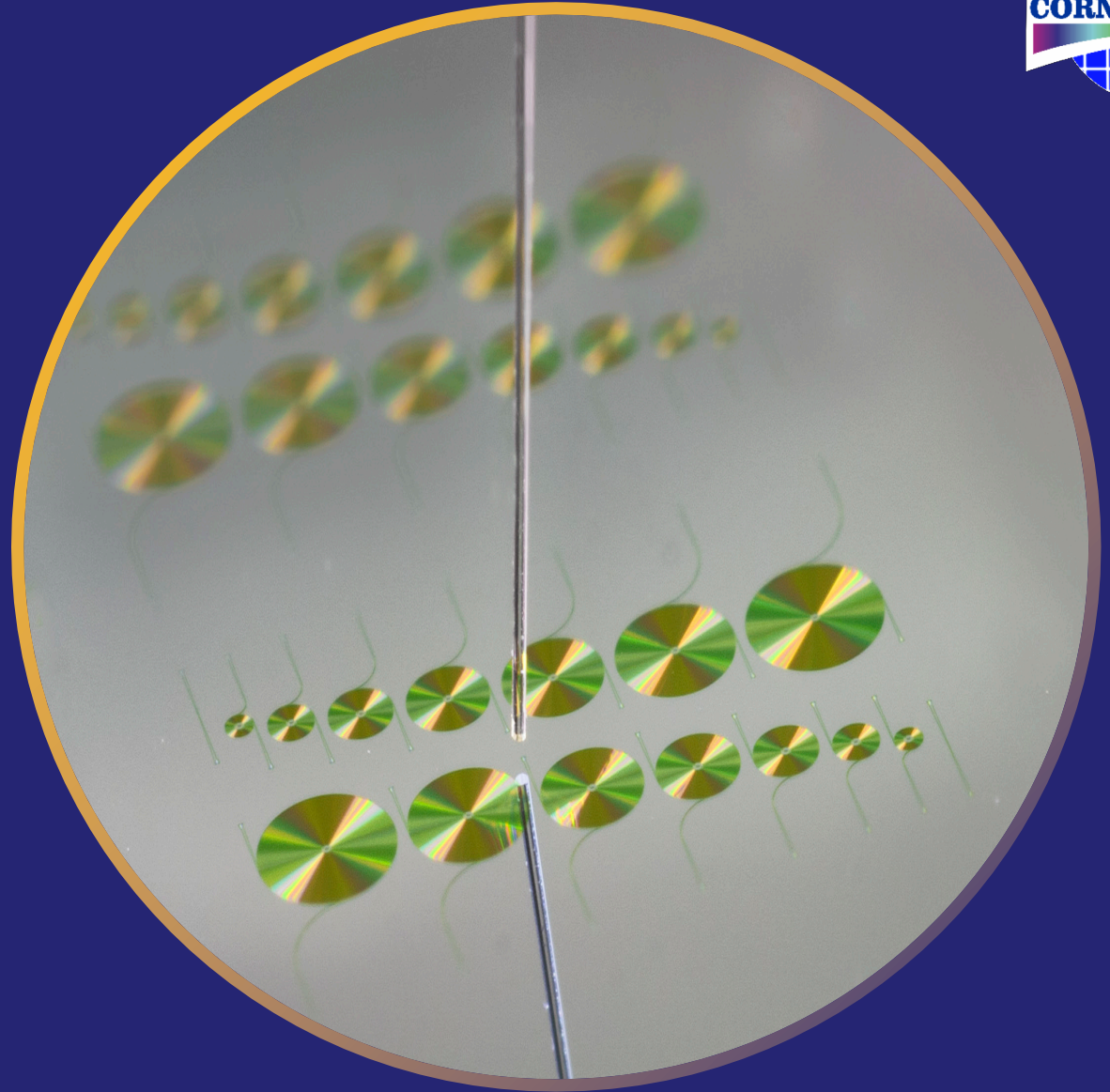


Image: Intel.

Silicon Photonics



What is silicon photonics?

The implementation of high density photonic integrated circuits by means of CMOS process technology in a CMOS fab



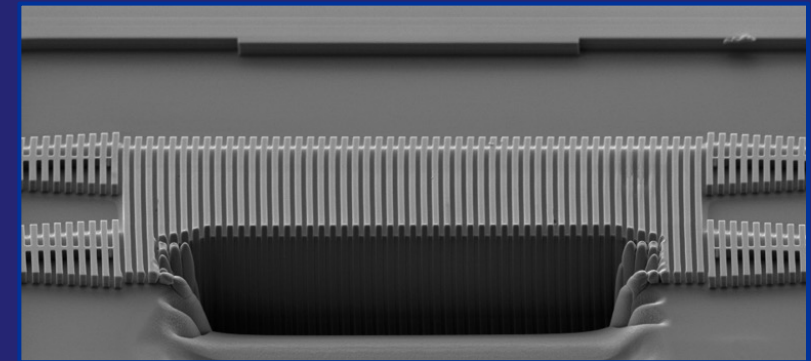
Pictures, courtesy of imec



Enabling complex optical functionality on a compact chip at low cost

Why silicon photonics?

- The prospect of integrating CMOS electronics and photonics on the same substrate:
 - Greater functionality.
 - Improved performance.
 - Cost reductions.
 - More advanced lithography.
- Mature processing derived from years of development in the electronics industry.
- High refractive index contrast (compact components).
- Massive interconnect density (WDM).
- Low cost.



Silicon photonics and CMOS

The **STRENGTH** of Silicon Photonics
is that it can make use of CMOS-technology

The **WEAKNESS** of Silicon Photonics
is that it must make use of CMOS-technology

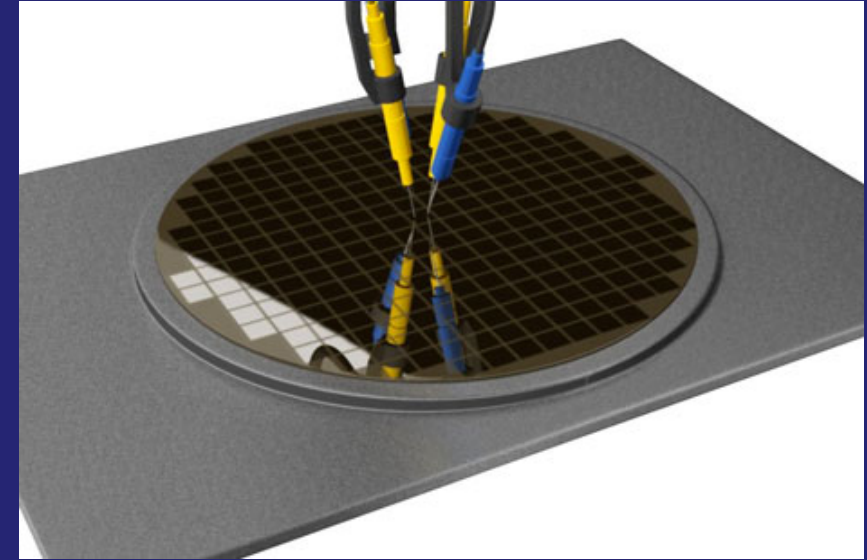
CMOS-technology requires extremely expensive infrastructure
with an extreme degree of sophistication
but delivers extremely cheap chips

Foundry Service



CORNERSTONE highlights

- Multi-project-wafer (MPW) service
- Various silicon-on-insulator (SOI) platforms
- Flexible processes
- Device prototyping at wafer scale
- Scalable process technology
- Hybrid processes using DUV lithography and e-beam lithography
- Competitive costs
- Potential for design consultancy



CORNERSTONE partners

Three UK universities are involved:

- 1) University of Southampton
 - Wafer-scale processing (DUV photolithography)
- 2) University of Glasgow
 - Chip-level processing (e-beam lithography)
- 3) University of Surrey
 - Ion implantation



Cleanroom capabilities @ Southampton

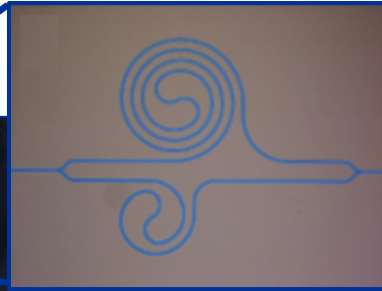
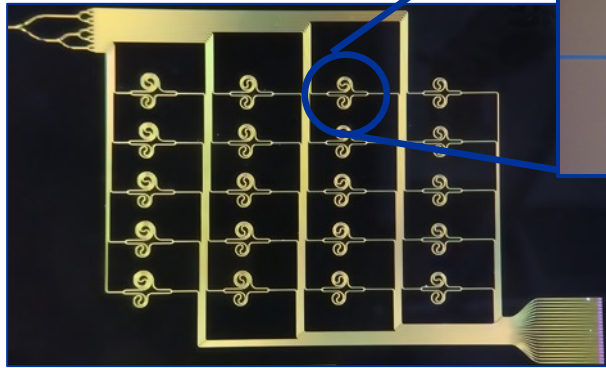
- DUV projection lithography
- E-beam lithography
- Contact lithography (i-line)
- Wet & dry etch systems
- Furnaces and RTA systems
- PECVD, LPCVD & ALD systems
- Evaporation & RI sputtering systems
- CMP, wafer dicing,...
- Bonding: wafer, wire, flip-chip
- FIB, SEM, ellipsometry,...



Device capabilities



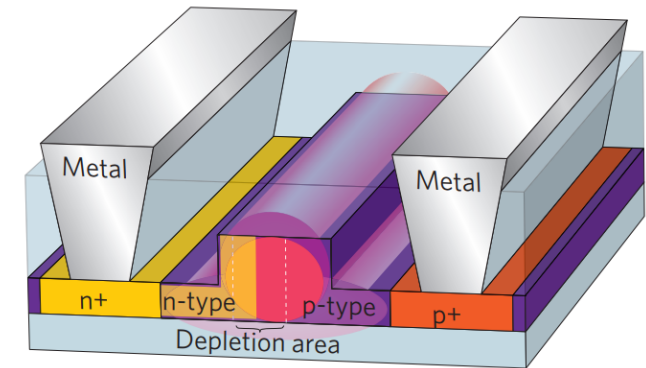
Spectrometers



M. Nedeljkovic et al., IEEE Photon. Technol. Lett., vol. **28**, iss. 4, 2016.

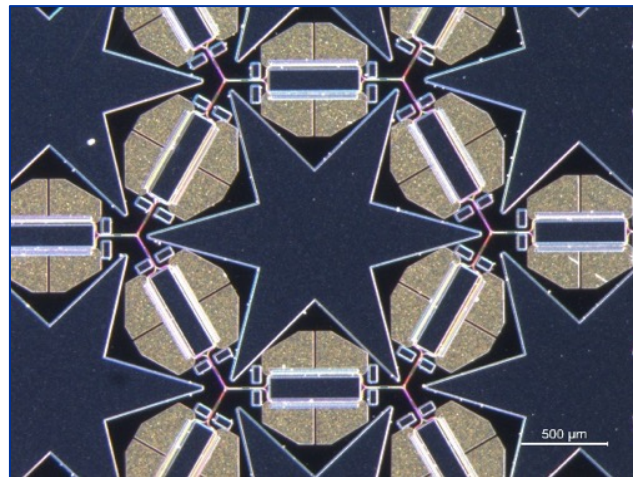
High speed modulators

G. T. Reed et al., Nat. Photonics, vol. **4**, iss. 8, 2010.



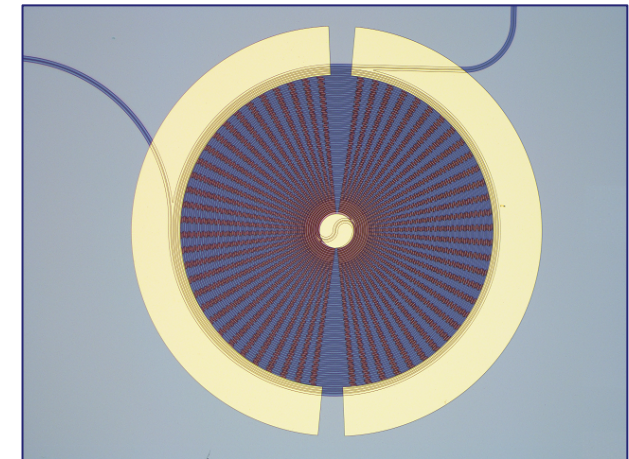
Tuneable processor cores

D. Pérez et al., Nat. Commun., vol. **8**, 636, 2017.



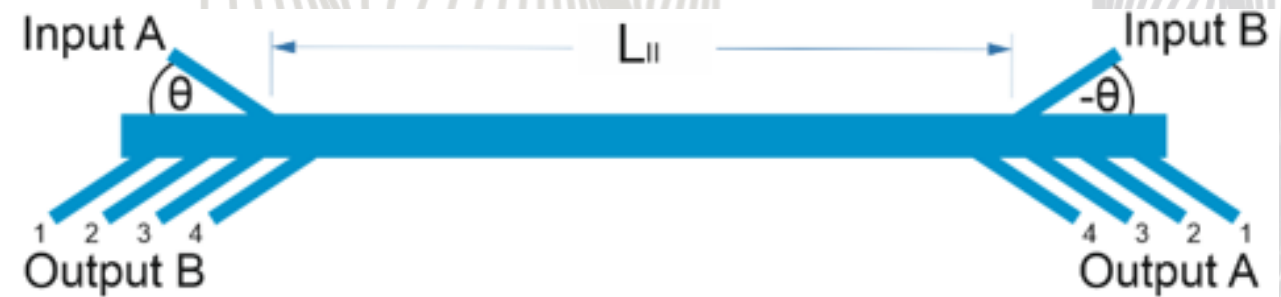
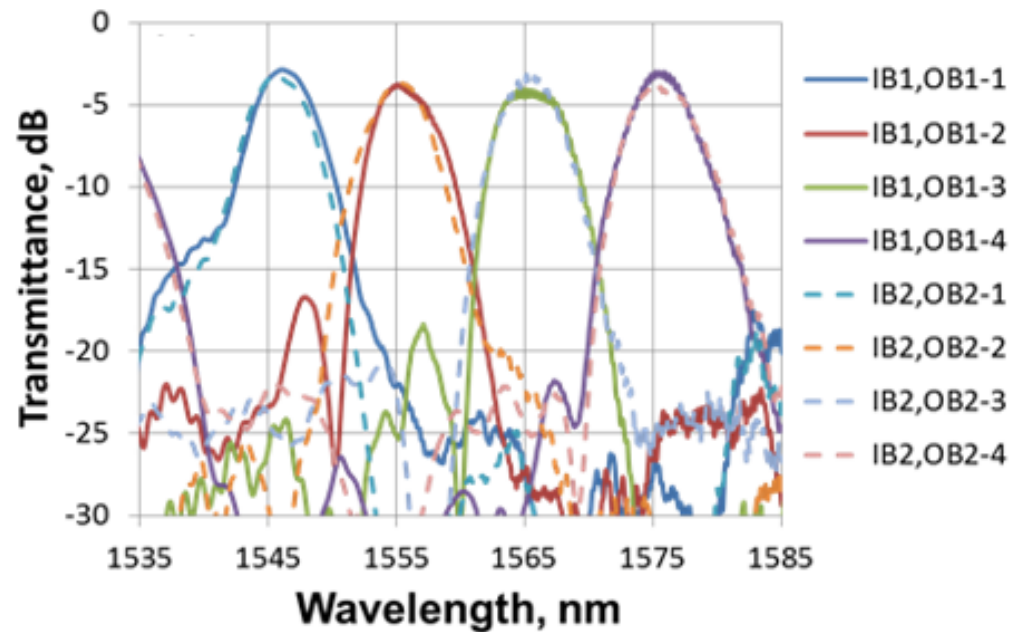
Thermal phase shifters

M. Nedeljkovic et al., IEEE Photon. Technol. Lett., vol. **26**, pp. 1352-1355, 2014.



Case study 1: Bidirectional angled MMI

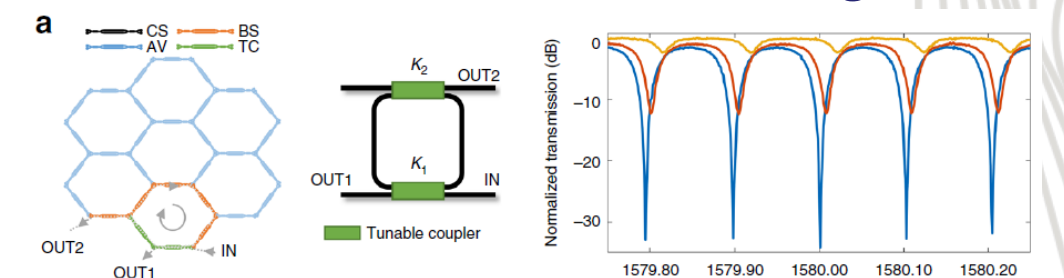
- Wavelength division multiplexing (WDM)
- Fabrication tolerances affect transmit and receive with same error



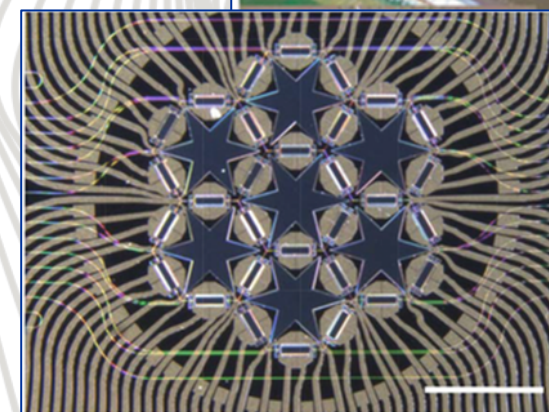
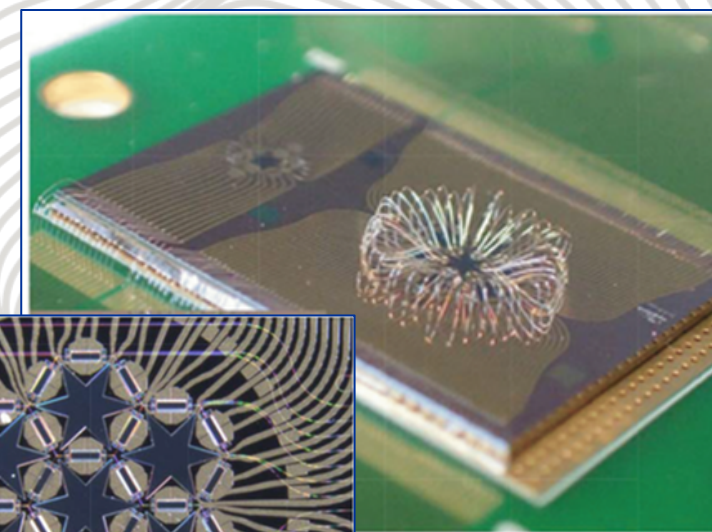
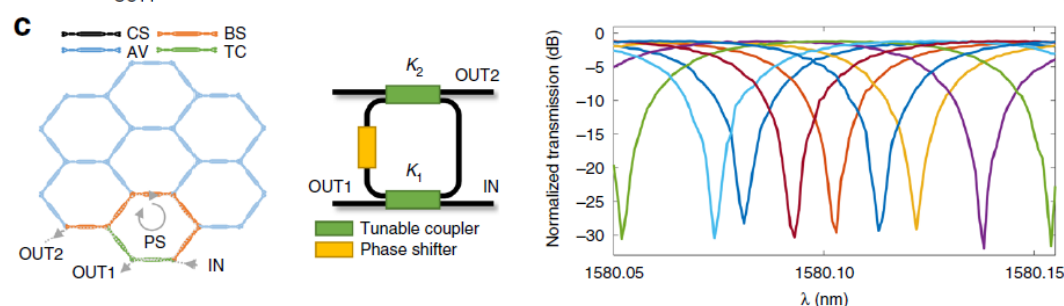
Case study 2: Programmable circuits

- Inspired by electronic FPGA
- 2D photonic waveguide mesh
- Demonstrated over 20 functionalities using the same mesh

Function 1:
Ring resonator

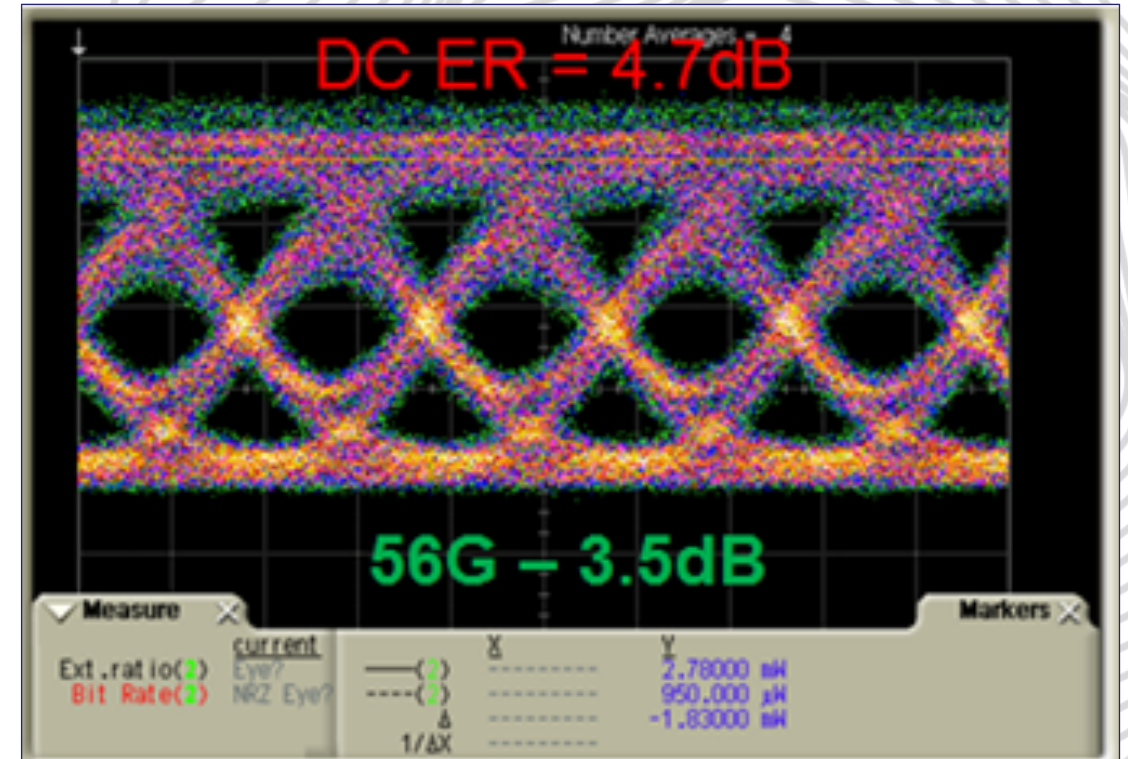
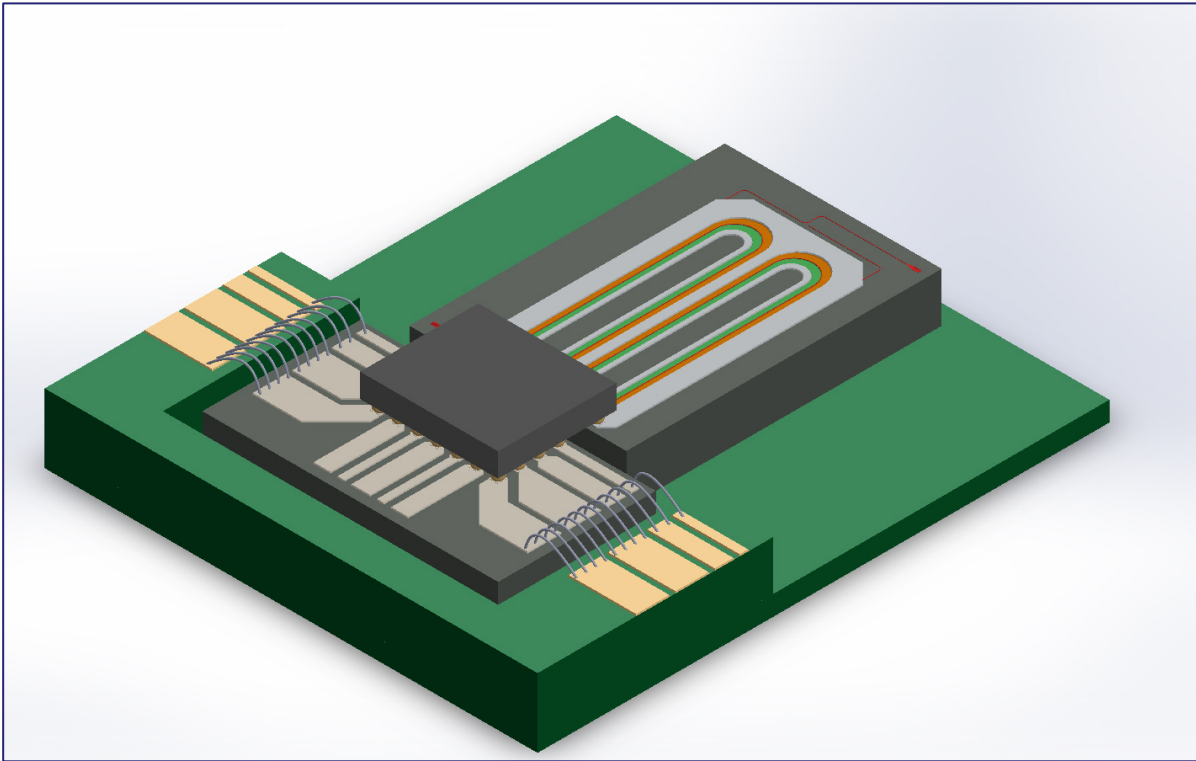


Function 2:
Ring resonator with
phase shifter



UNIVERSITY OF
Southampton

Case study 3: O-band modulators





www.cornerstone.sotonfab.co.uk