

Hyperscale use cases, challenges and case study for heterogenous integration

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Agenda

End User Use Cases

Challenges overview

Case Study: Packaging Deep Dive

Next Steps





Universal use cases that are drive technology



Recognition

Mining

Build identification models by machines of real world

Recognition is the "what is" and create a canonical representative model

Requires training!

Search instances of the model in the sea of data

Mining is searching across all forms of data (e.g., Image, text, video, logs etc.)

Requires inference!



Fundamental use cases have recurring theme of recognition, mining and synthesis for learning and knowledge creation



Synthesis

Creating new instance of models where one does not exist

Synthesis is creation by machines of new ideas

Requires multi-modality, GANs!



Data Centers are...

STORAGE

COMPUTE

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Data Centers are...

STORAGE

COMPUTE

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Data Centers are...



COMPUTE

NETWORK

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Data Centers are evolving



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What are the dominant serving workloads?

Current and emergent

- Ranking and recommendation
 - News feed and Search
- Computer Vision
 - Image classification, object detection
- Language
 - Translation, speech recognition
- Multi-modal
 - Metaverse synthesis







- Strains compute, memory, storage, and network
- Speed of innovation requires high-performance and flexibility
- Efficiency requires HW/SW co-design

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Chiplet Use Cases

Chiplet marketplace offerings

Compute

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Network and IO





Memory





Key Benefits:

- Reduce material COGS through • higher yielding silicon
- Accelerate TTM & reduce NRE through chiplet IP reuse
- Enable new capabilities: ullet
 - Scalability, composability •
 - Perf/W Efficiency •
 - High density •
 - Isolation (perf, pwr, security, fault) • and partitioning capabilities

How It All Started...



Data Center Growth



Scale & Disaggregation



Challenges across the chiplet technology stack

Co-design expands across all of these dimensions



Silicon Co-Design

Chiplet Packaging Options

Complexity



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Areas for Innovation / Partnership

Scale Up - "Advance"



Performance

Advanced packaging, 2.5 & 3D Smaller process nodes High power thermal solutions







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Scale Out - "Expand"

Efficient fabric interconnects (Optical & Electrical) Flexible configurations with standard interfaces

Distance

Industry Challenges for Open Chiplet Adoption

Cost Reduction

- Re-use existing silicon
- Reduce R&D cost _
- Fast product SKU development

Standardization

- D2D interface supporting variety of packaging options
- Pin templates for multi
 - vendor integration





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Fast Innovation

- Ability to innovate at different process nodes – no soup to nuts in 3nm
- Impact operation costs via reusability
- Adding 3rd party IP into existing IP library

Operations

- Agreed upon KGD tests to allow foundries to ship to OSATs for assembly and integration
- Common security protocols across _ supply chain