Community Led Hyperscale Open Innovation

OCP – ODSA Project

OpenFive Die-to-Die PHY & Controller for Chiplets

openfive SiFive

OpenFive, SiFive Business Unit

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About OpenFive

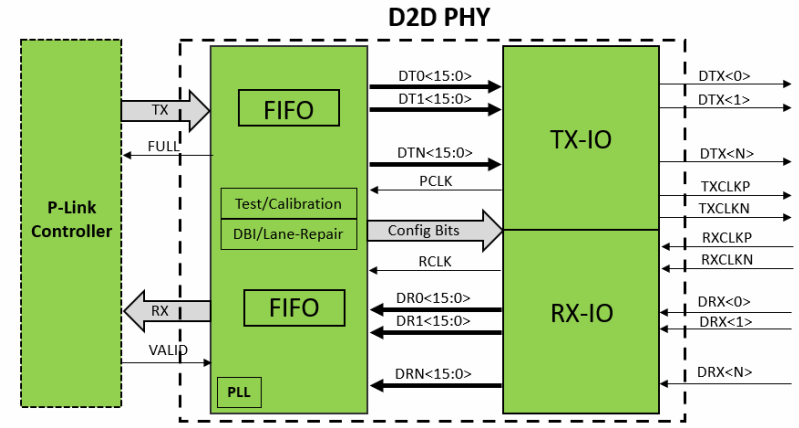
- OpenFive is Custom Silicon Solutions provider with Differentiated IPs
  - 350+ Tape-outs, with advanced technologies up to 5nm & beyond
  - Differentiated IP Subsystems for Connectivity, Memory and Chiplets

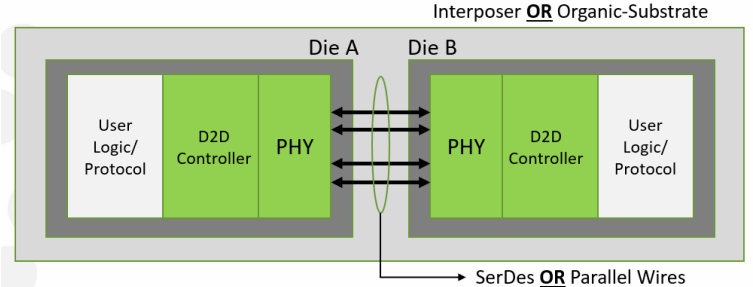
- Connectivity solutions to improve Yield, reduce Power and increase the Throughput between the chips/dies in the most Cost-Efficient ways
  - Over 10+ years and 100+ licenses in chip-to-chip Interlaken and 2.5D interposer based HBM solutions
  - Same technology in HBM and Interlaken is applied to OHBI/BoW PHYs and Controllers

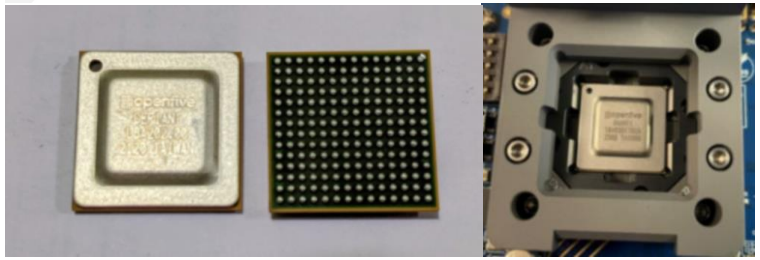
- OpenFive is an early member of OpenHBI workgroup under ODSA
  - Joined in early 2020 and participated in OpenHBI 1.0 Specifications
  - https://www.opencompute.org/documents/odsa-openhbi-v1-0-spec-rc-final-1-pdf

Die-to-Die IP Subsystem : PHY

- PHY Compatible to OpenHBI v1.0 at 8Gbps
  - IOs are optimized to support BoW and other PHYs
    - By changing the bump maps and packages
- D2D Subsystem including PHY and Controller
  - Speed : Up to 16 Gbps/lane (Package/Distance trade-off)
  - Power : Less than 0.5pJ/bit
  - Throughput : ~3.2Tbps/mm using Quad PHY slices
  - Latency : Less than 5ns, Tx + Rx PHY latency
  - Density : Supports 55u bump pitch for advanced packages
- Proven on Silicon!
  - 7nm silicon has 2 die back to back on advanced package
- More information on our website :
  - https://openfive.com/die-to-die-ip-subsystem/

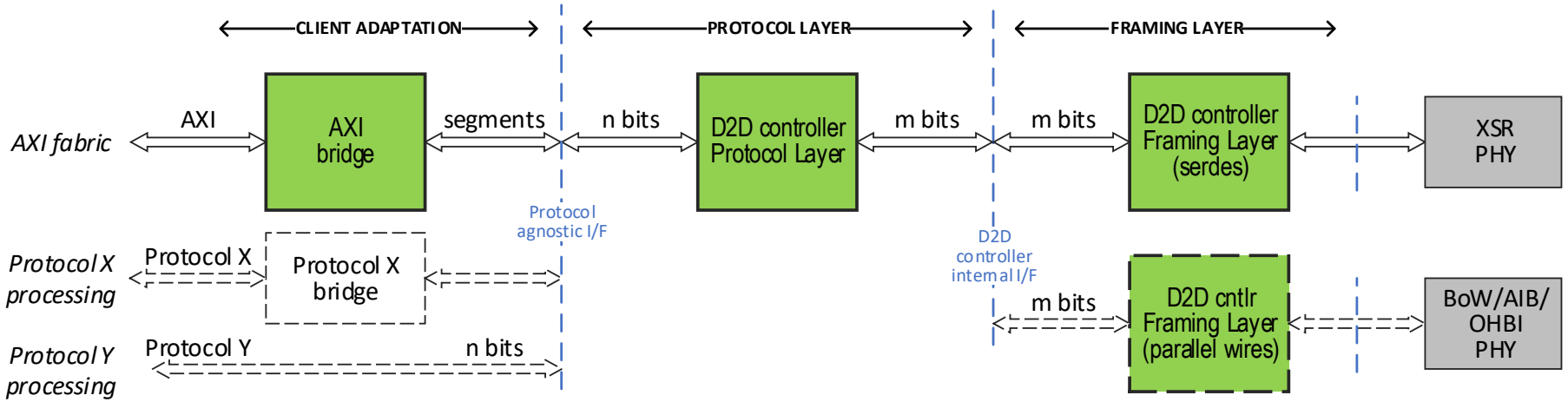






OpenFive 7/5nm silicon validation vehicles

Die-to-Die IP Subsystem: Controller



Client Adaption

- Adaption of Client signal to Controller Interface
- Support for AXI4, CXS, TL, xGMII etc.

Protocol Layer

- End to End error free delivery
- Flow Control
- Optional Re-transmission

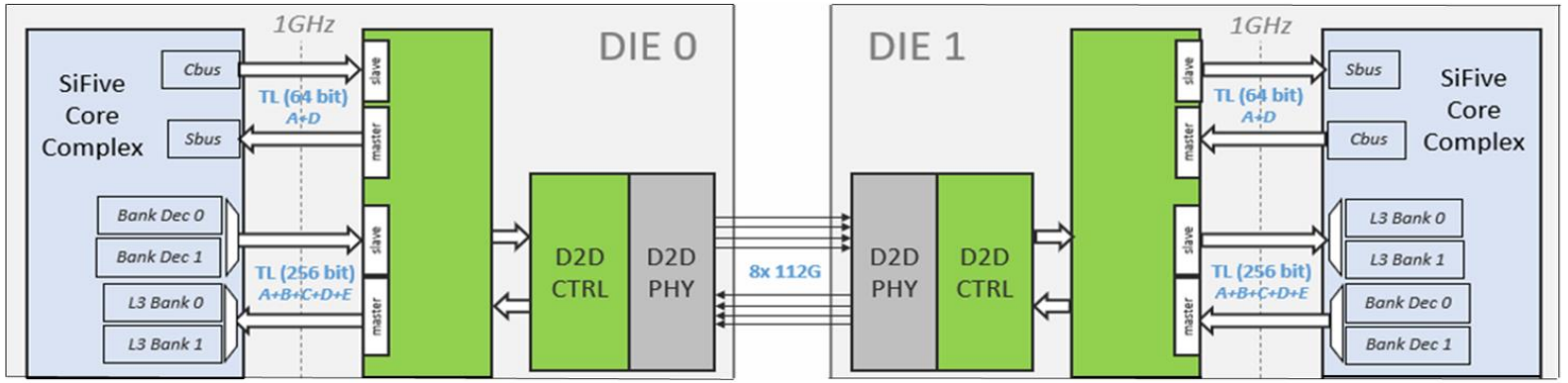
Framing Layer

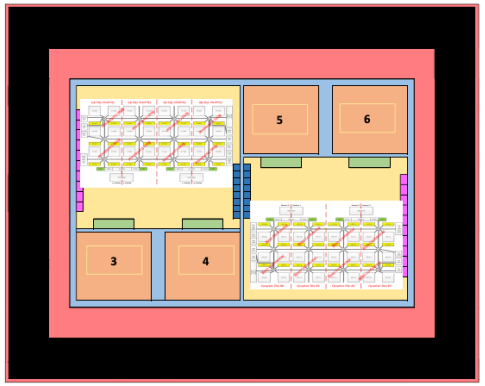
- Function depends on Parallel wires or SerDes
- Lane alignment/De-skew
- Optional FEC Engine

Supports XSR, BoW, OHBI and other PHYs

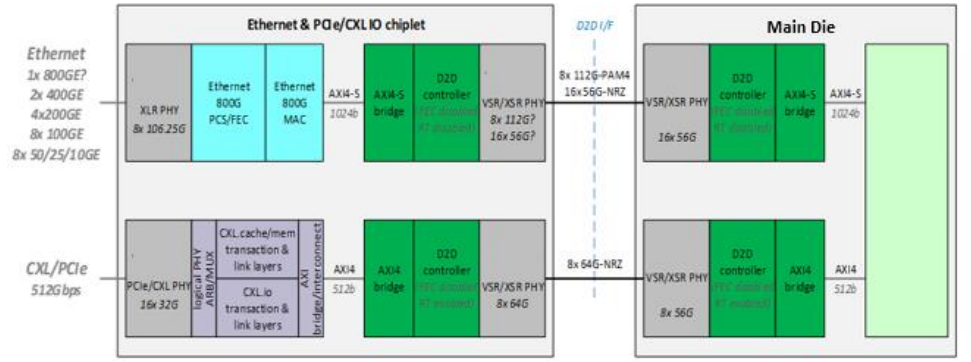
OpenFive Customer Chiplets Using Die-to-Die

CPU Chiplets





GP-GPU Chiplets



IO Chiplets

What is Next

- Customers requiring connectivity to specific CPU/GPU -
  - Multiple PHY interfaces exist such as XSR, OHBI, BoW, UCIe, NVLink etc.
  - OpenFive as customized IP & Silicon provider will continue the effort to support ALL
- Customers requiring heterogenous die disaggregation -
  - Closed box systems are agnostic to particular interface
  - We are already supporting them today : https://openfive.com/die-to-die-ip-subsystem/
- Going forward
  - Collaborations between Foundry, IP/Silicon and OSAT providers taking various types of Chiplets (CPU, IO and Heterogenous) to the next level of optimization
- Q & A