POC Requirements and use cases

ODSA Project Workshop

March 28, 2019

Consume. Collaborate. Contribute.

POC Requirements and use cases

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Why do a Proof-of-Concept

- Learn
- Reduce Risk
- Convince Skeptics

POC Unique Challenges

- Problem has to be hard enough that you expose the issues
- Solution has to be easy enough that you can do it fast

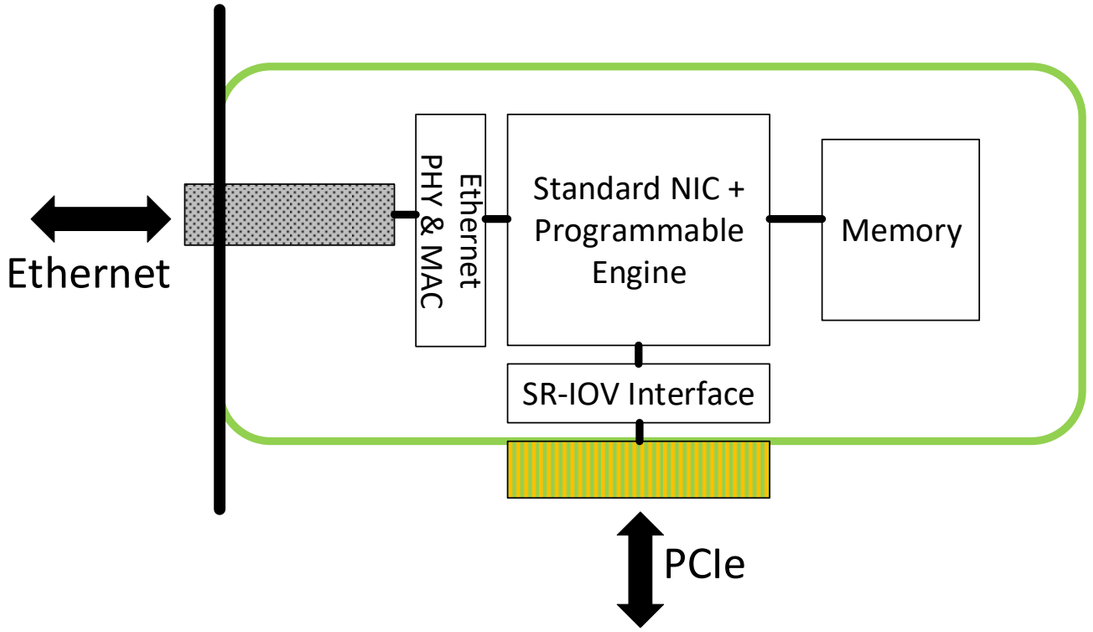
Multiple dimensions of POC

- Architectural
  - Validate interfaces protocols
  - Evaluate performance issues
  - Develop software programming models
- Physical
  - Explore chiplet integration and packaging
  - Validate power distribution
  - Develop high-speed I/O solutions
- Business
  - Force information sharing at a bare die-level
  - Exposing issues of sharing sensitive business metrics
  - Validate risk and value sharing models

Ambitious POC

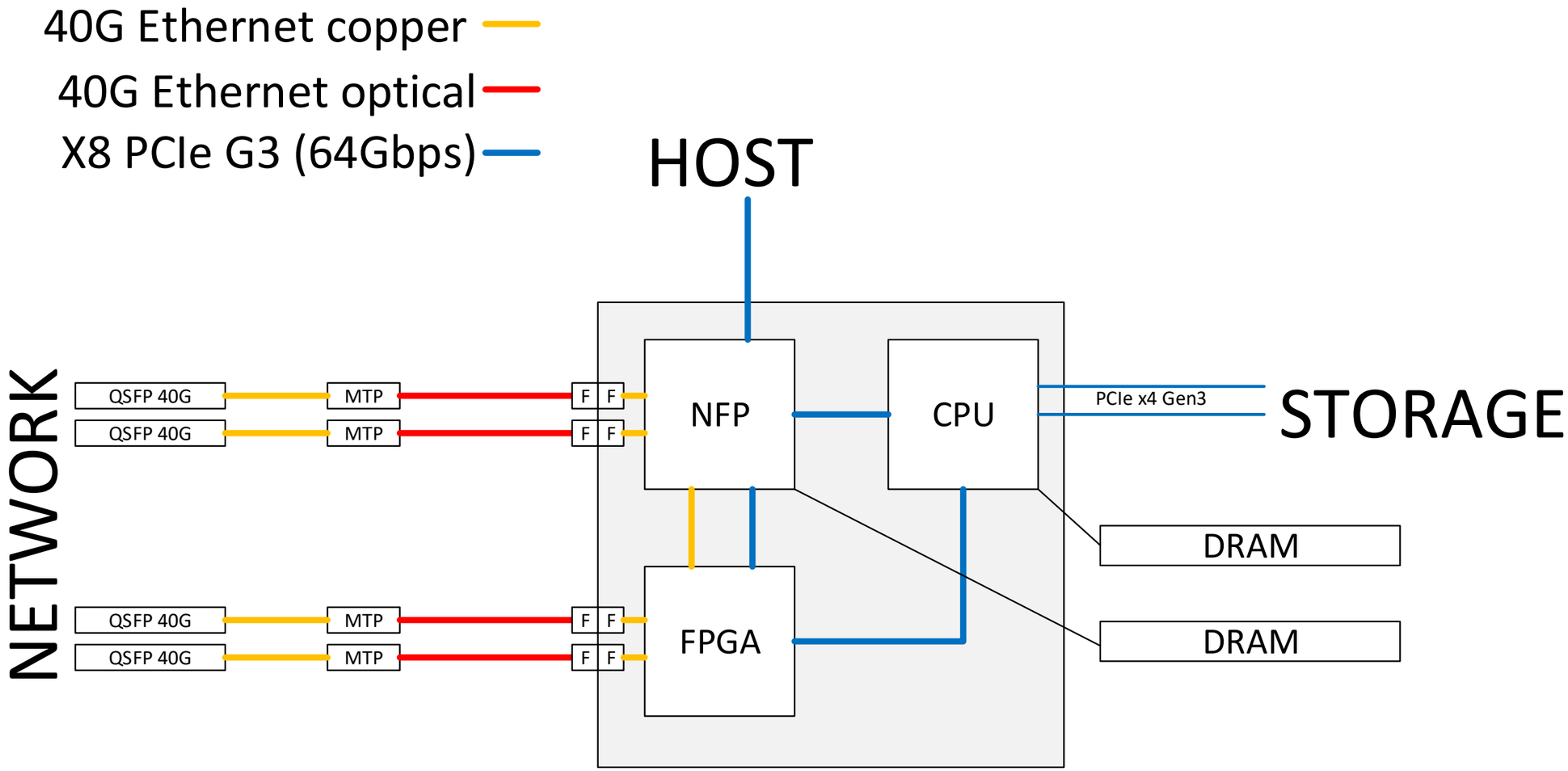
- Smart Network Interface Card
  - A NIC that offloads work from the host CPU
  - Virtualization, SDN and NFV moved more networking tasks from hardware to software on the host. . .
    . . . now we need to hardware accelerate those software tasks
  - Good candidate for POC because everyone wants a domain-specific accelerator, but lots of custom requirements and configurations
- To make it fun lets also cover Computational Storage Solutions
  - Another important category of domain specific accelerators
  - Leverage some of the same connectivity building blocks of Smart NICs

Smart NIC



- Programmable Engine Task
  - Match based on Src/Dst/transaction (go back to host software if no match)
  - Security checks
  - Optional TCP/IP and HTTP processing
  - Potentially simple substitutions in header
  - Potentially encrypt/decrypt
- Programmable Engine Requirements
  - Highly flexible because protocols and tasks change over time
  - Want low-latency and high-throughput
- Programmable Engine Implementation
  - Some combination of Configurable ASICs, CPU cores, and FPGAs
  - Configured as (a) part of NIC, (b) sidecar to NIC, or (c) bump in wire before NIC

POC



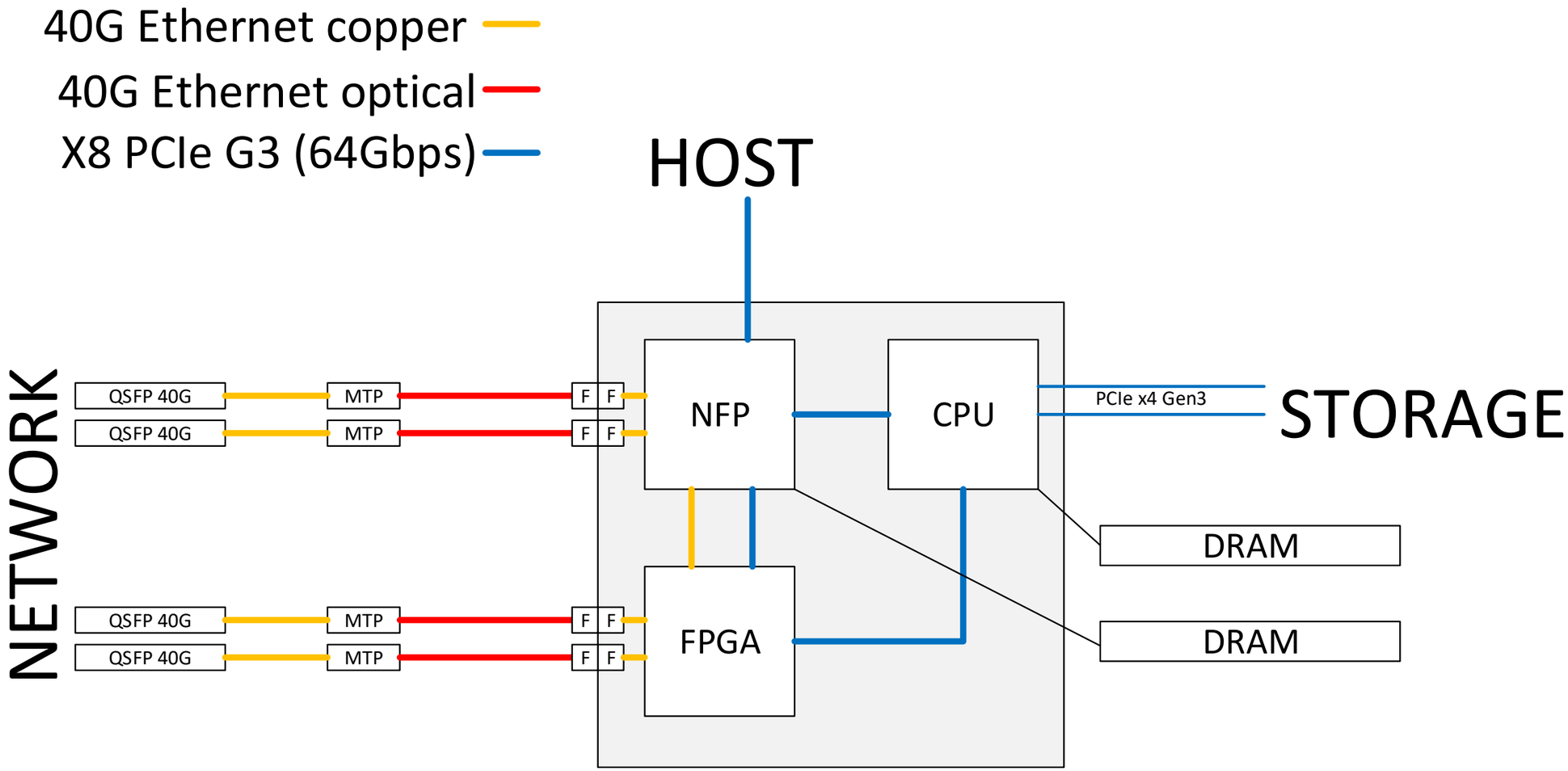
Major Units

- Network Processor
  - For networking support
- CPU module
  - For control plane
  - Storage connectivity
- FPGA
  - For data plane

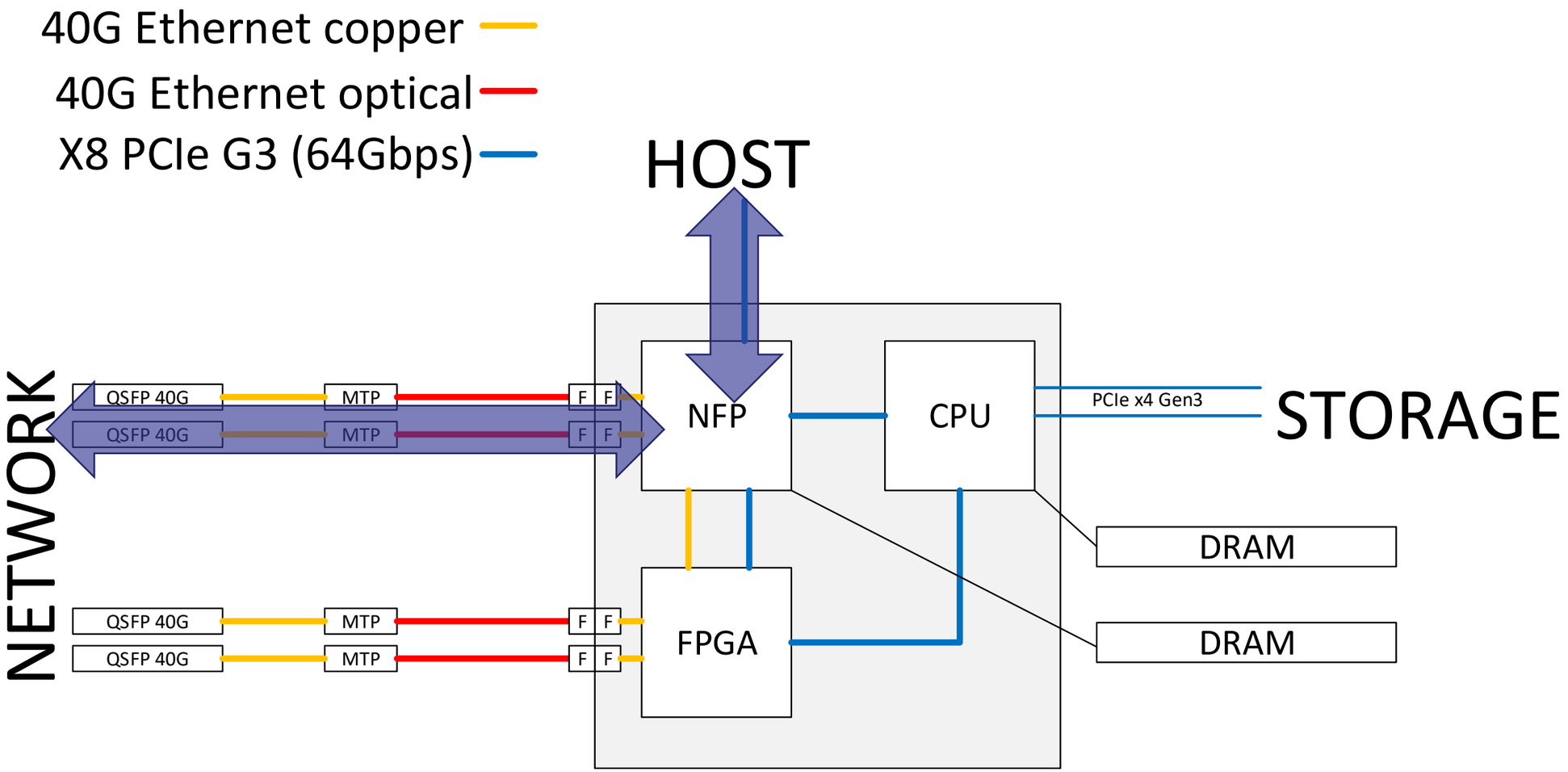
Connectivity

- PCIe Gen3 x8 (64 Gbps)
  - To host
  - To represent chiplet link
- 40G Ethernet
  - Performance match to PCIe Gen3 x8
- DDR3 memory

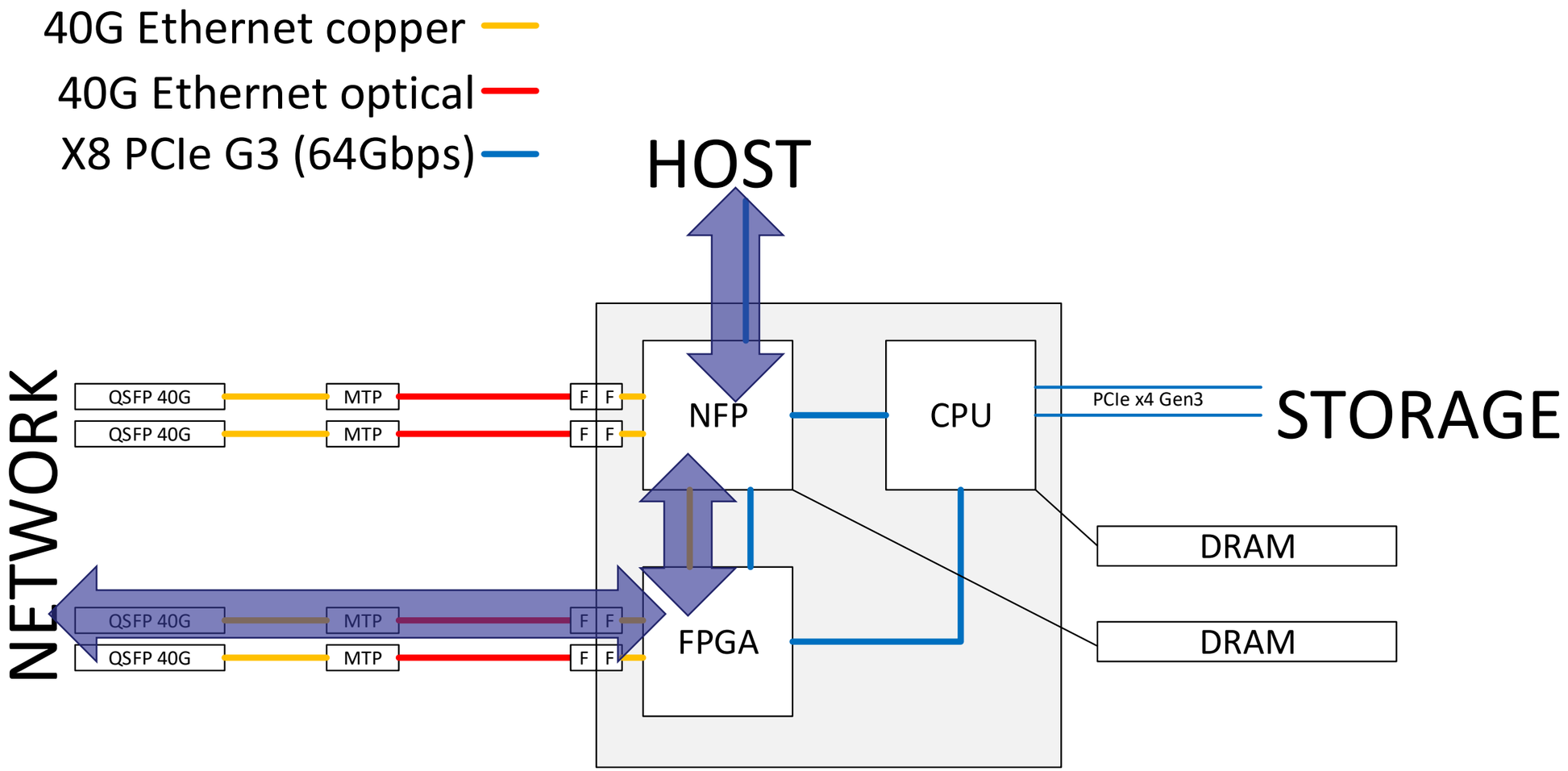
POC



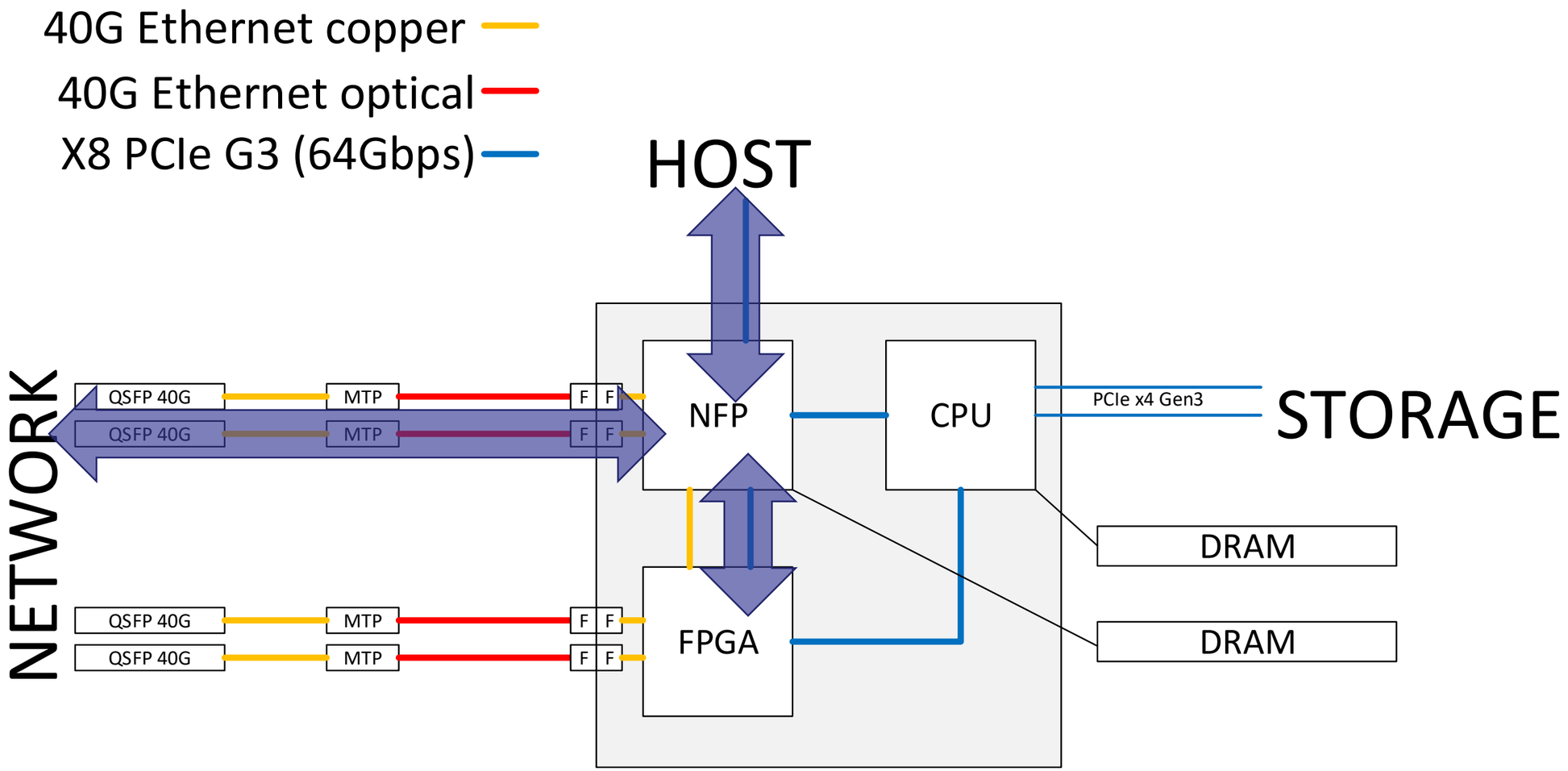
POC - NIC



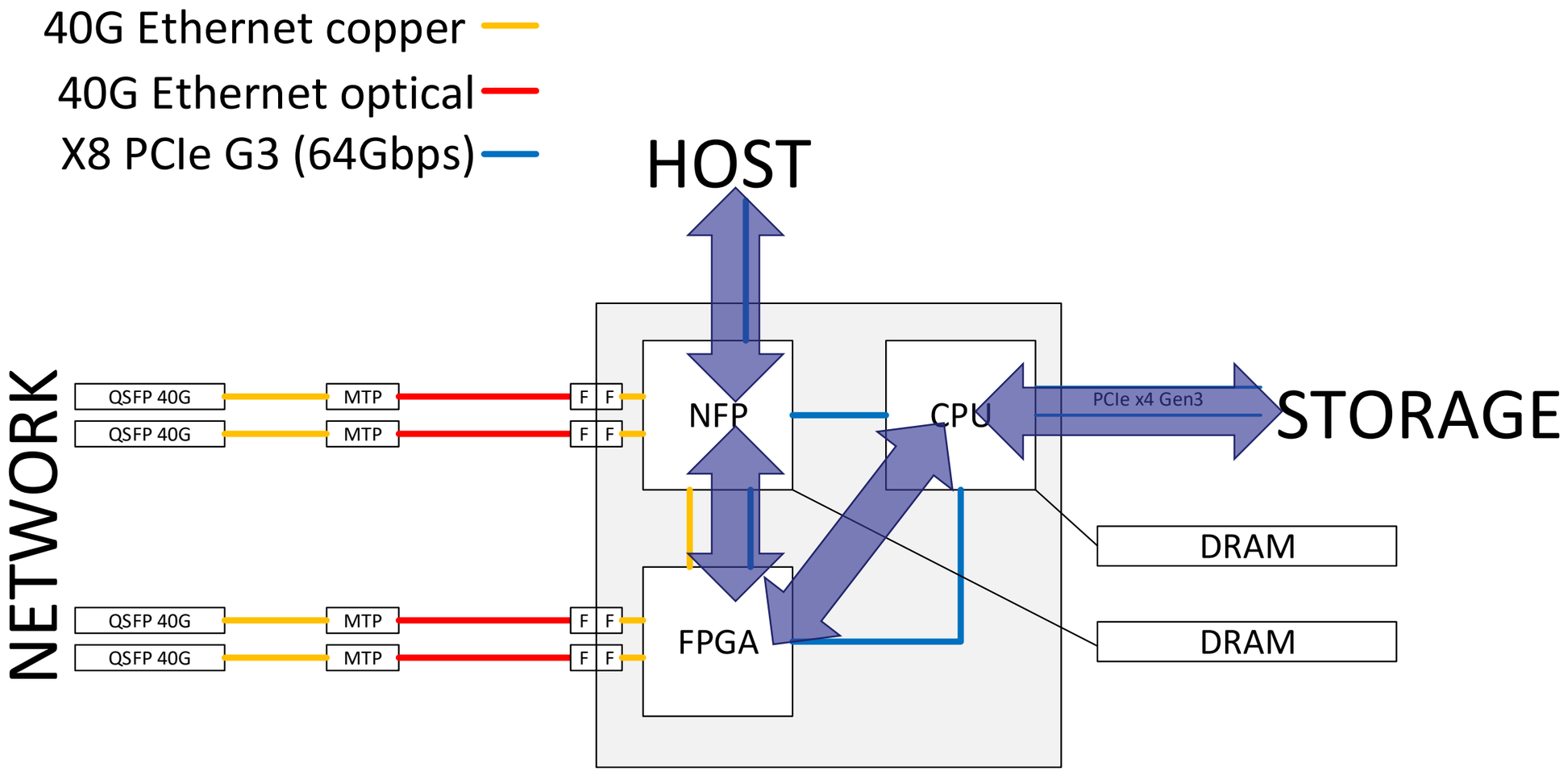
POC – Bump-in-the-wire SmartNIC



POC – SmartNIC w/ data accelerator



POC – Computational Storage



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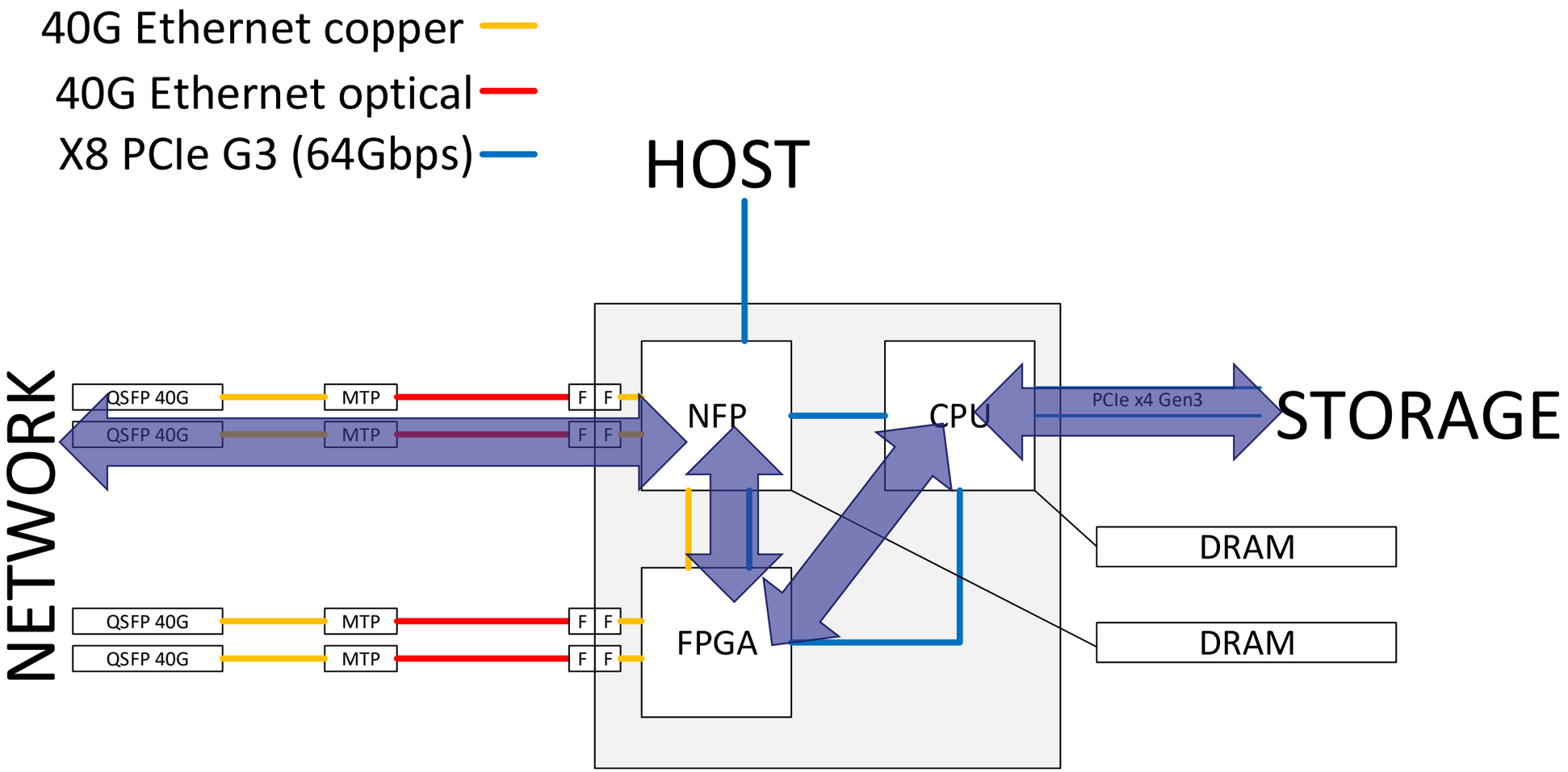
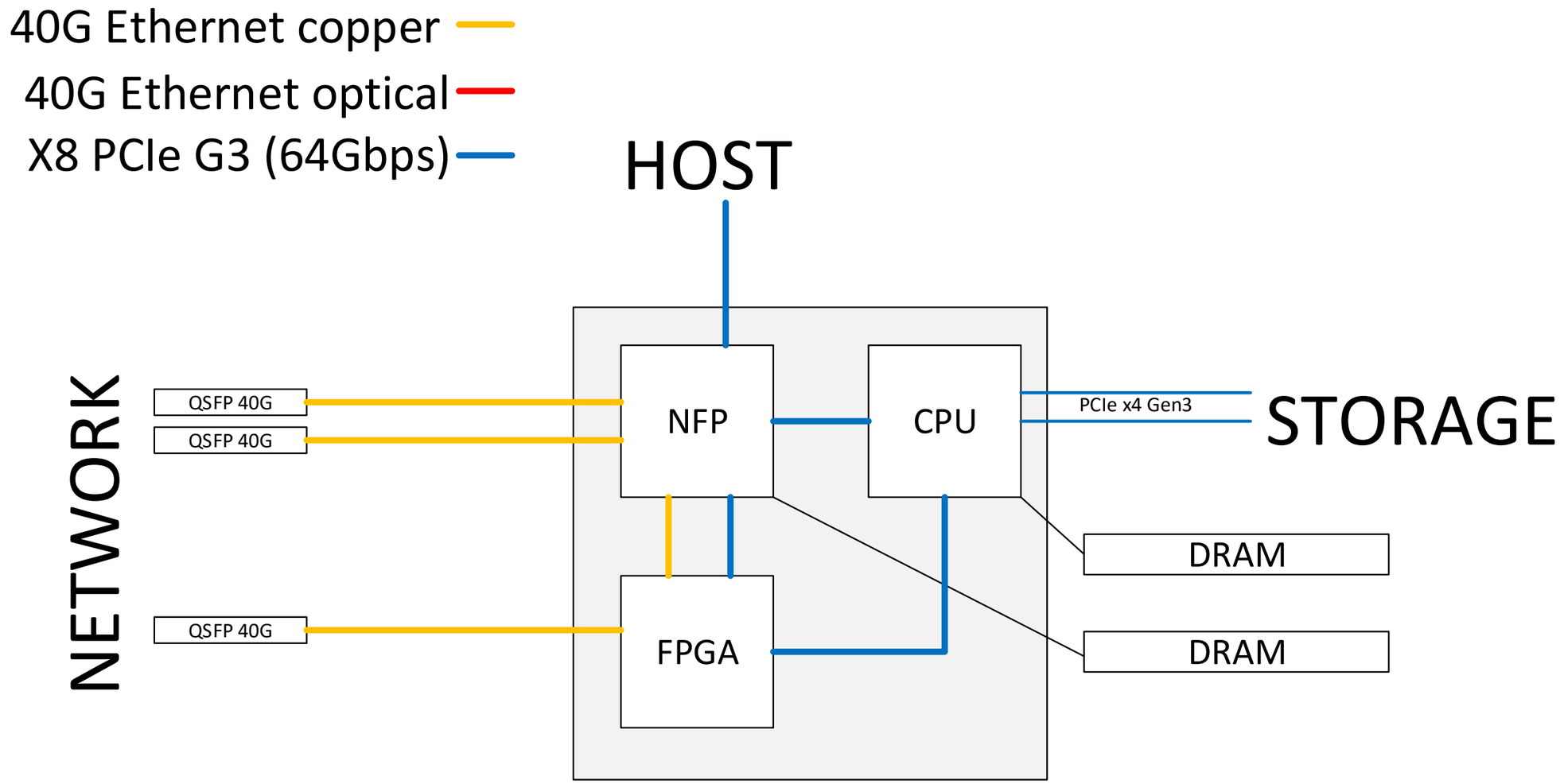
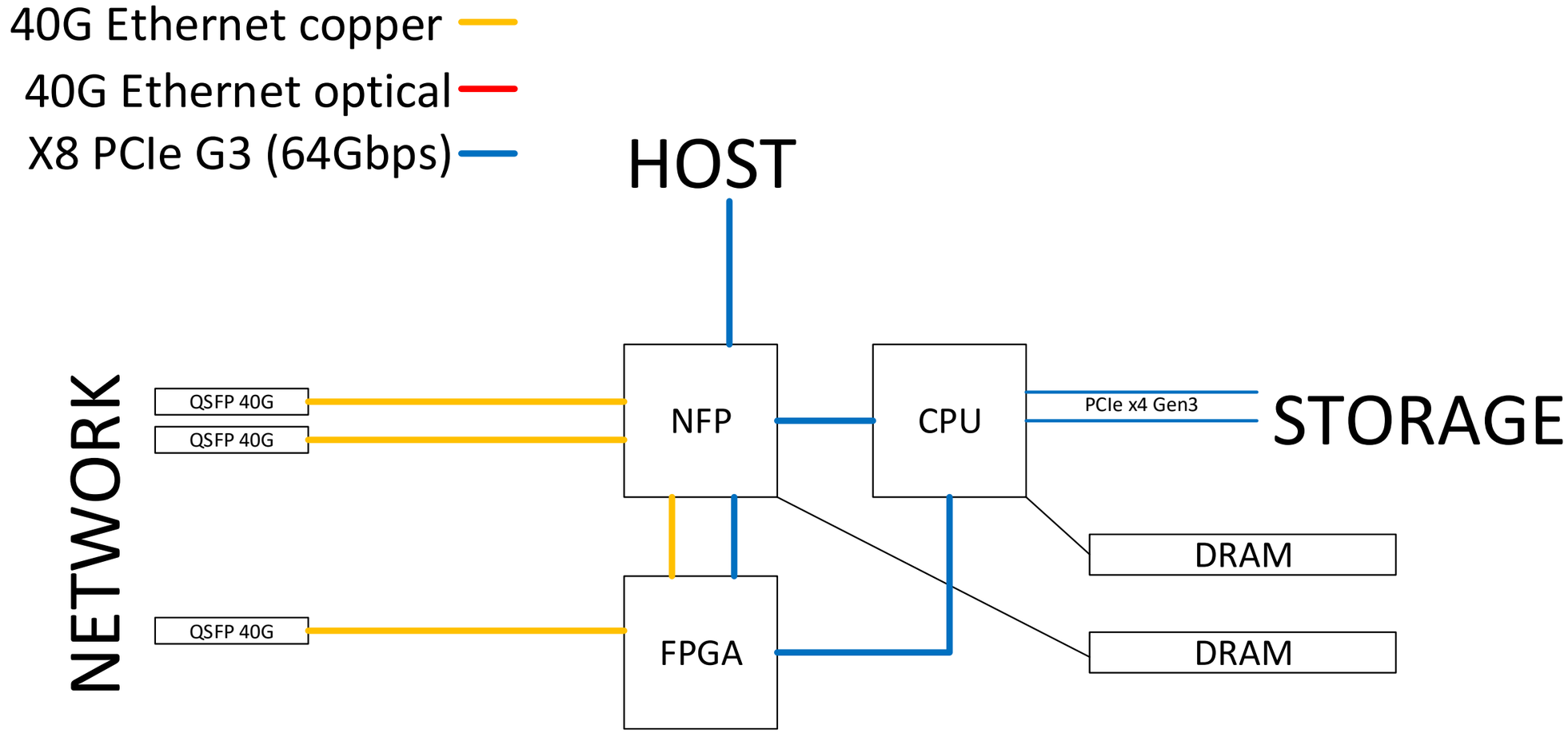


POC - Alternative



POC – SW Dev System



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THANK YOU

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