The Case for a Universal Chiplet Revolution

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Google
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(With thanks to: Amber Huffman, Amin Vahdat, Dave Patterson, Martin Maas)

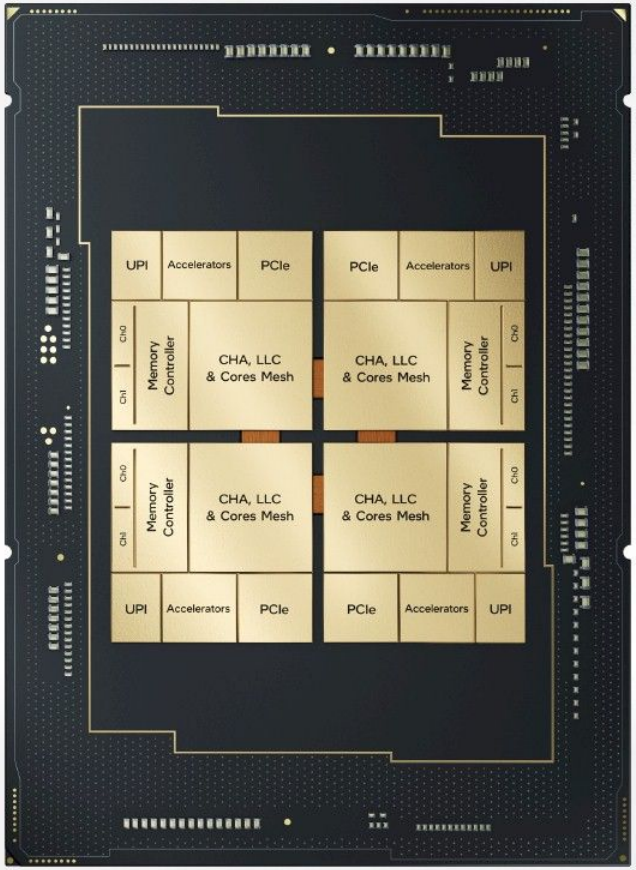
What is a Chiplet?

Historically, die=package=chip.

- Die = transistors+wires
- Package has pins, cooling plate, mechanical.

Recently, >1 die in a package/chip; die=chiplet.

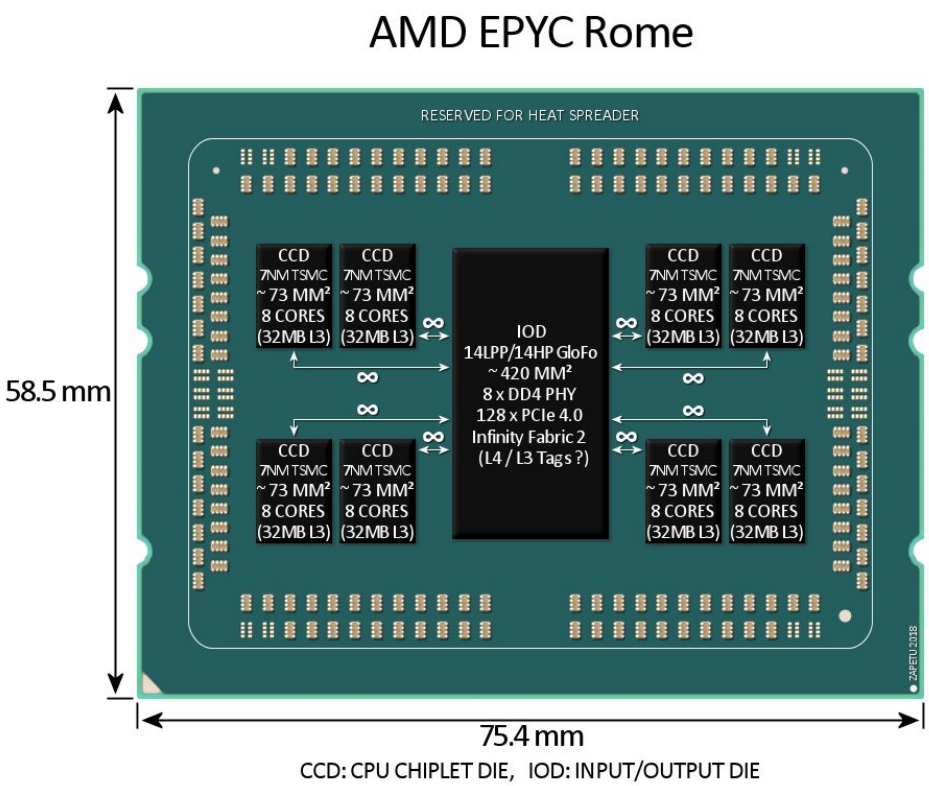
- TPUs/GPUs put >33 dies/package
- AMD has 4 “compute” dies + 1 “I/O” die/package.
- Intel’s new SKL parts use four identical dies.



Intel Skylake package, showing four symmetric chiplets combined to build one x86-architecture chip.

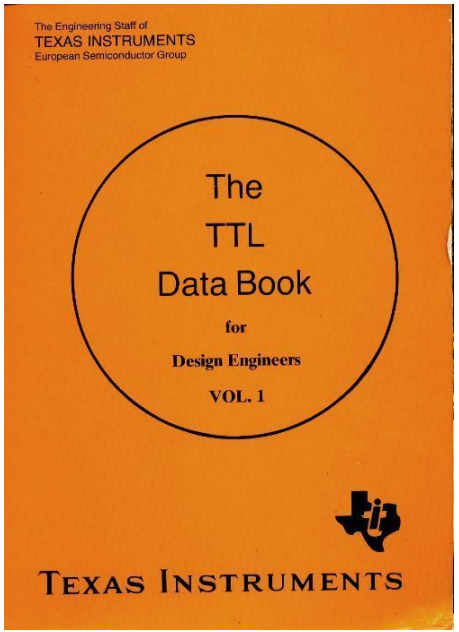
Bespoke Chiplet Solution

- As Moore's Law diminishes, semiconductor wafer costs rising faster than performance gains from latest technology
- Instead of increasingly larger chips in latest technology, use clever packaging and smaller chips, some in older technologies
  - AMD EPYC Rome: 1 I/O chiplet in 12 nm + ≤ 8 core complex chiplets in 7 nm
  - Intel Sapphire Rapids: 4 chiplets, each with a subset of cores and IOs
- Save money (smaller chips have higher yield, some use old tech) *and* allows bigger systems (more transistors)



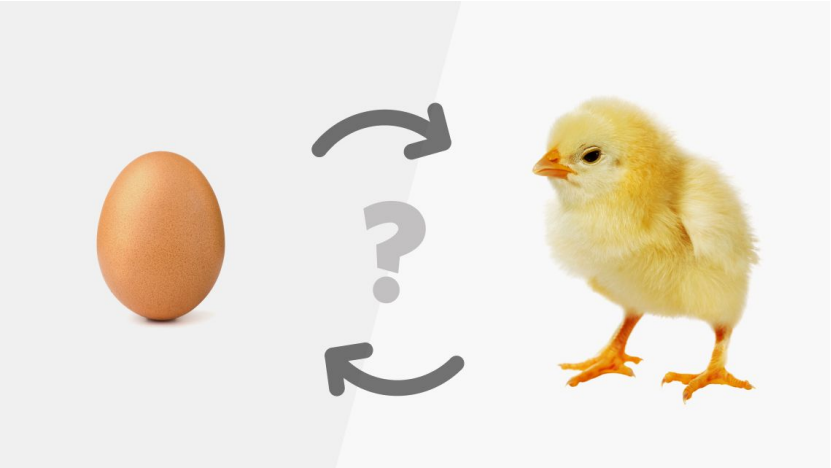
A Universal Chiplet Solution?

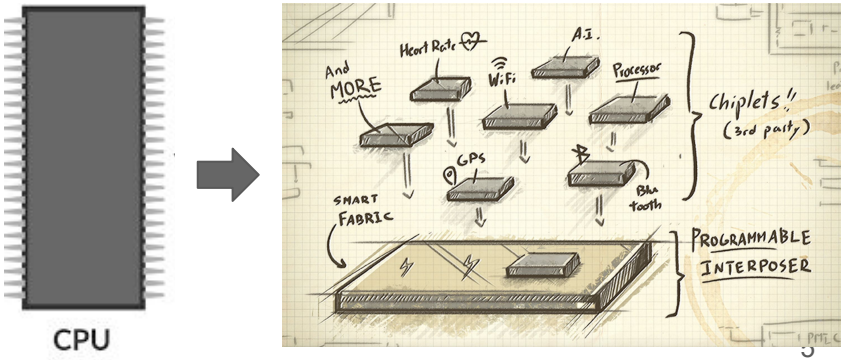
- Could industry standardize on chiplets for reuse across many product lines, thereby increasing their volumes and lowering relative mask costs?
  - Early days of integrated circuits had a standard
  - Texas Instruments TTL catalog
- To be universal, must be able fab anywhere, package anywhere, buy chiplets from anywhere
- Standardization Challenges:
  - Inter-die electrical interface standards
  - Inter-die communication protocol standards
  - Power distribution layers and packaging technology standards
  - Dimensions of standard chiplets
    (like TI 7400 TTL 14-pin and 16-pin packages)
  - Management standards
  - Verifiable security standards



Chicken versus Egg Problem

1. Chiplet suppliers won't manufacture chiplets if there is no demand
2. Customers won't design using chiplets until they are available for purchase
3. Even if one company offered a chiplet solution, customers don't want to be locked into a single source for chiplets and their packaging





How can we break the Chicken vs Egg

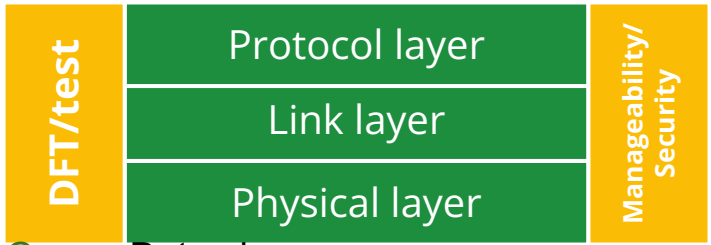
Many of us are building and consuming chips.

- We have many **common needs**: PCIe interfaces, HBM and other memory controllers, interconnect, CPU core clusters, etc.
- Allows chiplet consumers to focus on core competencies.
- Interoperable chiplet standards will help **all** of us.

Google Contributions

- Google and silicon

- Google has been active in the chiplet community to enable standardization
  - Published a blog to further the chiplet ecosystem; board member, OCP
  - Helped define and contribute data plane standard (oHBI) to OCP
  - Committed to be a board member of standard (UCIe)
  - Spearheaded an open source *control plane* (OpenChiplet)

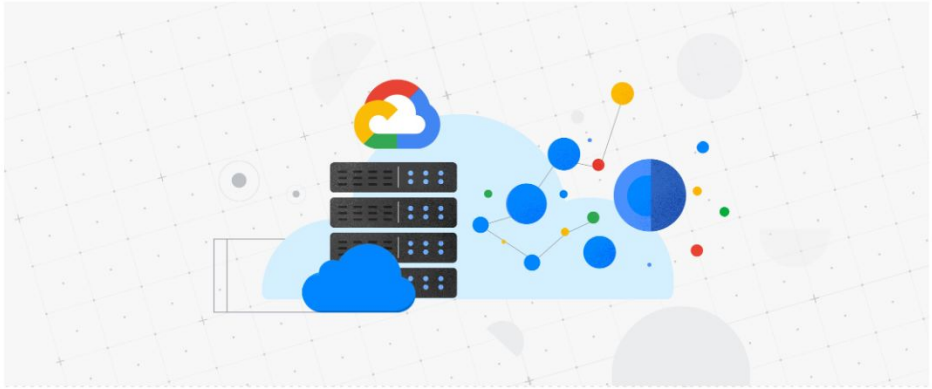


Green: Data plane
Orange: Control plane

Google blog

SYSTEMS

A chiplet innovation ecosystem for a new era of custom silicon



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March 2, 2022

As traditional Moore's law improvements slow down, we are now turning to custom chips to continue improving performance and efficiency. Innovations like Google's Tensor Processing Units (TPUs) and Video Coding Units (VCUs) have been incredibly valuable at sustainably meeting the growing demand for machine learning and video distribution services, and we expect to see additional custom chips that meet the emerging needs of our customers and users.

But building custom chips is a complex and costly endeavor. In particular, the semiconductor industry faces a key challenge. Each successive generation (technology

Google Contributions : OpenChiplet Specs chiplet marketplace

Full Stack : Software to Packaging

Layered Architecture : Defines an interoperable, multi-source chiplet product

Standard Interfaces : Open-source or Industry standard

Secure : Security built-in from Day 1

Programmability : Flexibility for customization by end-user or chiplet provider

Open : OpenChiplet Specification is published as a Google project on GitHub

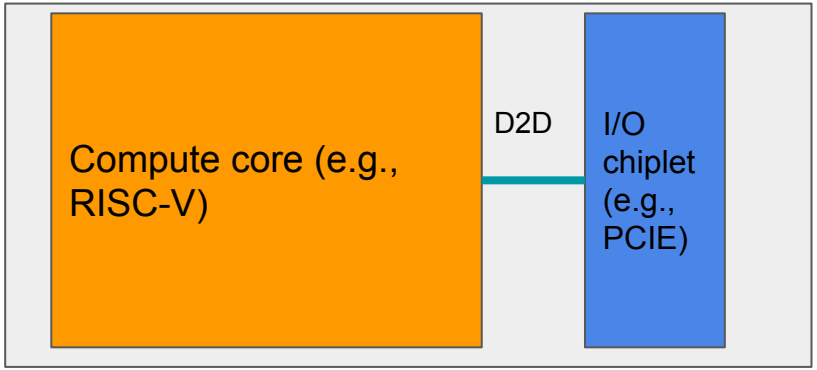
go/open-chiplet

https://github.com/google/open-chiplet

Let’s start talking!

- We would like to see chiplet marketplace ASAP
  - Standardization is just a means to the end
- Let us define the common needs with details
  - Common needs ⇒ more designs ⇒ more wafers ⇒ more robust silicon market.
- Build reference platforms (more later)
- Other ideas…
  - Is there a role for policy, or government to help out?
  - CHIPS Act?

Google Contributions & Call to Action



A reference platform to test out full stack (SW down to packaging) over a universal chiplet interface

Ability to switch different chiplets for functionality, performance, power etc. needs

We believe Chiplets are critical for future systems and invite feedback from the community on

1) what such a reference platform should look like,
2) what functionality should be part of it,
3) how Google can further a chiplet marketplace.

Takeaways

Chiplets are not just a technology—they also will enable a new era of interoperability, specialization, and win-win collaboration.

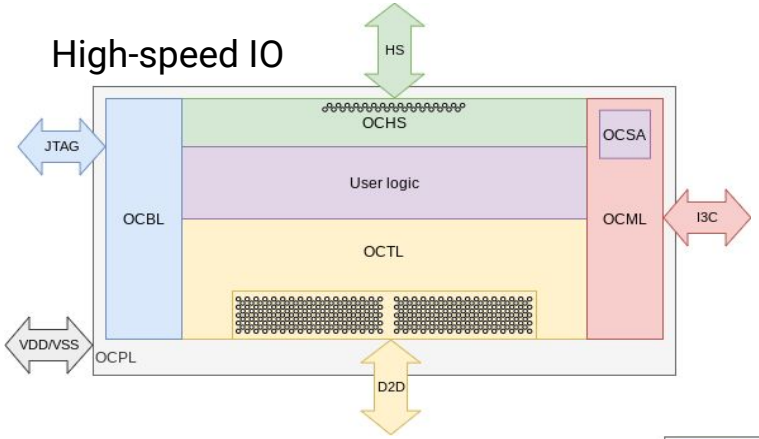
Getting there will take work, possibly at many levels: standards, companies (foundries, manufacturers, hyperscalers, and users), academia, and government.

The market won’t necessarily get us there by itself—let’s work together!

Appendix

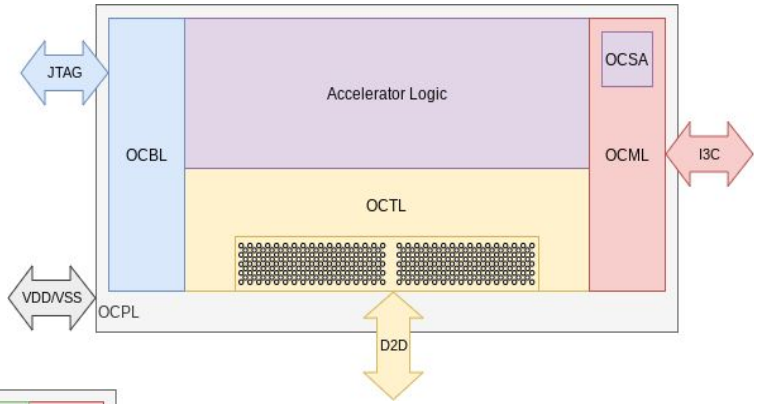
Many markets… One OpenChiplet Standard

High-speed IO



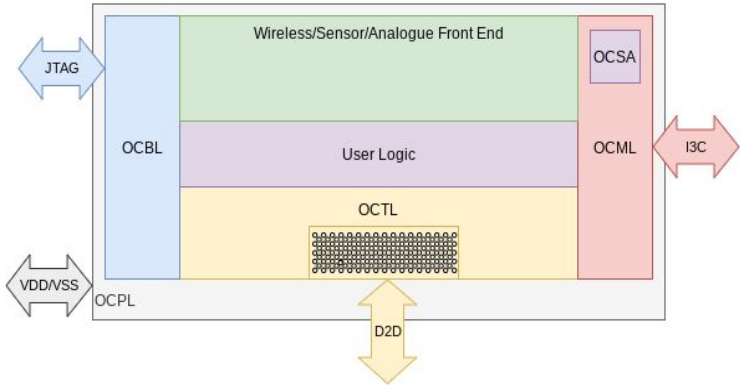
OCSA - Security Agent
OCML - Management Layer
OCBL - Build Layer
OCPL - Power/Electrical Layer

Accelerator/Coprocessor/Memory



OCTL - Transport Layer*
OCHS - High Speed Layer*

Analog/Mixed Signal



UCIe details

- UCIe has brought together leading foundry vendors (TSMC, Samsung, Intel) + OSAT leader + Si / IP leaders + Cloud/Hyperscale leaders to provide a clear path forward.
- UCIe already has more than 20+ Contributors since its announcement two months ago (on March 2)
- UCIe has a full Phy, Link, Protocol solution. This goes beyond a D2D interface, like with OpenHBI or BoW.
- UCIe will pull together the form factor, manageability & security aspects over the next 6-12 months.