Open. Together.
CHIPSEC on Non-UEFI Platforms

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CHIPSEC History

- CHIPSEC is a framework for analyzing the security of PC platforms including hardware, system firmware (BIOS/UEFI), and platform components.
- Originally developed by Yuriy Bulygin (@c7zero)
- First version of CHIPSEC was released in March 2014 at CanSecWest
- Currently used by firmware developers, system validation and system integrators

https://github.com/chipsec/chipsec.git
Current CHIPSEC Assumptions

- Runs on an Intel based platform
- Firmware has a threat model compatible with UEFI
- All platforms require the same level of security
Threat Model Assumptions

• **Configuration Settings**
  Program and lock registers when possible
  Minimize the use of non-volatile data that is updatable from OS

• **Flash Access**
  Ensure the Serial Peripheral Interface (SPI) flash can be updated in runtime
  Use the System Management Mode (SMM) or Protected Range (PRx) register to protect SPI flash
  Verify flash programming matches guidance from Intel

• **Others…**
So What’s the Problem?

- **Different methods to secure the platform exist**
  - Read Only (RO) backup firmware with forced recovery
  - Physical presence for update
  - RO firmware

- **Platforms have different security requirements**
  - Open Development System (cannot be locked down)
  - High Assurance Critical System (very, very locked down)

- **CHIPSEC modules do not comprehend different platforms requirements**
  - This means security engineers may find ‘false positive’ issues if your threat model is not well understood and documented.
Processing Results

• **Know your platform**
  Understand the security assumptions of your platform

• **Know your security requirements**
  Is physical attack part of your model?
  Are you developing or deploying custom firmware?

• **Understand why you may skip certain modules**
CHIPSEC Example

- CHIPSEC run on Chromebook in developer mode
  - Legacy Boot to Linux
  - Skylake Y processor
- Results Summary
  - Failure in `bios_wp`
  - Warnings in expected locations
  - UEFI tests skipped as expected
  - All others passed

Thanks to John Loucaides from Eclypsium for the log file.
False Positive Example in bioswp

[ ] Module: BIOS Region Write Protection

[*] BC = 0x0000008D << BIOS Control (b:d.f 00:31.5 + 0xDC)

[00] BIOSWE = 1 << BIOS Write Enable
[01] BLE = 0 << BIOS Lock Enable
[02] SRC = 3 << SPI Read Configuration
[04] TSS = 0 << Top Swap Status
[05] SMM_BWP = 0 << SMM BIOS Write Protection
[06] BBS = 0 << Boot BIOS Strap
[07] BILD = 1 << BIOS Interface Lock Down

[-] BIOS region write protection is disabled!

• Failure due to different security model being used
  SMM based protections disabled
  Configuration locked (good)
• User needs to understand that this is not a real failure
What Can the OCP Community Do?

- Require Published Threat Models for OCP Accepted Hardware
- Discuss updates to CHIPSEC to support different threat models
  - Open issues on GitHub if you find problems
  - Looking for community guidance on implementation
- Create or update modules to support multiple threat models
- Submit issues and pull requests on GitHub

https://github.com/chipsec/chipsec
Get Involved Today

Project: [https://github.com/chipsec/chipsec](https://github.com/chipsec/chipsec)
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