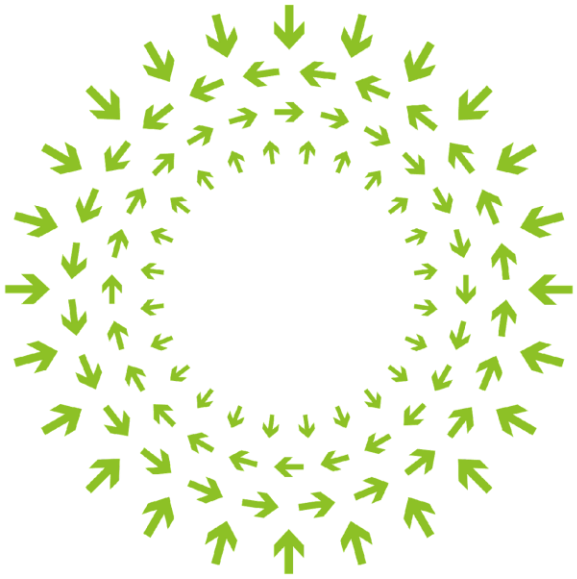

OPEN

Compute Project

Platform Infrastructure Connectivity (M-PIC) Base Specification

Part of the

Datacenter – Modular Hardware Systems (DC-MHS) Rev 1.0 Family

Version 0.70

April 22nd, 2022

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1.2. Acknowledgements

The Contributors of this Specification would like to acknowledge the following companies for their feedback:

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2. Version Table

Date	Version #	Description
April 22nd 2022	0.7	Initial public release.

3. Scope

This document defines technical specifications for the Platform Infrastructure Connectivity Specification used in Open Compute Project. This document shall comprise the hardware product types complete technical specification.

Any supplier seeking OCP recognition for a hardware product based on this spec must be 100% compliant with any and all features or requirements described in this specification.

3.1. Typical OCP Sections Not Applicable

This is a Base specification, requiring other MHS specifications to fully define a design. The following typical Sections of an OCP specification are not included because they are not applicable to this specification.

Rack Compatibility
Physical Spec
Rear Side Power, I/O, Expansion
Mechanical
Onboard Power System
Environmental Regulations/Requirements
Prescribed Materials
Software Support
System Firmware
Hardware Management
Security

4. Overview

This specification defines and standardizes common elements needed to interface a Host Processor Module (HPM) to the platform/chassis infrastructure elements/subsystems within the DC-MHS 10 family of OCP servers. Standardization of the common interfaces and connectors enables hardware compatibility between DC-MHS HPMs and various DC-MHS system components.

The standardized common elements defined in this specification can be utilized by DC-MHS form-factor specifications and/or DC-MHS peripherals. The elements defined within this specification are not inherently required with a DC-MHS form-factor. The form-factor specifications call out which of these elements are required or optional, the physical placement, and any additional details specific to that form-factor.

This specification defines connectors, signals, and electrical interface requirements to enable connectivity and hardware compatibility to the following types of platform/chassis infrastructure:

1. Cooling infrastructure including:

   a. **Cooling modules** with one or more intelligent fan controllers, interfaced to air-movers
   b. Monitoring and control of **liquid-cooling infrastructure**, handled as intelligent cooling modules
2. **Power distribution/management:** Connectors for input power from source or PDB (power distribution board) and connectors to output power to peripheral subsystems.
3. **Boot storage peripheral**: small modules that provide minimal storage for a hyper-visor or OS, typically using USB or 1 to 4 lanes of PCIe, typically a monolithic storage device or a controller with RAID1 using two media devices.
4. **Intrusion switch** to detect physical access to the internals of a platform.
5. **Internal Host USB** for Internal Key functions, debug, or as an additional source for control panel USB.
6. **Control panels** for human interaction beyond what is offered on DC-SCM. This includes options for indirect support for buttons, LEDs, more complex displays, and external peripheral ports like USB.
7. **Smart NIC Management Interface:** for Smart NICs that are connected to and managed by HPM via M-XIO.
8. **Coin Cell Battery** to supply for battery back-up power for features like RTC.
9. **DC-SCM** – Data Center Secure Control Module Revision 2.0 is used with DC-MHS.

4.1. Items Not Included

- Designs or specific implementation requirements on platform infrastructure including those referenced above.
- Elements specified by DC-SCM
- Elements specified by DC-MHS XIO Specifications
- Elements supporting rack-level infrastructure
- NVMe Hot plug: attention and LEDs
- Edge/Telco: time-sync requirements

5. Terminology

Table 1: Terminology

Standardized Term	Meaning	Alternative Terms
DC-SCM	Data Center Secure Control Module	
DC-MHS	Data center - Modular Hardware System	
M-FLW	Modular Hardware System Full Width HPM Form Factor	FLW
M-DNO	Modular Hardware System Partial Width Density Optimized HPM Form Factor	DNO
M-XIO	Modular Hardware System eXtensible I/O	XIO

M-CRPS	Modular Hardware System Common Redundant Power Supply	PSU, CRPS
HPM	Host Processor Module PCB or PCBA form factor defined in M-FLW or M-DNO	
Smart NIC	A programmable network device used to improve data center networking performance, security, features, and flexibility.	IPU or DPU
MCU	A microcontroller unit	uC
CEM	Card Electromechanical specification	
ACPI	Advanced Configuration and Power Interface	
PIB	Power Distribution Board	
PDB	Power Interface Board	
SMBus	Server Management Bus	SMB
PMBus	Power Management Bus	PMB
+12VStby	12V Standby from CRPS	
+12V	12V Main Power from CRPS	

6. Thermal Design

Systems have variable cooling requirements ranging from air movers to liquid cooling or hybrid solutions. This section describes the power and management interface for cooling systems which play an important role in the overall thermal solution. The HPM interface covered for cooling addresses only cooling subsystems connected to HPM via separate cooling subsystem boards because the HPM formfactors standardized on off-HPM cooling solutions. The adoption of DC-SCM caused the change in air mover cooling system architecture from discrete fan controls via BMC to cooling system being controlled over SMBus or I3C. That choice to use off HPM cooling solutions provides greater flexibility and applicability of an HPM to different platforms and cooling solutions. The method chosen for DC-MHS utilizes the managed power distribution connection (namely PICPWR) from the HPM or power distribution board for power and all remote cooling control management. The PICPWR connector includes a SMB/I3C interface and 4 additional sideband signals (per channel) that can be used to manage the cooling subsystem board. (See section **7.1** for the 12V PICPWR definition and/or section **7.2** for the 48V PICPWR definition.)

There is no intent to provide a dedicated remote cooling connector /interface definition.

In some cases, the cooling system may be managed and/or powered at a chassis or rack level so the HPM may play no role in the cooling system.

7. Power Delivery

7.1. 12V Power Distribution and Management

This section covers the minimum power distribution architecture requirements for a 12V HPM, and peripheral subsystems attached to the HPM. Example peripheral subsystems include, but not limited to, risers, backplanes, cooling, battery power, ingress from PSU or higher-level power source (e.g., multimodal). PICPWR stands for Platform Infrastructure Connectivity Power distribution connector. The goal is for HPM and Power Distribution boards to provide a homogeneous power + sideband interface for powering remote peripherals (like backplanes, risers, PCIe CEM AUX connections, etc.). Peripheral subsystems that do not require HPM to supply or manage their ingress power source are outside the scope of this specification. If an HPM contains PICPWR connectors, the use of those connectors is optional.

7.1.1. 12V PICPWR Power Connector Form Factor

Distribution of power within the HPM and to/from Peripheral Subsystems can be implemented in any connector form factor that meets minimum requirements:

- Connector has power pins with equal capability for power supply and return
- Connector has 6 sideband pins dedicated for power delivery management

Power connectors that meet the minimum requirements are referred to as PICPWR connectors

A PICPWR connector can include an implementation that has additional function/signals (for example, high-speed IO) shared in a common connector housing. Additionally, a PICPWR connector can support multiple channels of sideband signals, where each channel contains 6 sideband pins dedicated for power delivery management.

Figure 1 shows examples of a stand-alone PICPWR connector as well as a PICPWR implementation as part of a larger connector with additional functions/signals.

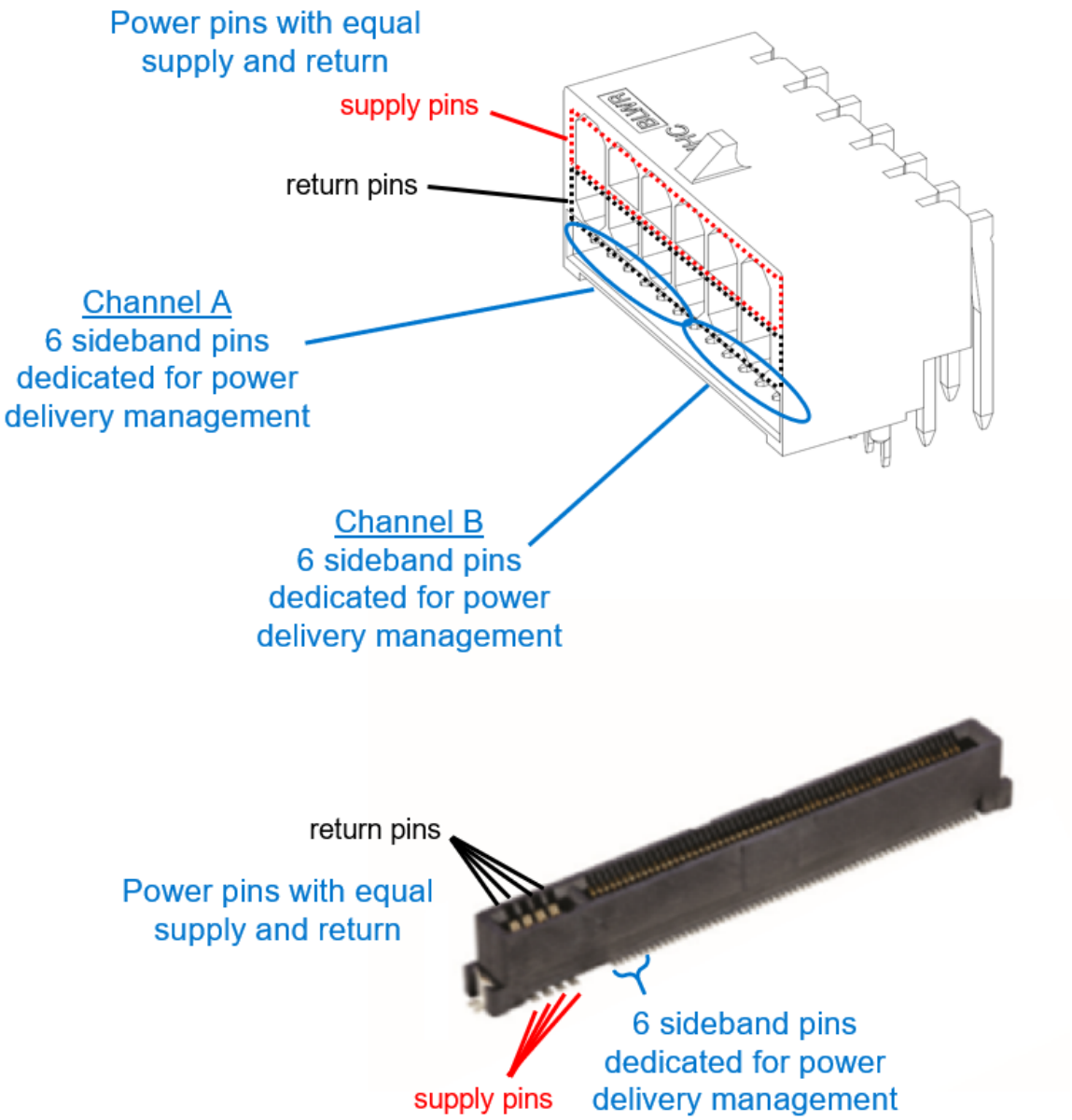

Figure 1: Examples of 12V PICPWR Connectors

7.1.2. 12V PICPWR Connector Power Labeling Requirements

Since each PICPWR connector power rating will depend on the ampacity and number of supply and return pins in the connector, as well as the size of copper planes attached to the connector, a visible silkscreen must be placed near the PICPWR connector to indicate the maximum TDP capability of the PICPWR implementation. Example “PWR*n*_12V_600W”, where *n* is a unique identifier/number for each PICPWR connector instantiation in the design.

7.1.3. 12V HPM Power Distribution Architecture

This section describes implementations of the HPM where the PSU or power subsystem is directly docking into the HPM.

Referring to *Figure 2*, the HPM power distribution architecture has the following attributes:

- PICPWR connectors are connected to the primary power output (i.e., “12V_PRIMARY”) of the power supply or power source subsystem.
- “12V_PRIMARY” is defined as the output of a power switching circuit where
  - 12V_PRIMARY is sourced by +12V in ACPI Power states from ACPI-S5 and higher (i.e., in ACPI-S5 to ACPI-S0)
  - 12V_PRIMARY is sourced by +12VStby in ACPI Power states less than ACPI-S5
  - If a platform has an S5 configuration whose 12V_Primary load is within the CRPS +12VStby limit, they may choose to be in ACPI-S5 with 12V_Primary sourced by +12VStby.
- 12V PICPWR connectors can only connect to 12V_PRIMARY
- PICPWR connectors are bi-directional: can be either power source (power egress) or power sink (power ingress). Refer to the HPM form factor specifications for current flow direction.
- Other than the power capability of the power connector, each PICPWR connector on the HPM is logically equivalent.
- It is strongly recommended that HPM designs balance current flow through adjacent PICPWR connectors to enable source or load sharing and without overloading one of the two current paths.
- There is **no power gating to PICPWR connectors on 12V_PRIMARY**.
- In implementations where the PSU is directly docking into the HPM, it is the responsibility of the HPM and/or the PSU implementation to gate the voltage output of the PSU to prevent the wrong voltage to be distributed through the 12V_PRIMARY rail (e.g., 48V instead of 12V).

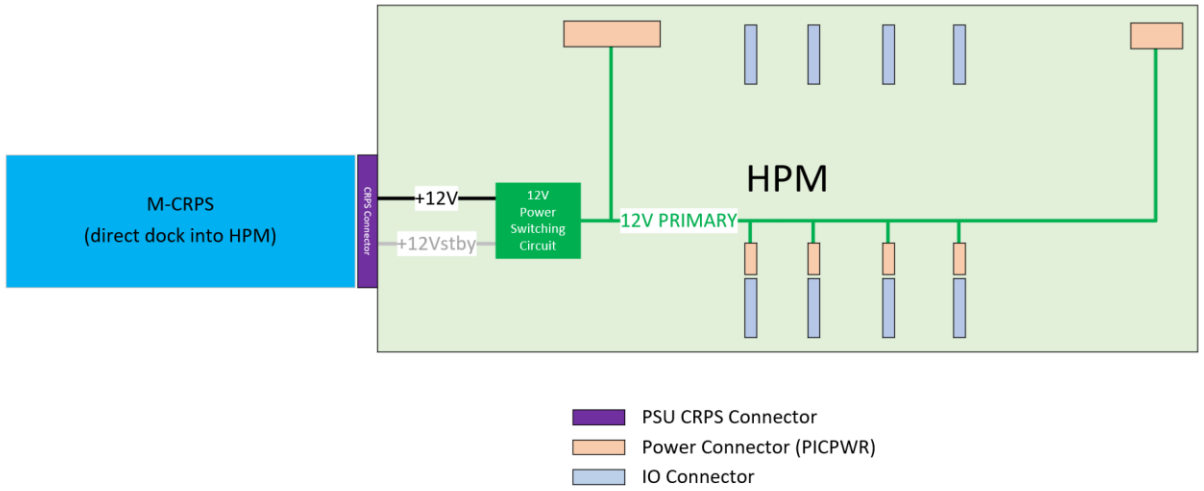

Figure 2: HPM 12V Power Distribution Architecture (PSU Direct mate to HPM variant)

7.1.4. 12V Remote Power Distribution Architecture

This section describes requirements of a Remote Power Distribution implementation where the PSU or power subsystem is docking into the Remote Power Distribution or PDB/PIB (Power Distribution Board / Power Interface Board) and powering the HPM via a PICPWR connector on the HPM.

Referring to *Figure 3*, the Remote Power Distribution architecture has the following attributes:

- 12V power switching implemented on the Remote Power Distribution and connects the switching output "12V_PRIMARY" to a PICPWR connector on the HPM
- "12V_PRIMARY" is defined as the output of a power switching circuit where:
  - 12V_PRIMARY is sourced by +12V in ACPI Power states from ACPI-S5 and higher (i.e. in ACPI-S5 to ACPI-S0)
  - 12V_PRIMARY is sourced by +12VStby in ACPI Power states less than ACPI-S5
  - If a platform has an S5 configuration whose 12V_Primary load is within the CRPS +12VStby limit, they may choose to be in ACPI-S5 with 12V_Primary sourced by +12VStby.
- In implementations where the PSU is directly docking into a PDB, it is the responsibility of the PDB and/or the PSU implementation to gate the voltage output of the PSU to prevent the wrong voltage to be distributed through the 12V_PRIMARY rail (e.g., 48V instead of 12V).
- If configurations with power subsystems directly docking into the HPM and connected to the HPM through a PDB exist, requirements for each attachment method must be met, even though they may share power.

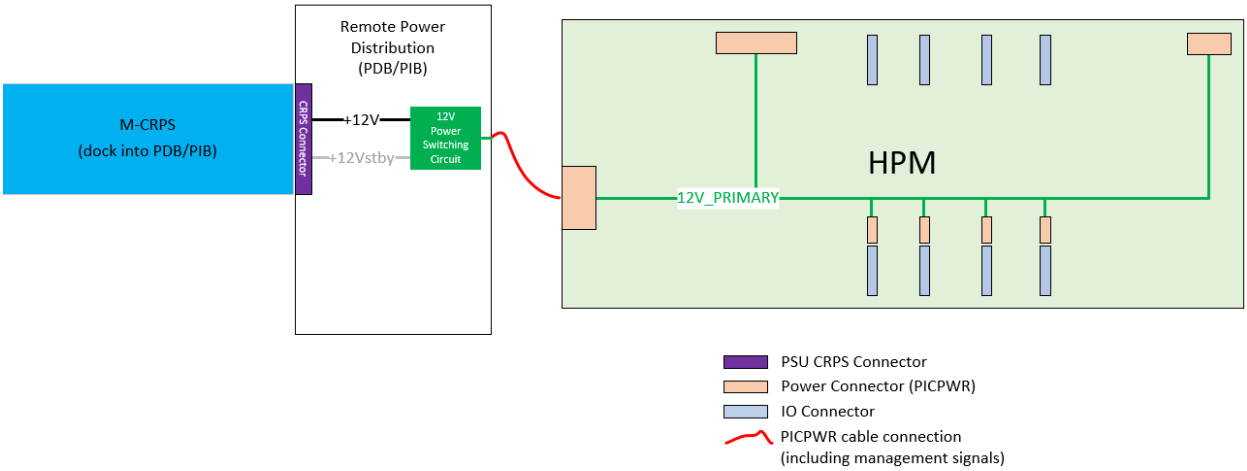

Figure 3: Remote 12V Power Distribution Architecture (PSUs mate to PDB/PIB variant)

7.1.5. 12V Peripheral Subsystem Power Distribution Architecture

Referring to *Figure 4*, the Peripheral Subsystem power architecture has the following attributes:

- Peripheral subsystems can attach to any PICPWR connector on the HPM that has the power capability to support loads of the peripheral subsystem.
- PICPWR connectivity methods are dependent on system needs and connection type(s) supported at each PICPWR location (e.g., card edge or a compatible cable).
- For cable applications with PICPWR connectors, the pinouts must both meet M-PIC pinout requirements.
- A peripheral subsystem consists of a management subsystem, a power gating subsystem, and a power load.
- The peripheral subsystem must assume that the power rail supplied from the HPM will be operational in the ACPI-S5 power state. If the load on the peripheral subsystem is not intended to operate in the S5 domain, then the peripheral subsystem must implement appropriate power gating for the load.
- Loads directly attached to PICPWR connectors are not supported (e.g., PCIe AUX power cable attaching from PICPWR to PCIe AIC is NOT supported). Since there is no gating on the HPM, all loads must be powered via a peripheral subsystem (with gating) to prevent 12V_PRIMARY from being overloaded while it's sourced by +12VStby. Gating is controlled by the HPM using PICPWR_SB[4:1] and/or SMBus.

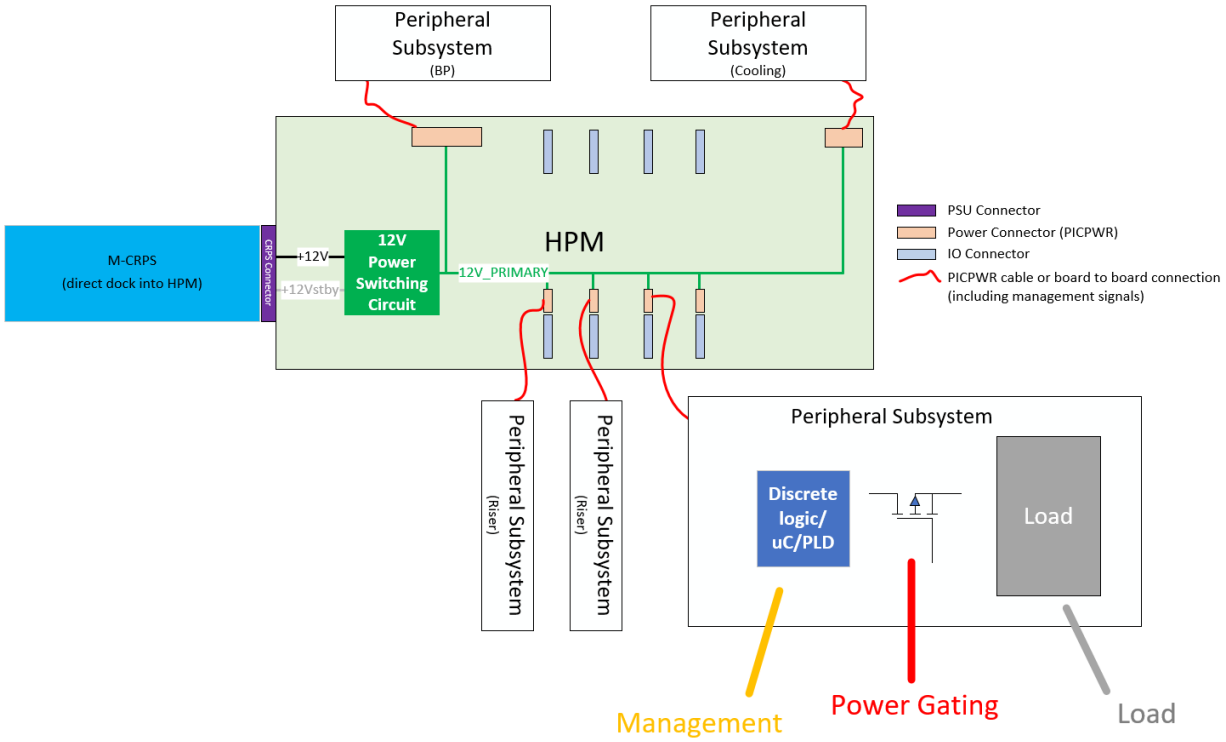

Figure 4: Peripheral Subsystem 12V Power Distribution Architecture

Figure 5 shows additional details of the power architecture of a Peripheral Subsystem.

- The power gating in the Peripheral Subsystem is needed if loads are not intended to operate in ACPI-S5 state. Power gating can be implemented in a variety of forms including, but not limited to, load switches, hot-swap controller, voltage regulators. It is the responsibility of system implementors to design a Peripheral Subsystem that does not cause back-feeding, over current or over voltage events to propagate back into the HPM and Power Supply subsystem.
- 4 Sideband GPIOs and an SMBus interface is provided to the peripheral subsystem to enable the HPM to perform status, control, and inventory.
- It is strongly recommended that Peripheral designs balance current flow through PICPWR connectors in applications that source power through more than one PICPWR connector (on HPM or on the peripheral) to prevent overloading one of the two current paths.

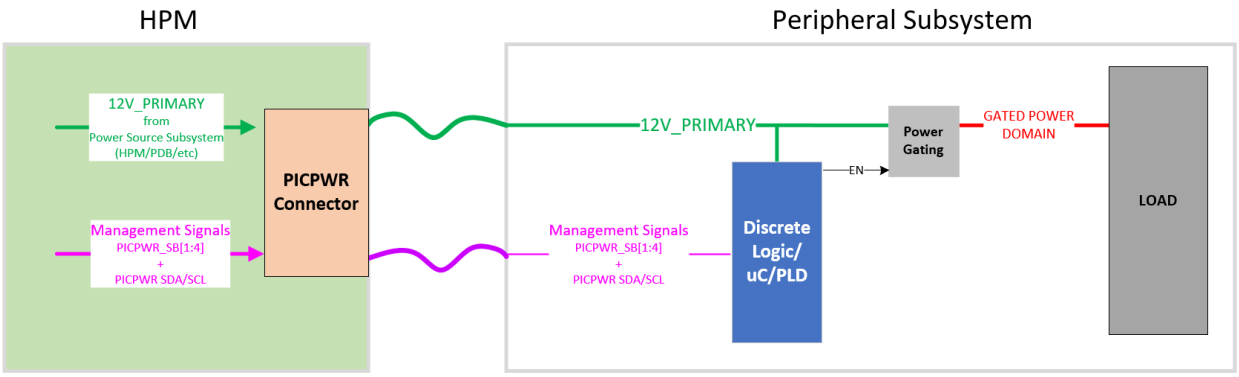

Figure 5: Peripheral Subsystem 12V Power Distribution Architecture Details

7.1.6. 12V PICPWR Connector Pin Definition

Table 2: 12V PICPWR Pin Definition

Pin(s)	Signal Name	Signal Requirements
PWR	12V_PRIMARY	Primary power rail from the power source subsystem used to power downstream loads & logic on peripheral subsystem 12V_PRIMARY is defined as the output of a power switching circuit where: ● 12V_PRIMARY is sourced by +12V in ACPI Power states from ACPI-S5 and higher (i.e., in ACPI-S5 to ACPI-S0) ● 12V_PRIMARY is sourced by +12VStby in ACPI Power states below ACPI-S5 ● If a platform has an S5 configuration whose 12V_Primary load is within the CRPS +12VStby limit, they may choose to be in ACPI-S5 with 12V_Primary sourced by +12VStby.
PWR	GND	Ground return for 12V_PRIMARY and side-band signals
SB1: 4	PICPWR_SB[1: 4]	Sideband GPIOs for status, control, and inventory of peripheral subsystem; Must be connected to HPM FPGA with prescribed terminations for “Plug-N-Code” specific usages. For Electrical Requirements see section **8.10**, *Table 3*, and *Figure 6*.
SB5	PICPWR_SCL	SMBus, 3.3V, up to 400KHz or I3C Basic 1.1.1 mode, 1.8V, at higher speeds (I3C speeds vary based on overall topology and loading).
SB6	PICPWR_SDA	

		For SMBus operation, a pullup to 3.3V is enabled. For I3C mode, the pullup would be integrated in the I3C device upstream of the PICPWR connector, would be configurable (start at 3.3V then go to 1.8v), and transaction based. See section **8.10**. Electrical Requirements.

Each instantiation of a PICPWR connector must implement a unique set of 6 sidebands. Additionally, *Table 3* describes how the sideband signals on the HPM must be implemented.

Table 3: Required HPM implementation for each 12V PICPWR connector

Pin	**Signal Name**	**HPM Implementation Requirements**		
		HPM Connections	**Termination**	**HPM GPIO Buffer Type**
SB1	PICPWR_SB1	connect to HPM FPGA GPIO	22Ω Series + 127kΩ pullup to +3.3Vaux	Configurable as both open-drain AND push-pull
SB2	PICPWR_SB2	connect to HPM FPGA GPIO	22Ω Series + 127kΩ pullup to +3.3Vaux	Configurable as both open-drain AND push-pull
SB3	PICPWR_SB3	connect to HPM FPGA GPIO	22Ω Series + 127kΩ pullup to +3.3Vaux	Configurable as both open-drain AND push-pull
SB4	PICPWR_SB4	connect to HPM FPGA GPIO	22Ω Series + 127kΩ pulldown to GND	Configurable as both open-drain AND push-pull
SB5	PICPWR_SCL	connect to DC-SCM SMBus subsystem	For SMBus operation, a 2.21kΩ pullup to 3.3V is enabled. For I3C mode, the pullup would be integrated in the I3C device upstream of the PICPWR connector, would be configurable (start at 3.3V then go to 1.8v), and transaction based.	SMBus or I3C Basic compliant
SB6	PICPWR_SDA	connect to DC-SCM SMBus subsystem		SMBus or I3C Basic compliant

Figure 6 shows the required HPM implementation with the example of two 12V PICPWR connector instantiations. Pullups on SCL and SDA are shown for reference, see *Table 3* for details.

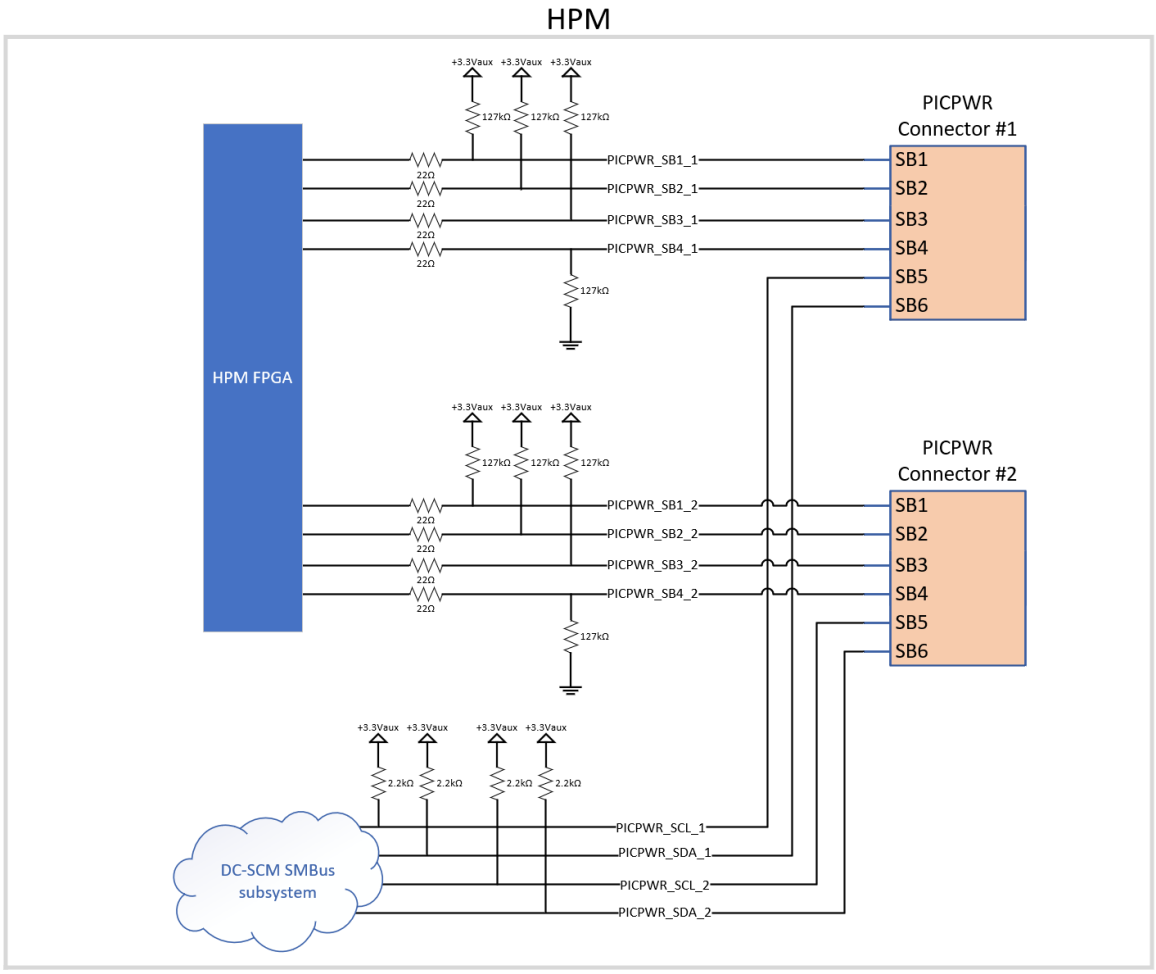

Figure 6: HPM implementation with two 12V PICPWR connectors

7.1.6.1. 12V 2x6+12SB PICPWR Right Angle Header Pinout

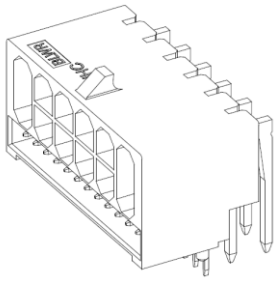

Figure 7: 12V 2x6+12SB PICPWR Right Angle Header

Manufacturer: Bellwether
Part Number: 70367-122*

(for reference only, part number for example cable plug: Bellwether 70369-1260)

Notes:
This connector has two independent channels (A & B) of PICPWR sideband management signals. These connector part numbers are current as of publication. Please refer to connector vendors or [document TBD] for part numbers that best meet the application.

Table 4: 12V 2x6+12SB PICPWR Right Angle Header Pinout

Circuits [1:6]	GND
Circuits [7:12]	12V_PRIMARY
SB1	PICPWR_SB1_A
SB2	PICPWR_SB2_A
SB3	PICPWR_SB3_A
SB4	PICPWR_SB4_A
SB5	PICPWR_SCL_A
SB6	PICPWR_SDA_A
SB7	PICPWR_SB1_B
SB8	PICPWR_SB2_B
SB9	PICPWR_SB3_B
SB10	PICPWR_SB4_B
SB11	PICPWR_SCL_B
SB12	PICPWR_SDA_B

7.1.6.2. 12V 2x6+12SB PICPWR Vertical Header Pinout

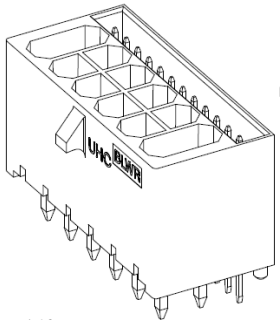

Figure 8: 12V 2x6+12SB PICPWR Vertical Header

Manufacturer: Bellwether
Part Number: 70368-122*

(for reference only, part number for example cable plug: Bellwether 70369-1260)

Notes:
This connector has two independent channels (A & B) of PICPWR sideband management signals. These connector part numbers are current as of publication. Please refer to connector vendors or [document TBD] for part numbers that best meet the application.

Table 5: 12V 2x6+12SB PICPWR Vertical Header Pinout

Circuits [1:6]	GND
Circuits [7:12]	12V_PRIMARY
SB1	PICPWR_SB1_A
SB2	PICPWR_SB2_A
SB3	PICPWR_SB3_A
SB4	PICPWR_SB4_A
SB5	PICPWR_SCL_A
SB6	PICPWR_SDA_A
SB7	PICPWR_SB1_B
SB8	PICPWR_SB2_B
SB9	PICPWR_SB3_B
SB10	PICPWR_SB4_B
SB11	PICPWR_SCL_B
SB12	PICPWR_SDA_B

7.1.6.3. 12V Near Side Riser PICPWR Egress Pinout

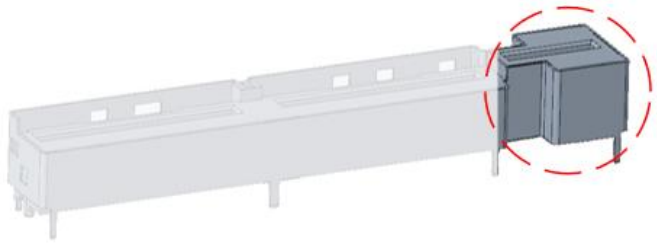

Figure 9: 12V Near Side Riser PICPWR Egress

Manufacturer: Amphenol
Part Number: G03V213X2HR

Notes: This connector has XIO and PICPWR pins all within the same housing. *Table 6* only covers the pinout of the power section of this connector (circled in *Figure 6*). Refer to M-XIO specification for additional pinout details. This connector has two independent channels (A & B) of 12V PICPWR sideband management signals. This connector part number is current as of publication. Please refer to connector vendors or [document TBD] for part numbers that best meet the application.

Table 6: 12V Near Side Riser PICPWR Egress Pinout

PA[1:4]	12V_PRIMARY
PB[1:4]	GND
SA1	PICPWR_SB1_A
SA2	PICPWR_SB2_A
SA3	PICPWR_SB3_A
SA4	PICPWR_SB4_A
SA5	PICPWR_SCL_A
SA6	PICPWR_SDA_A
SB1	PICPWR_SB1_B
SB2	PICPWR_SB2_B
SB3	PICPWR_SB3_B
SB4	PICPWR_SB4_B

SB5	PICPWR_SCL_B
SB6	PICPWR_SDA_B

7.1.6.4. 12V 3+12SB+3 PICPWR Blind-mate Right Angle Connector Pinout

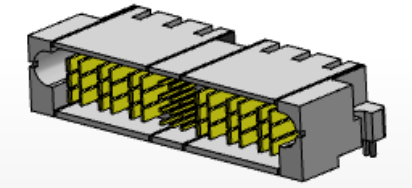

Figure 10: 12V 3+12SB+3 PICPWR Blind-mate connector

Manufacturer: Amphenol

Part Number: 10106263-6003003LF or Equivalent

Notes: Connector power pin current rated at 30A per contact. This connector part number is current as of publication. Please refer to connector vendors or [document TBD] for part numbers that best meet the application.

Table 7: 12V 3+12SB+3 PICPWR Blind-mate Right Angle Connector Pinout

P[1:3]_ [1:8]	GND
A1	PICPWR_SCL_A
A2	PICPWR_SDA_A
A3	PICPWR_SB1_A
B1	PICPWR_SB2_A
B2	PICPWR_SB3_A
B3	PICPWR_SB4_A
C1	PICPWR_SCL_B
C2	PICPWR_SDA_B
C3	PICPWR_SB1_B
D1	PICPWR_SB2_B
D2	PICPWR_SB3_B
D3	PICPWR_SB4_B
P[4:6]_ [1:8]	12V_PRIMARY

7.1.7. Example 12V Topologies

7.1.7.1. Powering a 12V PCIe Device with AUX Power Cable

Figure 11 shows a couple of example implementations of how to use PICPWR to power a PCIe device with an AUX cable. Note that the PCIe AUX power cable is not directly attached to the HPM's PICPWR connector. Instead, the AUX power cable comes from a PDB or a Peripheral subsystem with management and power gating capability.

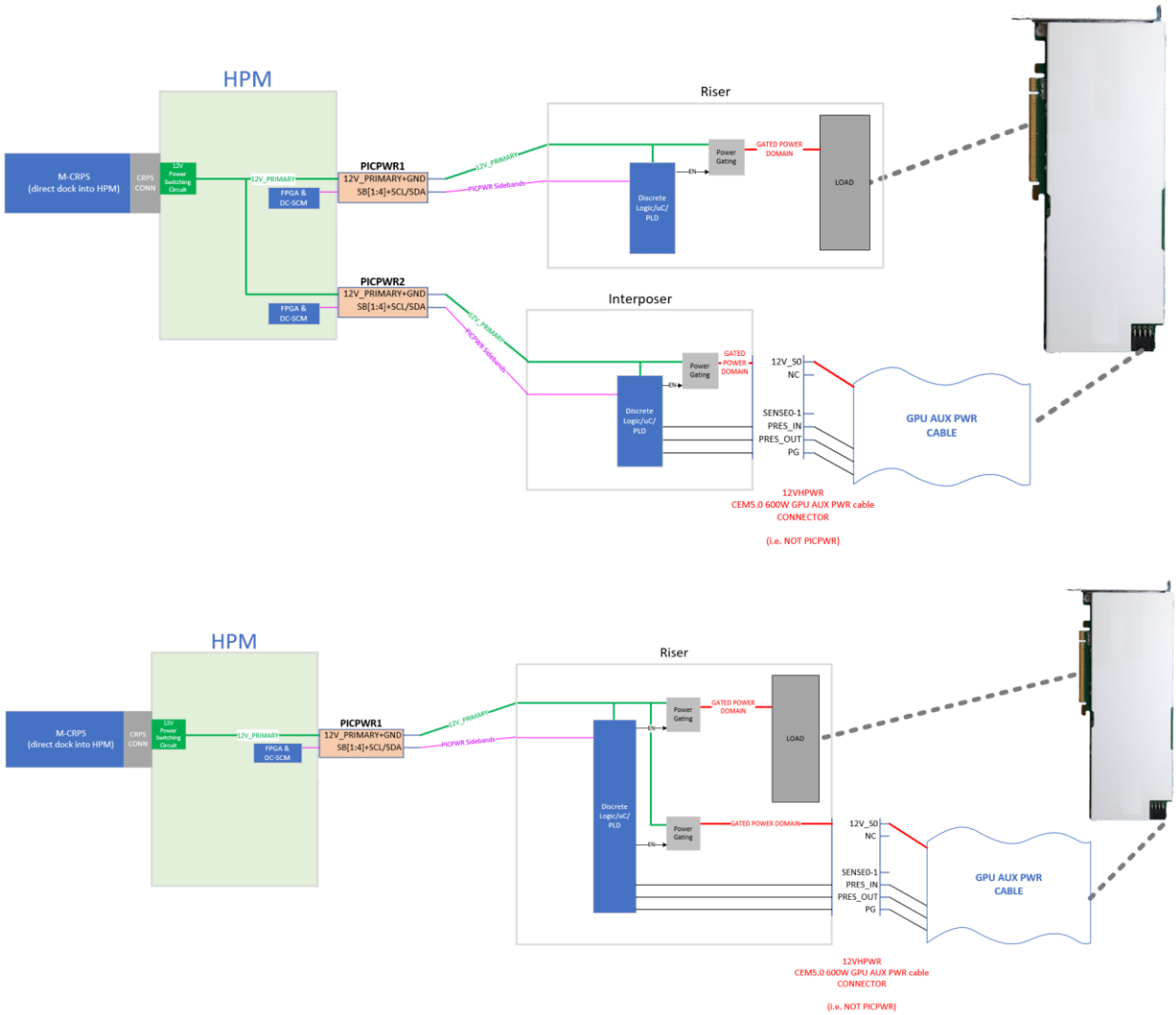

Figure 11: Powering a 12V CEM Riser & 12V PCIe Device 's AUX Power Cable

7.1.7.2. Multiple 12V PICPWR Connectors Powering a Peripheral Subsystem

Figure 12 shows two PICPWR connectors on the HPM powering a single peripheral subsystem to support the large power requirements of a single peripheral subsystem. It is strongly recommended that HPM, cable, and Peripheral designs balance current flow through both PICPWR connectors in applications with shared sources or loads to prevent overloading one of the two current paths.

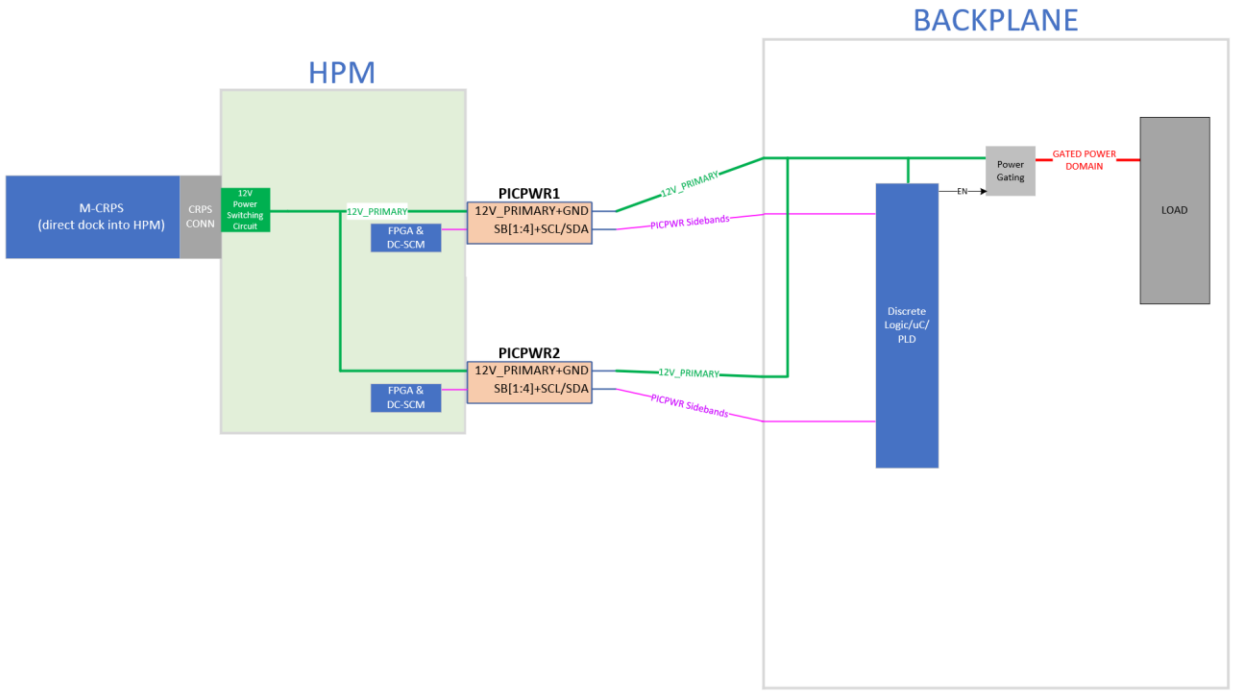

Figure 12: Multiple 12V PICPWR Connectors Powering a Single Peripheral Subsystem

7.1.7.3. 12V PICPWR Implementation in a PSU PDB Topology

In *Figure 13*, PSUs on a PDB provide power to the HPM through PICPWR connectors. The HPM and the PSUs communicate all real-time control and status through the PICPWR sideband pins. PICPWR SMBus and sideband pins provide a mechanism for PMBus messages between the HPM and PSUs. Note that analog signals, including a cable presence detection signal, are cabled from the PDB to the HPM through the analog signal connector as described in section **7.1.8.**

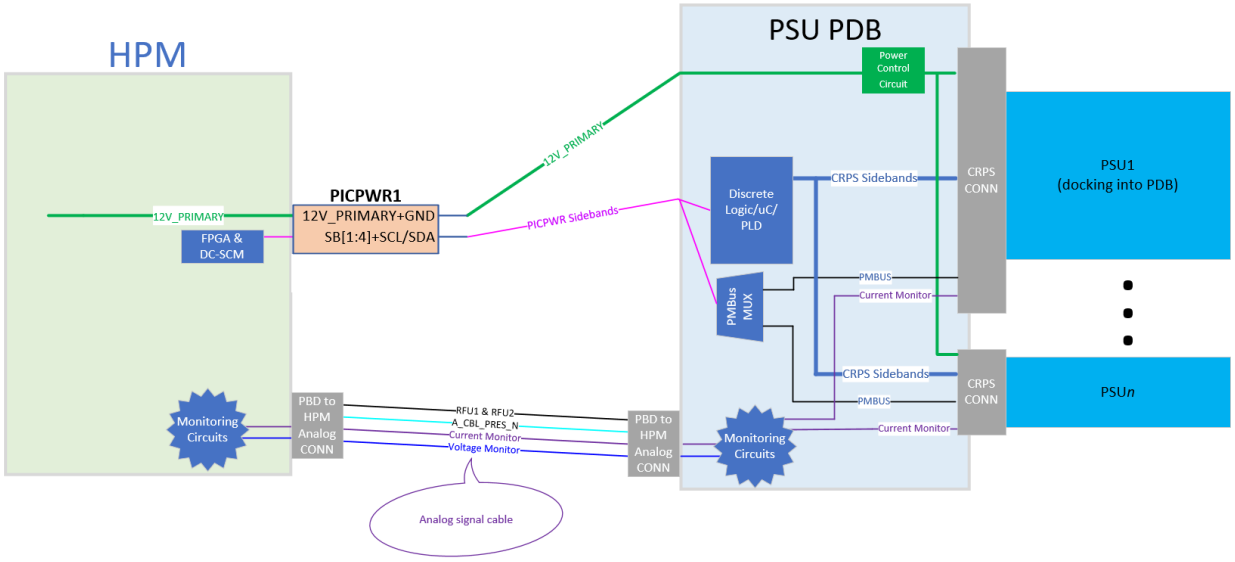

Figure 13: Power Supplies through PDB

7.1.8. 12V 1x6 Vertical PDB to HPM Analog Header

This section defines an optional connection for HPMs used with a PDB. This connector provides analog connections used to monitor current and voltage from the M-CRPS modules on the PDB.

Table 8: PDB to HPM Analog Connector Pinout

Pin	Name	Usage
1	Current Monitor	Shared current monitor signal that represents the total output current for all shared power supplies.
2	Voltage Monitor	Output signal from PDB circuit.
3	GND	GND Return for signal referencing.
4	A_CBL_PRES_N	HPM to PDB cable detection. Use the same topology as PICPWR_SB3.
5	RFU1	Reserved for future use – No connect on both sides
6	RFU2	Reserved for future use – No connect on both sides

1x6 Vertical Header Manufacturer: Molex Part Number: 2083810603

Notes: This connector part number is current as of publication. Please refer to connector vendors or [document TBD] for part numbers that best meet the application.

7.2. 48V Power Distribution and Management

This section covers the minimum power distribution architecture requirements for a 48V HPM, and peripheral subsystems attached to the HPM. Example peripheral subsystems include, but not limited to, risers, backplanes, cooling, battery power, ingress from PSU or higher-level power source (e.g., multimodal). PICPWR stands for Platform Infrastructure Connectivity Power distribution connector. The goal is for HPM and Power Distribution boards to provide a homogeneous power + sideband interface for powering remote peripherals (like backplanes, risers, PCIe CEM AUX connections, etc.). Peripheral subsystems that do not require HPM to

supply or manage their ingress power source are outside the scope of this specification. If an HPM contains PICPWR connectors, the use of those connectors is optional.

7.2.1. 48V PICPWR Power Connector Form Factor

<TBD>

Add a keying table for 12V vs 48?

7.2.2. 48V PICPWR Connector Power Labeling Requirements

Since each PICPWR connector power rating will depend on the ampacity and number of supply and return pins in the connector, as well as the size of copper planes attached to the connector, a visible silkscreen must be placed near the PICPWR connector to indicate the maximum TDP capability of the PICPWR implementation. Example “PWR*n*_48V_600W”, where *n* is a unique identifier/number for each PICPWR connector instantiation in the design.

7.2.3. 48V HPM Power Distribution Architecture

<TBD/UI>

Other 48V/12V variants may be added in a future version of this specification.

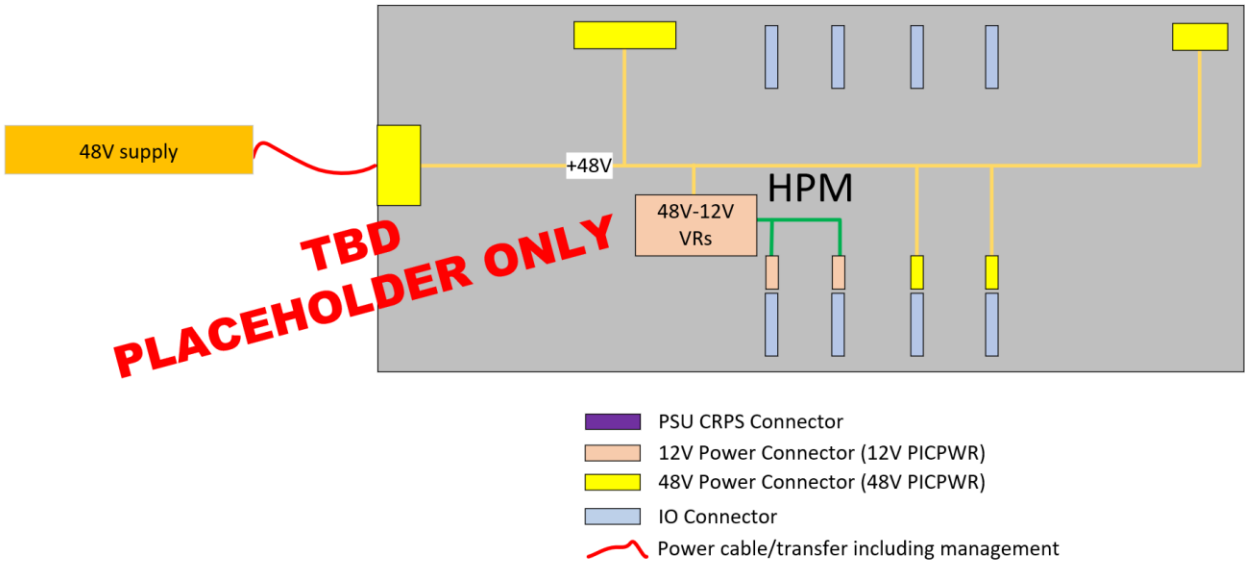

Figure 14: HPM 48V Power Distribution Architecture (48V to HPM variant)

7.2.4. 48V PICPWR Connector Pin Definition

<TBD>

8. IO System

8.1. Boot Storage Peripheral

This section defines an optional cable optimized interface for a boot/storage peripheral. If present, the peripheral interface is comprised of one M-XIO x4 (defined in the M-XIO specification) connector and one PICPWR connection. Because this interface is using standard DC-MHS building blocks, it could also be used for other peripherals that don't required the extended sideband signals. HPMs could also be implemented with an integrated boot storage subsystem or without a boot storage subsystem. This subsystem is typically implemented as 1 or 2 M.2 media devices or similar, and often with a RAID 1 controller. PCIe generational/speed requirements are not provided. Multiple HPMs sharing a single boot storage peripheral is outside the scope of this specification.

8.2. Intrusion Switch

HPM form-factors supporting an intrusion switch shall implement as follows:

1. 1x3 Vertical header Manufacturer: FIT (Foxconn) Part Number: HSM1033-K1100-9H Notes: This connector part number is current as of publication. Please refer to connector vendors or [document TBD] for part numbers that best meet the application.
2. The signal HPM_SCM_INTRUSION_N is routed directly between header and DC-SCM without other circuit connectivity. Polarity of the HPM_SCM_INTRUSION_N has an active low indicating intrusion.
3. Presence-detect signal routed to HPM's FPGA
4. Electrical details of the signal are defined in the DC-SCM 2.0 specification.

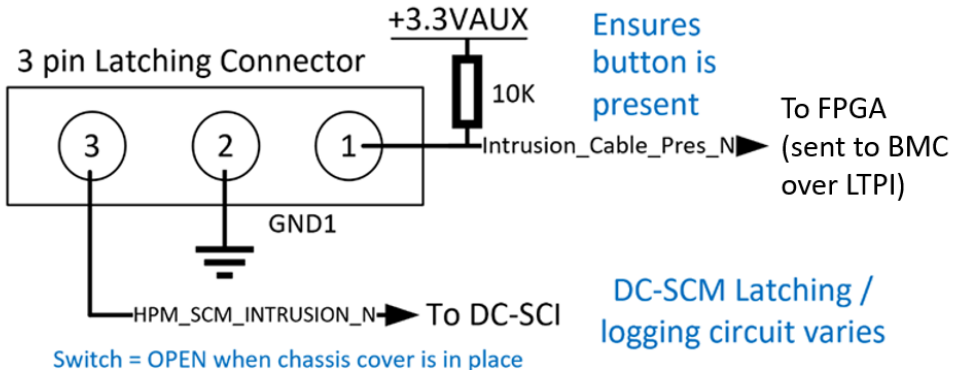

Figure 15: Intrusion Switch Pinout and Connectivity

8.3. Internal Host USB3 Connector

If the HPM includes only one internal host USB3.1 connector (Internal port), it shall be a vertical type C connector. Refer to *Figure 16* for an example of Host and BMC managed USB connectivity.

Usage examples include Control Panel expansion, debug, or an Internal key. Physical presence, location, and envelope / keep out of the attached device or cable exit are to be defined by individual HPM form factor specifications. Additional USB connectors located on the HPM are outside the scope of this specification.

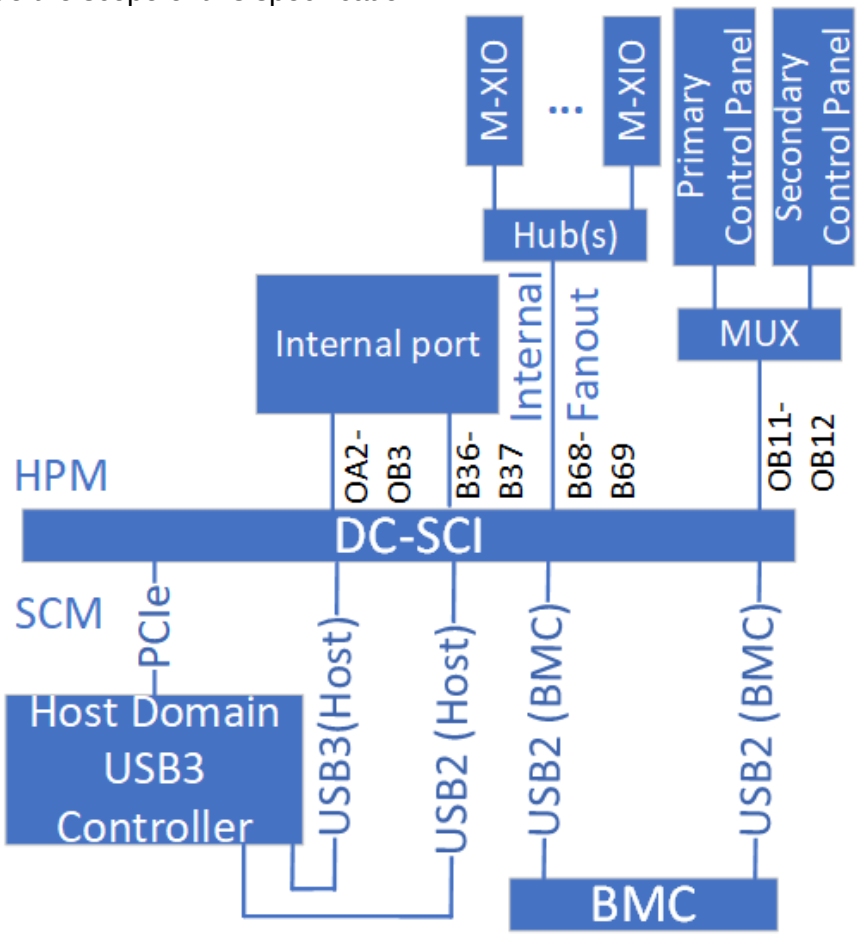

Figure 16: Example High Level USB Diagram

8.4. Control Panel Interfacing

If the HPM form-factor includes a single control, then it will be the primary control panel (PCP) connector. If an HPM form-factor includes two control panels, the additional control panel will be the secondary control panel (SCP) connector. Connecting multiple HPMs to a single control panel is outside the of scope of this specification.

Additional buses or signals may be sourced from DC-SCM hosted connectors. For example, if front VGA or display port feature is added to the system, it could be sourced from the DC-SCM.

If USB3 is required in one or more control panels, it may be cabled from the Internal USB3 connector on the HPM described in section **8.3**.

Table 9: Primary HPM Control Panel Pin Definition

Signal	Description	Spec	Notes
12V_CP GND	Control Panel Power S5 available power distribution	12V +/-8%, Up to 200mA before 12V_PRIMARY is sourced by +12V. Up to 1.4A after 12V_PRIMARY is sourced by +12V.	12V_CP is derived from raw CRPS +12VStby but switched to +12V when it's available. It could also be shared with other subsystems.
[SMB/I3C]_BMC_SDA /SCL	From DC-SCM BMC	3.3V Aux powered. Available from S5, up to 400KHz or I3C basic mode, 1.8V, at higher speeds (I3C speeds vary based on overall topology). For SMBus operation, a pullup to 3.3V is enabled. For I3C mode, the pullup would be integrated in the I3C device upstream of the PICPWR connector, would be configurable (start at 3.3V then go to 1.8v), and transaction based. See section **8.10**. Electrical Requirements.	Used for Temp sensor, and/or other SMBus devices
PCP_SB[4:1]	From HPM FPGA for GPIO expansion on Control Panel	Use the same HPM topology, termination values as PICPWR_SB[4:1] See section **8.10**. Electrical Requirements See *Figure 6* for topology	Sideband GPIOs for status, control, inventory, and/or other control panel functions; Must be connected to HPM FPGA with prescribed terminations for "Plug-N-Code" specific usages.
USB_PCP_DP/DN	One USB 2.0 combo (SCMOTG/ HPMHOST) connection from DC-	See section **8.10**. Electrical Requirements	Potential use cases: boot key, service port, keyboard, or mouse. Expect a USB Hub on control panel for richer features. Video or

	SCM (pins OB11, OB12). When the secondary control panel connector exists, a MUX on this bus between control panel connectors is advised for maximum platform flexibility.	Refer to *Figure 16* for Host USB high level DC-SCM to HPM USB connectivity.	USB3.0 would be fly over from enabled HPM
SPI	SPI bus from DS-SCM	>=33 MHz See section **8.10**. Electrical Requirements 3.3V_VAUX signaling (in S5)	Higher speed bus for devices such as SPI flash HPM is the SPI controller source where: MOSI is an output from HPM. MISO is an input to HPM.

Primary HPM to Control Panel connector

2x10 Vertical Header Manufacturer: Molex Part number: 2083912003

Notes: This connector part number is current as of publication. Please refer to connector vendors or [document TBD] for part numbers that best meet the application.

Table 10: Primary HPM Control Panel Pinout

Pin	Signal
A1	12V_CP
A2	12V_CP
A3	NC

Signal	PIN
GND	B1
[SMB/I3C]_BMC_SDA	B2
[SMB/I3C]_BMC_SCL	B3

A4	GND
A5	USB2_PCP_DP
A6	USB2_PCP_DN
A7	GND
A8	MISO
A9	CS
A10	MOSI

GND	B4
PCP_SB4	B5
PCP_SB3	B6
PCP_SB2	B7
PCP_SB1	B8
GND	B9
CK	B10

Table 11: Secondary HPM Control Panel Pin Definition

Signal	description	spec	Notes
P12V_CP GND	Control Panel Power S5 available power distribution	12V +/-8%, Up to 200mA before 12V_PRIMARY is sourced by +12V. Up to 1.4A after 12V_PRIMARY is sourced by +12V.	12V_CP is derived from raw CRPS +12VStby but switched to +12V when it's available. It could also be shared with other subsystems.
[SMB/I3C]_BMC_SCP_SDA/SCL	From DC-SCM BMC	3.3V powered. Available from S5, up to 400KHz or I3C basic mode, 1.8V, at higher speeds (I3C speeds vary based on overall topology). For SMBus operation, a pullup to 3.3V is enabled. For I3C mode, the pullup would be integrated in the I3C device upstream of the PICPWR connector, would be configurable (start at 3.3V then go to 1.8v), and transaction based. See section **8.10**. Electrical Requirements.	Used for Temp sensor, and/or other SMBus devices
SCP_SB[4:1]	From HPM FPGA for GPIO expansion on Control Panel	Use the same HPM topology, termination values as PICPWR_SB[4:1]	Sideband GPIOs for status, control, inventory, and/or other control panel

		See section **8.10**. Electrical Requirements See *Figure 6* for topology	functions; Must be connected to HPM FPGA with prescribed terminations for “Plug-N-Code” specific usages.
USB_SCP_DP/DN	One USB 2.0 combo (SCMOTG/HPMHOST) connection from DC-SCM (pins OB11, OB12). A MUX between control panel connectors is advised for maximum platform flexibility.	See section **8.10**. Electrical Requirements Refer to *Figure 16* for Host USB high level DC-SCM to HPM USB connectivity.	Potential use cases: boot key, service port, keyboard, or mouse. Expect a USB Hub on control panel for richer features. Video or USB3.0 would be fly over from enabled HPM
RFU_[1:4]	RFU pins	Must not be Connected	Reserved for Future Use

Secondary HPM to Control Panel Connector

2x10 Vertical Header Manufacturer: Molex Part number: 2083912003

Notes: This connector part number is current as of publication. Please refer to connector vendors or [document TBD] for part numbers that best meet the application.

Table 12: Secondary HPM Control Panel Pinout

Pin	Signal
A1	12V_CP
A2	12V_CP
A3	NC
A4	GND
A5	USB2_SCP_DP
A6	USB2_SCP_DN
A7	GND
A8	RFU_1
A9	RFU_2
A10	RFU_3

Signal	Pin
GND	B1
[SMB/I3C]_BMC_SDA	B2
[SMB/I3C]_BMC_SCL	B3
GND	B4
SCP_SB4	B5
SCP_SB3	B6
SCP_SB2	B7
SCP_SB1	B8
GND	B9
RFU_4	B10

Vendor rated at 1A per contact

8.5. TPM

If using a single node configuration with a single DC-SCM, then then the TPM used is located on the DC-SCM. Other configurations are outside the scope of this specification because the DC-SCI lacks the interface for more than one TPM. Placement or mechanical aspects are outside the scope of this specification.

8.6. OCP NIC 3.0

See HPM form factor specifications for guidance on explicit OCP NIC supported variations (SFF, LFF, hot plug supported, etc.).

8.7. Smart NIC Management Interface

DC-MHS supports the option to manage DPU/Smart NIC/IPU devices using BMC USB2.0 host controller signals through the M-XIO connectivity from HPM to peripherals (x8 cable or wider). Therefore, no additional interface needs to be defined in this specification. Management of DPU/Smart NIC/IPU devices shared with multiple HPMs is outside the scope of this specification. Refer to *Figure 16* for Host USB high level DC-SCM to HPM USB connectivity.

8.8. Coin Cell Battery

A CR2032 system coin cell battery shall reside on the HPM. The coin cell battery holder shall be compatible with a CR2032 battery. Orientation of the connector coin cell battery holder is outside the scope of this specification.

8.9. DC-SCM Revision

DC-MHS is defined using the features and the form factor of DC-SCM revision 2.0. Use of DC-SCM revision 1.0 is outside the scope of this specification.

Note: Even though DC-SCM doesn’t require a new interface for HPM discovery, it is important for HPM designers to consult the DC-SCM revision 2.0 specification for HPM discovery logic requirements.

8.10. Electrical Requirements

The PICPWR and Control Panel logic levels for single-ended digital signals (PICPWR_SB[4:1]_[B:A], [P/S]CP_SB[4:1] , INTRUSION_CABLE_PRES_N, HPM_SCM_INTRUSION_N, and SPI) are defined in *Table 13*.

For SMBus signals (named with SCL or SDA) logic levels, refer to the System Management Bus (SMBus) Specification, Version 3.1.

For I3C signals (named with SCL or SDA) logic levels, refer to the I3C Basic 1.1.1 Specification.

For USB, reference Universal Serial Bus Specification. Inputs and outputs are referenced from the signal destination's standpoint.

The destination subsystem is responsible for 1) electrical protection of local circuitry if the peripheral/subsystem is unpowered, 2) any cross-power domain isolation (such as when connecting MAIN powered only targets to the upstream AUX powered bus) and 3) any necessary voltage level translation in SMBus mode.

Table 13: 3.3V Logic Signal Requirements

Symbol	Parameter	Min	Max	Unit	Notes
Vih	Input High Voltage	2.0	3.465	V	
Vil	Input Low Voltage	-0.3	0.8	V	
Voh	Output High Voltage	2.3	3.465	V	
Vol	Output Low Voltage		0.2	V	
SPI Vih	Input High Voltage for SPI	0.7 x VCC*	VCC + 0.4*	V	Only for SPI signals
SPI Vil	Input Low Voltage for SPI	-0.3	0.8	V	Only for SPI signals
SPI Voh	Output High Voltage for SPI	VCC - 0.2*		V	Only for SPI signals
SPI Vol	Output Low Voltage for SPI		0.4	V	Only for SPI signals

*Voltage level to be defined

9. References

DC-MHS Family of Specifications

The Data Center – Modular Hardware System (DC-MHS) family of specifications are written to enable interoperability between key elements of datacenter and enterprise infrastructure by providing consistent interfaces and form factors among modular building blocks. At the time of this publication there are the following specification workstreams:

- **M-FLW** (**M**odular Hardware System **F**ull **W**idth Specification) – Host Processor Module (HPM) form factor specification optimized for using the full width of a Standard EIA-310 Rack mountable server. The specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-DNO** (**M**odular Hardware System Partial Width **D**e**n**sity **O**ptimized Specification) – Host Processor Module (HPM) specification targeted to partial width (i.e. ½ width or ¾ width) form factors. Such form factors are often depth challenged and found not only in enterprise applications but also in Telecommunications, Cloud and Edge Deployments. While the EIA-310 Rack implementation is chosen as a key test case for use, the specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-CRPS** (**M**odular Hardware System **C**ommon **R**edundant **P**ower **S**upply Specification) – Specifies the power supply solutions and signaling expected to be utilized by DC-MHS compatible systems.
- **M-PIC** (**M**odular Hardware System **P**latform **I**nfrastructure **C**onnectivity Specification) – Specifies common elements needed to interface a Host Processor Module (HPM) to the

platform/chassis infrastructure elements/subsystems. Examples include power management, control panel and cooling amongst others.

- **M-XIO** (**M**odular Hardware System E**x**tensible **I/O**) – Specifies the high-speed connector hardware strategy. An M-XIO source connector enables entry and exit points between sources such as Motherboards, Host Processor Modules & RAID Controllers with peripheral subsystems such as PCIe risers, backplanes, etc. M-XIO includes the connector, high speed and management signal interface details and supported pinouts.
- **M-PESTI** (**M**odular Hardware System **Pe**ripheral **S**ideband **T**unneling **I**nterface) – Specifies a standard method for discovery of subsystems, self-describing attributes, and status (e.g., versus a priori knowledge/hard coding firmware and BIOS for fixed/limited configurations). Examples: vendor/module class, physical connectivity descriptions, add-in card presence, precise source to destination cable coupling determination.

To access additional DC-MHS specification please visit <<TBD>>

Additional References

This specification also relies on the following Open Compute Project specifications

- OCP Server Network Interface Card (NIC) 3.0 – Specifies NIC card form factors targeting a broad ecosystem of NIC solutions and system use cases.
  Mezz (NIC) » Open Compute Project
- OCP Datacenter Secure Control Module (DC-SCM) Revision 2.0 – Specifies a SCM designed to interface to an HPM to enable a common management and security infrastructure across platforms within a data center.
  Hardware Management/Hardware Management Module – Open Compute
- SMBus Management Interface Forum. System Management Bus (SMBus) Specification. System. Management Interface Forum, Inc, Version 3.1, 19 Mar 2018
- USB Implementers Forum. Universal Serial Bus Specification, Revision 2.0, April 27th, 2000
- MIPI alliance Specification for I3C Basic℠ v1.1.1 (9-Jun-2021)

10. Trademarks

Names and brands may be claimed as trademarks by their respective companies. I3C is a trademark of MIPI Alliance.

Appendix A - Checklist for IC approval of this specification (to be completed by contributor(s) of this Spec)

This will be filled out at v1.0

Complete all the checklist items in the table with links to the section where it is described in this spec or an external document.

Appendix B - OCP Supplier Information and Hardware Product Recognition Checklist

This is a base specification, and no specific designs can be derived from this specification. Future Design specs will be established based on MHS specifications, and supplier information and HW checklist will be applicable and filled by future contributors