



Open. Together.



OCP
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SUMMIT

Panel: Collaborative Silicon Development

Bapi Vinnakota
ODSA Sub-Project Lead

Distinguished Panelists

“Open is the means to participate in and build something beyond the scope of a single company or individual.”

Brian Allison, IBM: IBM Senior Technical Staff Engineer and Chief Engineer for External Engagements including CAPI and OpenCAPI. Over his 25 year career at IBM, Brian was the Chief Engineer of various industry leading IBM chip sets that spanned cache coherent, memory and node controllers.

Kevin Drucker, Facebook: Sr. Hardware Systems Engineer. Over 26 years of experience in Architecture and Engineering Leadership roles, delivering products across ASIC, FPGAs, PCBAs, software and hardware systems. Domain expertise in Networking, Storage and Compute.

David Kehlet, Intel, Research Scientist, AIB champion, extensive experience leading FPGA, ASIC and IP engineering teams.

Mark Kuemerle, Fellow, Integrated Systems Avera Semiconductor. Broad experience in a wide range of large complex infrastructure ASICs. PHY/Interface workstream leader in the ODSA.

Format

Length: 1 hour

Opening statements: 20 minutes

Q&A (including the audience): 40 minutes

Open Announcements in 2019

Busy year for Open silicon

March, 2019: OCP announces Open Domain-Specific Architecture

March, 2019: Microsoft releases Zipline at OCP Global Summit

March, 2019: CHIPS Alliance announced

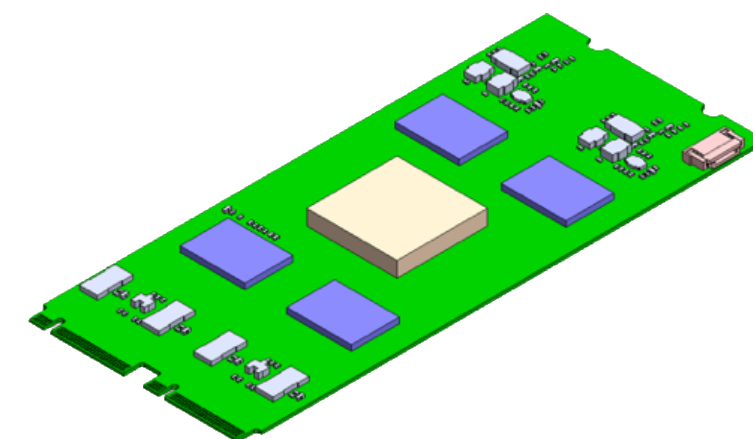
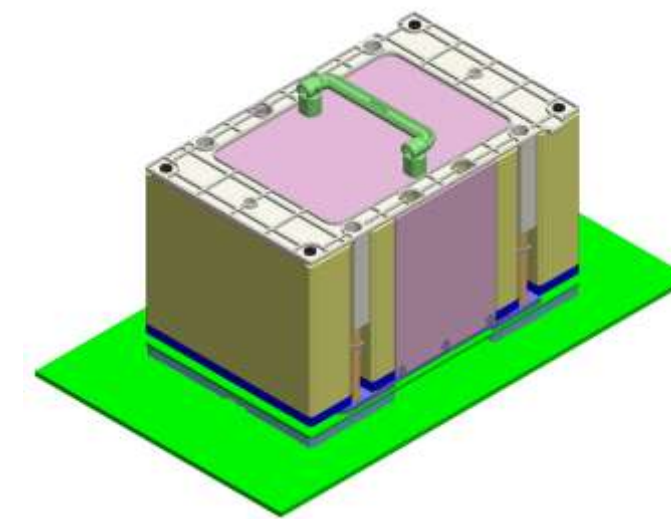
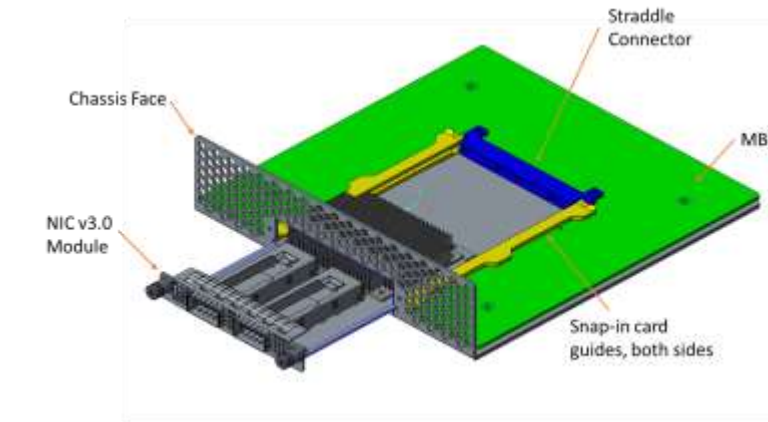
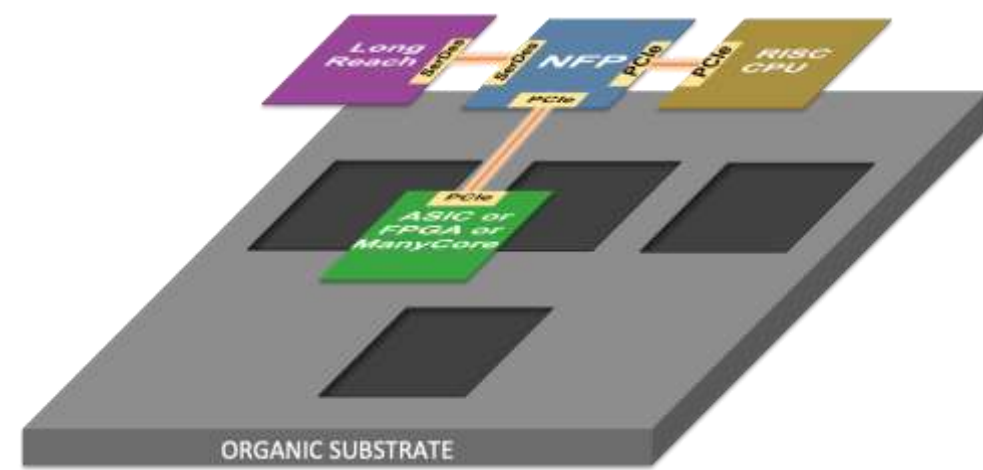
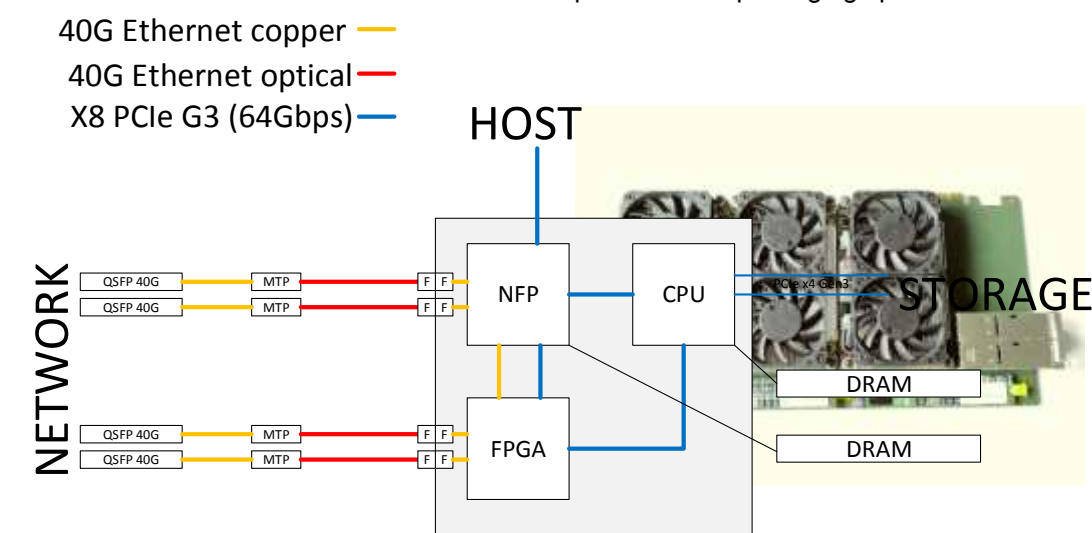
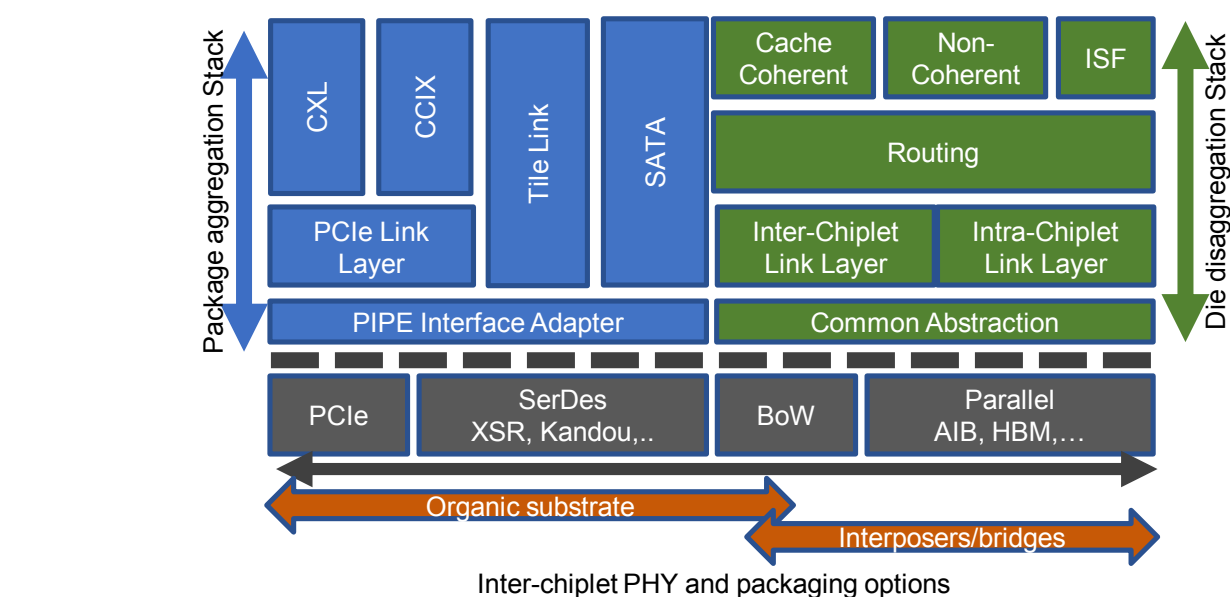
June, 2019: Open Hardware Alliance announced

August, 2019: IBM open sources OpenPower ISA.



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ODSA Goal: Chiplet Marketplace



Chiptlet Marketplace

Collaboration required

ODSA Activities

OCP Use cases

Collaborate on the “Uncore”

Uncore: Everything but the computing core, cache, cache controllers, network i/o, memory i/o, memory controllers.

Kevin: How does Open IP get used

Mark: Packaging, test

Brian: Security

Dave: Best IP to build a product around

Collaborative Silicon Development Panel: “Acceptance Criteria, How does IP get used”

Kevin Drucker, Sr. Hardware Systems Engineer, Facebook

Sustainable Chiplet Business Model

- **Challenge:** Viability of an Open “Chiplet” Eco-System requires the development of funding and revenue models that yield a sustainable business model for “Chiplet” suppliers, consumers and SIP end-users.
- **Key Considerations:**
 - Evolution of / Analogous to “soft” and “hard” IP industry
 - Potentially similar funding and revenue models to IP development
 - Caveat: deliverable is the ultimate “hardened” IP → Chiplet
 - Must be a value add: for example - each Chiplet could target best Si node for optional PPA.
 - Longevity for IP investment → Leverage proven Chiplets across nodes

Coalesce Around Common Interfaces

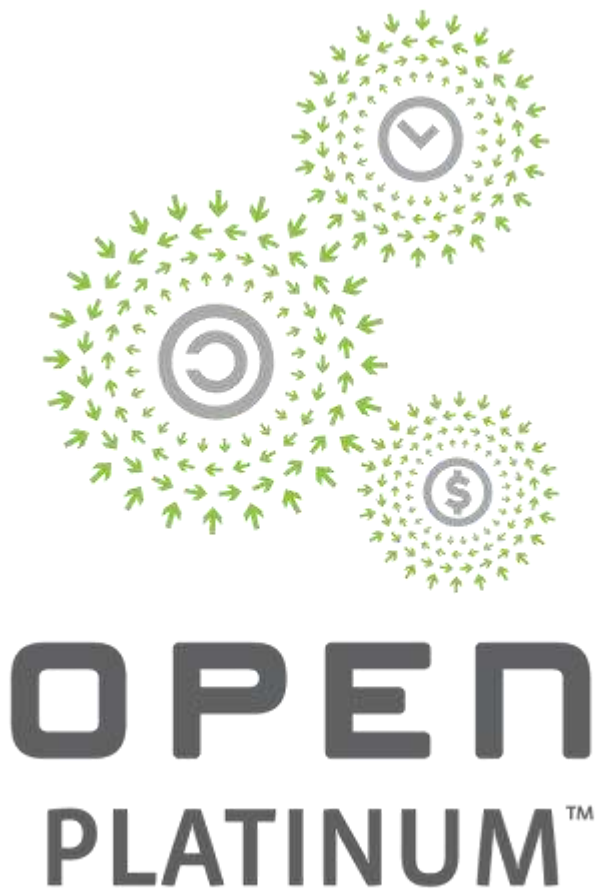
- **Challenge:** Industry coalescing around common die-to-die (d2d) interfaces can help jump start the Chiplet Eco-system
- **Extending the IP analogy:**
 - Common interfaces have helped build a robust IP ecosystem
 - Key examples of success through common interfaces:
 - PIPE (Physical Interface for PCI-Express): originally developed for PCIe
 - Now used as PHY / Link Layer interface for PCIe, CXL, USB, etc.
 - DFI (DDR PHY Interface): Interface between Memory controller / Memory PHY
 - Opened the door to integrating best in class Memory controller IP and Memory PHY IP... even if from different suppliers
 - AXI (Advanced eXtensible Interface): Originally developed for embedded CPU / Peripheral interconnect, now used across a **massive** eco-system of IP products

“Open” Makes SIP Integration “Easier”

- **Challenge:** A robust **open** eco-system where 3rd party and captive Chiplets co-exist and integrate into SIP products requires collaboration across a number of fronts:
- **Key Considerations for Acceptance:**
 - Readily adoptable d2d interfaces, protocols and stacks
 - **Open** set of common deliverables available for a Chiplet product
 - Support for **Open** standards for Known Good Die (KGD)
 - Support for **Open** standardized testability buses / DFT strategies (for example, something like IEEE-1500) for successful SIP manufacturing test
 - **Open** Chiplet data exchange formats may facilitate broad participation in integration tooling

Who's not on the panel?

Mark Kuemerle
ODSA Standards
Avera Semi

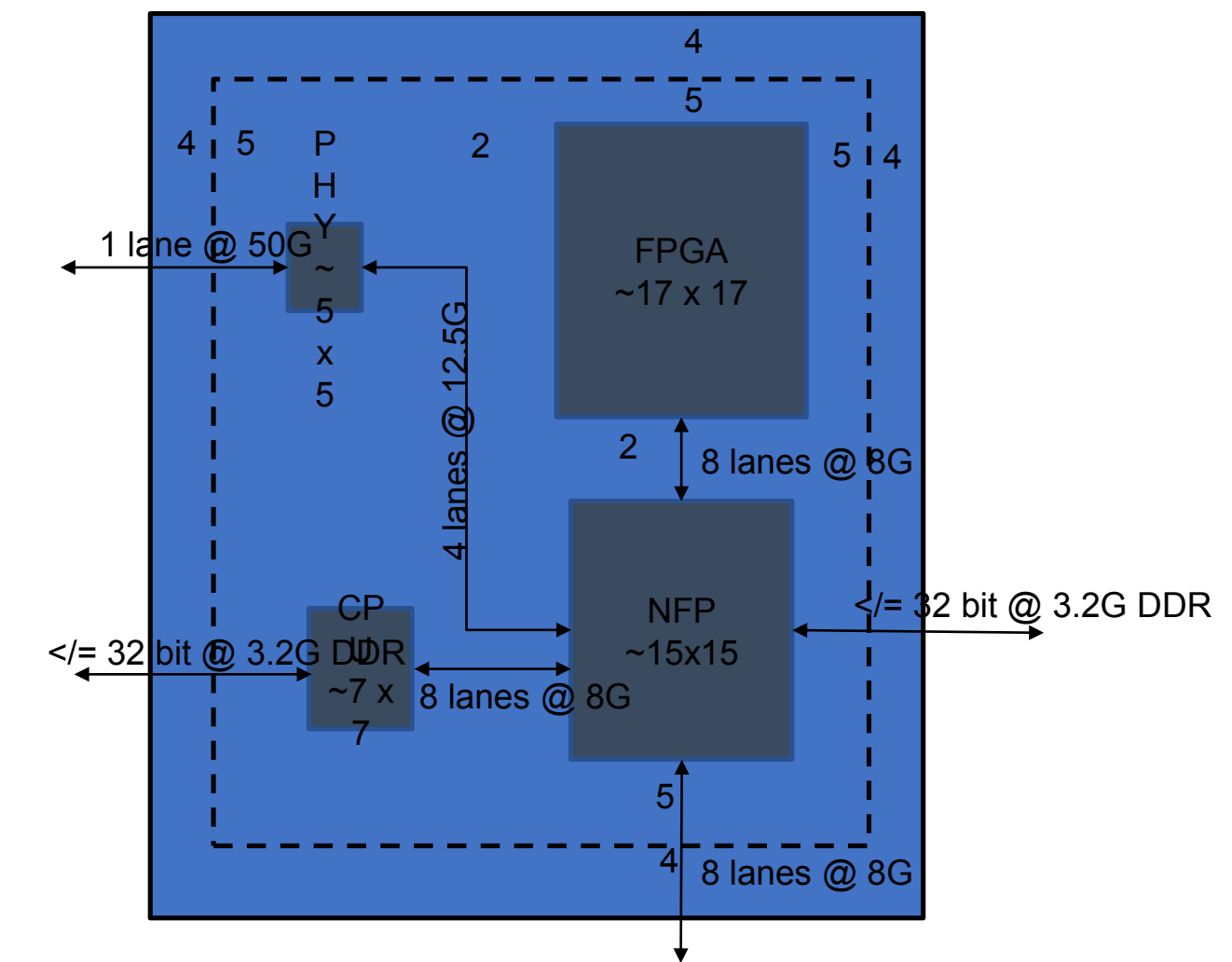


Who's not here?

Two of our biggest challenges are packaging and test:

Packaging... is covered later – come back tomorrow

Test is one of our biggest needs ... please help



Test

Goal is to incorporate what we already have standards for:

- Leverage standards (IEEE 1149.1, 1149.6) to map from board level testing to SiP level testing
- Incorporate IEEE 1500 standards from HBM-type systems
- IO PLL/DLL lock and calibration
- At speed test (loopbacks, etc)

Challenges

- Fine bump pitches for higher bandwidth interconnect
- Tiny drive / IO
- Enumeration, ordering
- BER – when to use FEC, when not to

Please chip in to help address these challenges

Panel: Collaborative Silicon Development - Security

Brian Allison, IBM, Senior Technical Staff Member

Open Domain Hardware

- The world is now embracing the concepts of Open Domain Hardware beyond form factors etc
 - This is now including Open Source RTL
 - Much like what has been happening in the Software Domain for quite some time with Linux
 - We are seeing this in the CHIPs Alliance with a number of hardware companies participating as an example
 - Other examples are ODSA etc
- Even IBM is starting to show it's interest in the arena with what was recently announced at the Linux Foundation meeting in San Diego
 - Moving OpenPower under the Linux Foundation
 - Opening up the ISA and releasing an initial ISA implementation on github
 - Open Sourced 3 Hardware Initiatives also on github
 - Open Memory Interface (OMI) Host FPGA Reference Design
 - Open Memory Interface (OMI) Device FPGA Reference Design
 - OpenCAPI 3.0 Device Side FPGA Reference Design

Open Domain Chiplets

- What would the folks in the chiplet world be asking for?
 - Establish a catalog of trusted chiplets because it's going to be hard as a consumer of chiplets to know how to avoid malicious chiplet designs
- An important point to consider
 - Virtual vs physical addressing
 - If a chiplet gets access to physical addresses then a new set of security issues around design bugs surface since that chiplet now has hypervisor-like access in the system
 - This is in addition to malicious chiplet designs

Why do I care about Virtual Addressing?

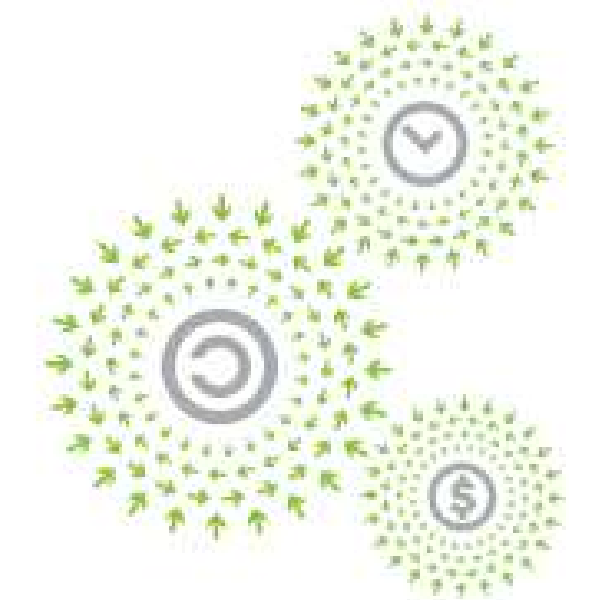
- **An OpenCAPI device operates in the virtual address spaces of the applications that it supports**
 - Eliminates kernel and device driver software overhead
 - Everything runs in User Space
 - Allows device to operate on application memory without kernel-level data copies/pinned pages
 - Simplifies programming effort to integrate accelerators into applications
 - OpenCAPI API is very simple to understand and leverage
 - Culmination => Improved Overall Application Performance
- **The Virtual-to-Physical Address Translation occurs in the host CPU**
 - Makes it easier to ensure **interoperability between OpenCAPI devices and different CPU architectures**
 - Example would be that NVLINK 2.0 and OpenCAPI play in the same Shared Virtual Memory
 - Allows for efficient communication between GPU and Accelerators
 - **Security** - Since the OpenCAPI device never has access to a physical address, this **eliminates the possibility of a defective or malicious device accessing memory locations belonging to the kernel or other applications that it is not authorized to access**

Trusted Chiplet IP

- How does a consumer verify that a chiplet is trusted and understood?
 - Possible avenue to to verify integrity of chiplet(s)?
 - Cadence OASIS Compares
 - Testbench patterns included with Chiplet IP
 - Others?

Collaborative Silicon Development Panel: “Best IP for Building a Product”

David C. Kehlet, Research Scientist, Intel Corporation



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“Best IP for Building a Product”

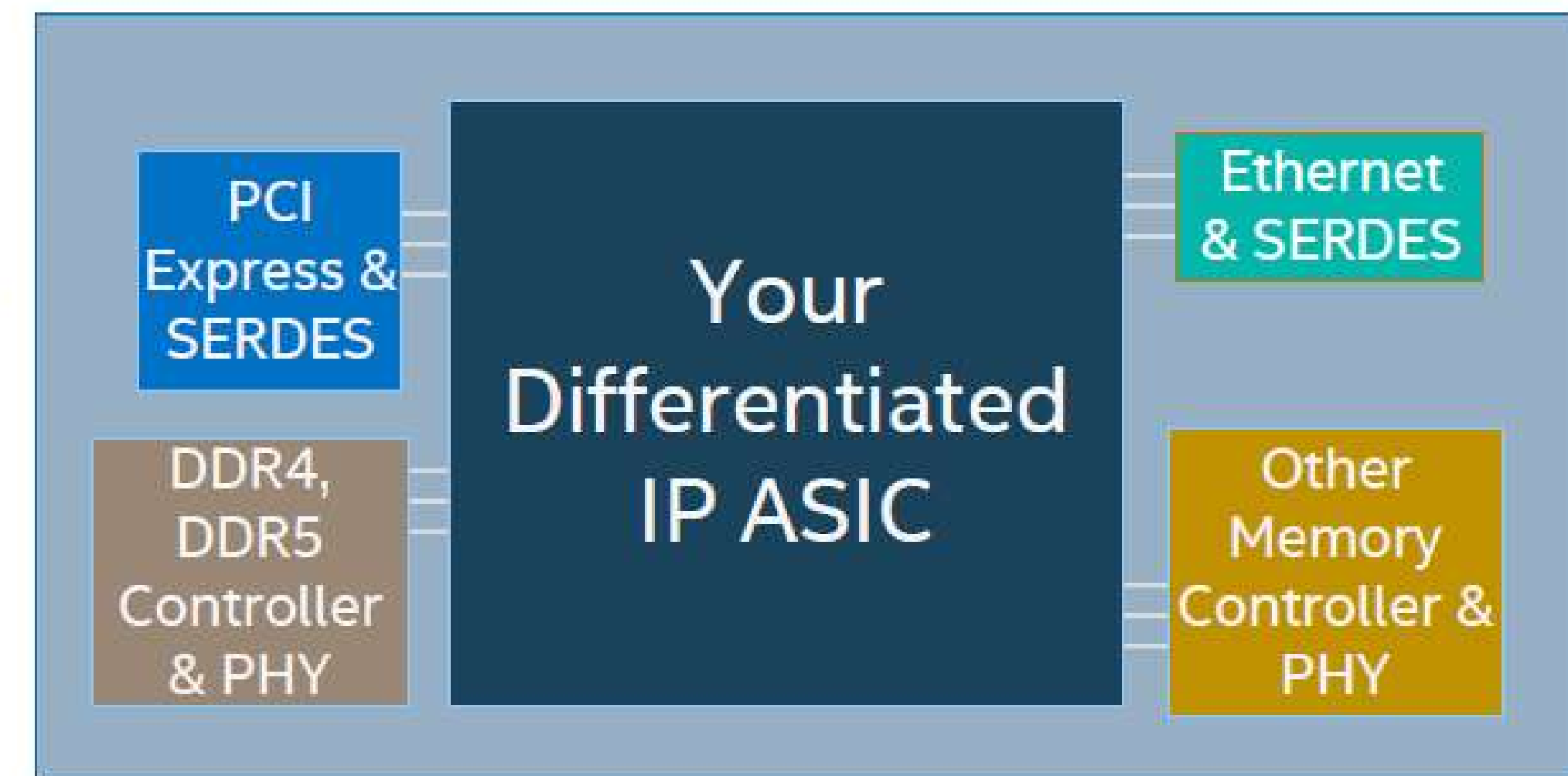
→ ***Best IP to Build Around your Product!***

Chiptlets for I/O Connectivity

- PCI Express
 - or CXL: cache data from CPU host memory, host can access local memory
- Ethernet
- ADC/DAC
- Photonics

Chiptlets for Memory System

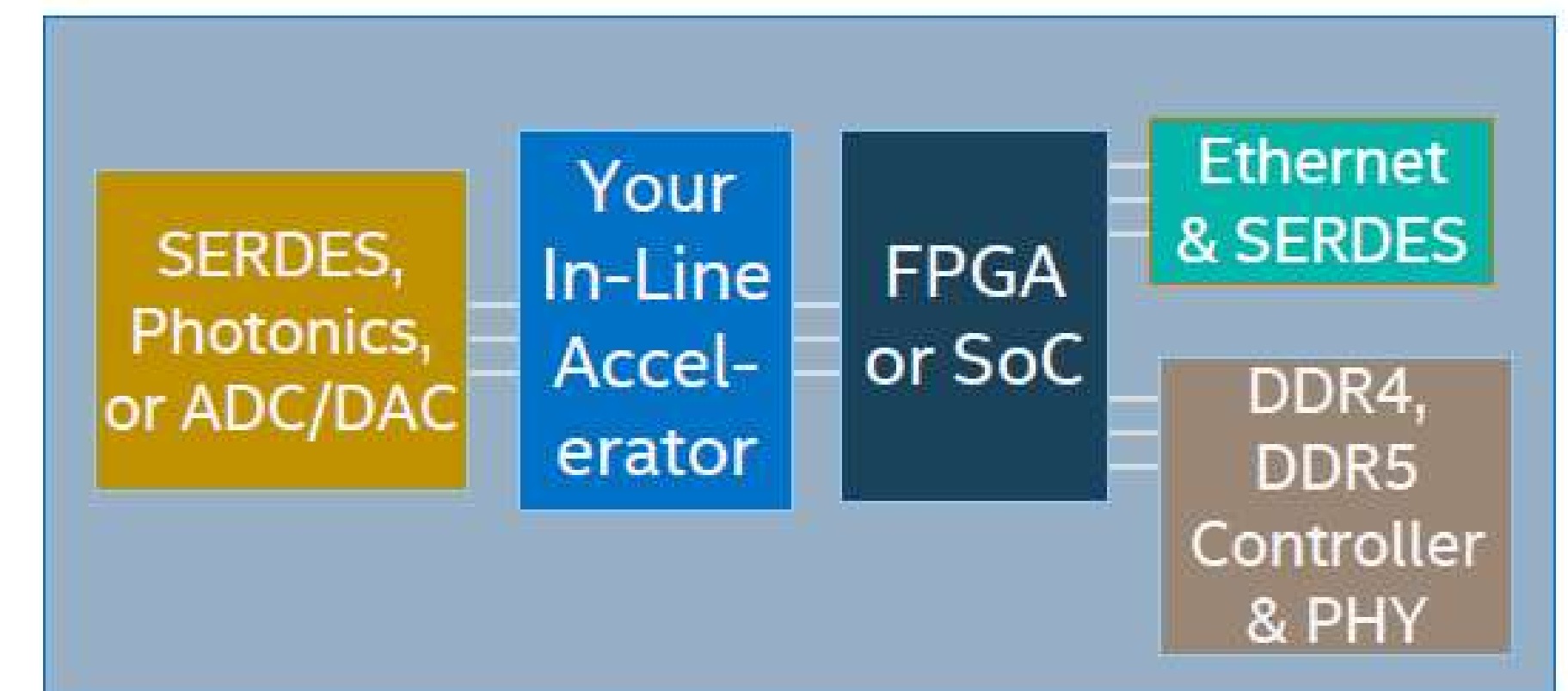
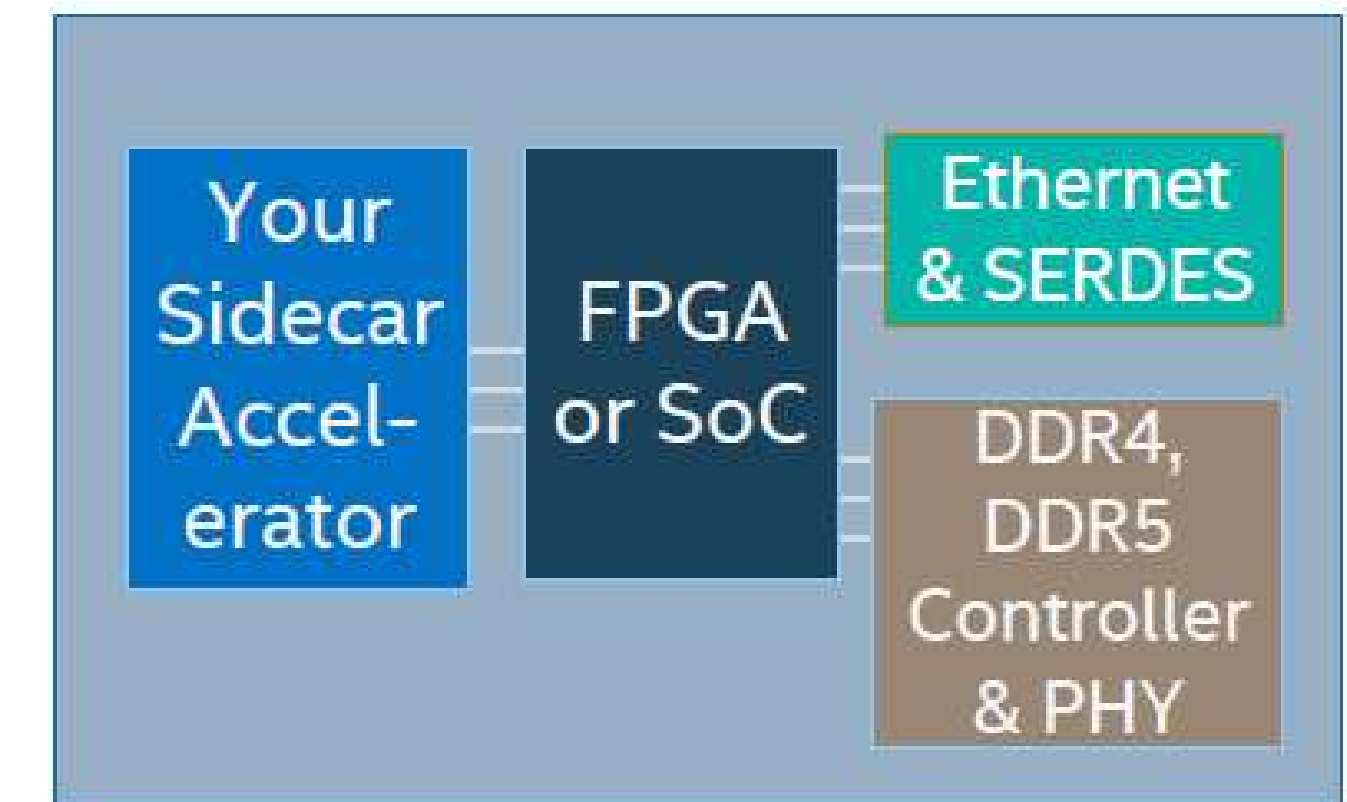
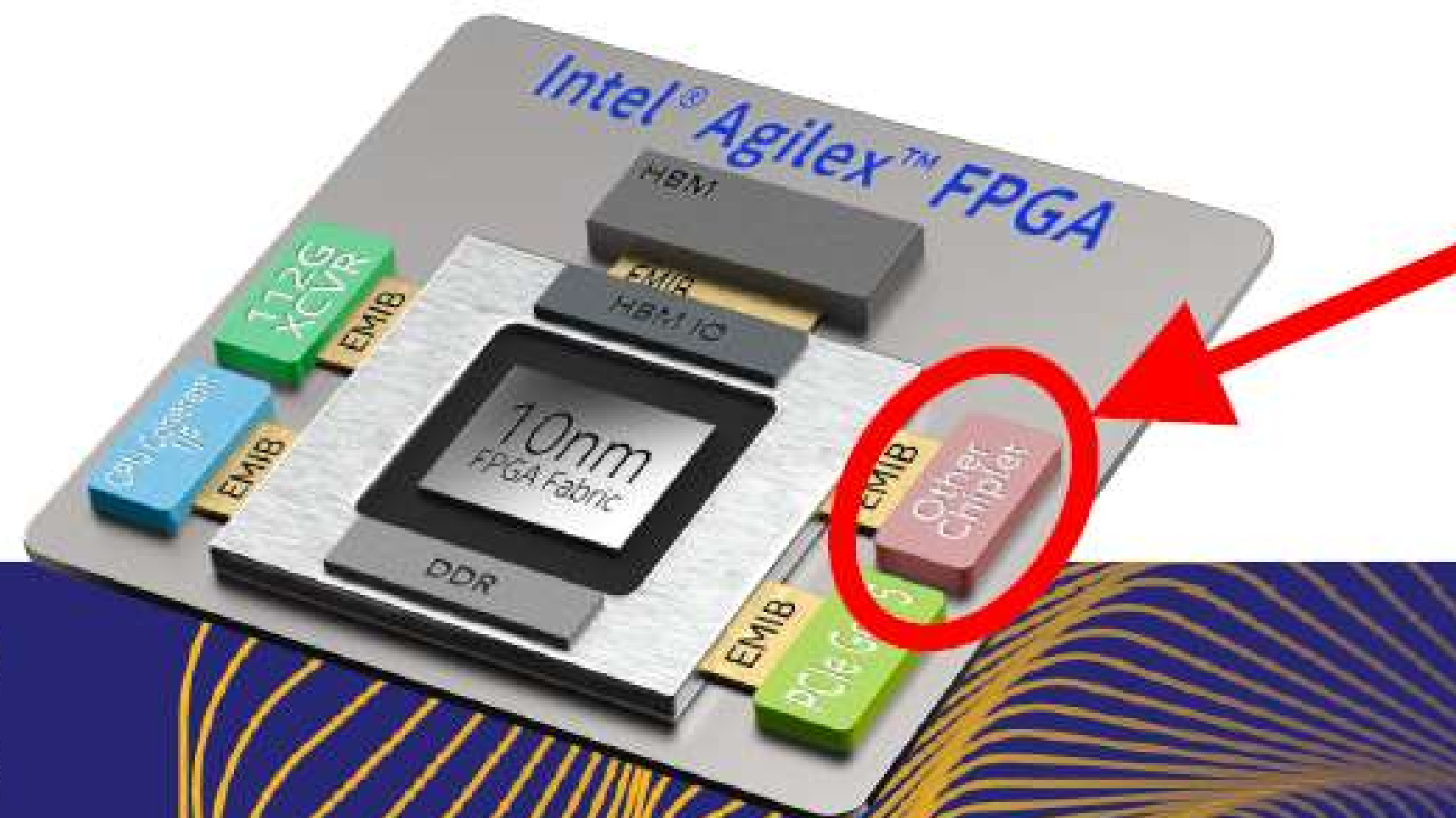
- DDR4, DDR5
- GDDR6? MRAM? HBM2/3?



“Best IP for Building a Product”

Or use an SoC or FPGA for connectivity

- Low latency, high bandwidth chiplet connection works well for accelerators
- Sidecar and In-Line configurations

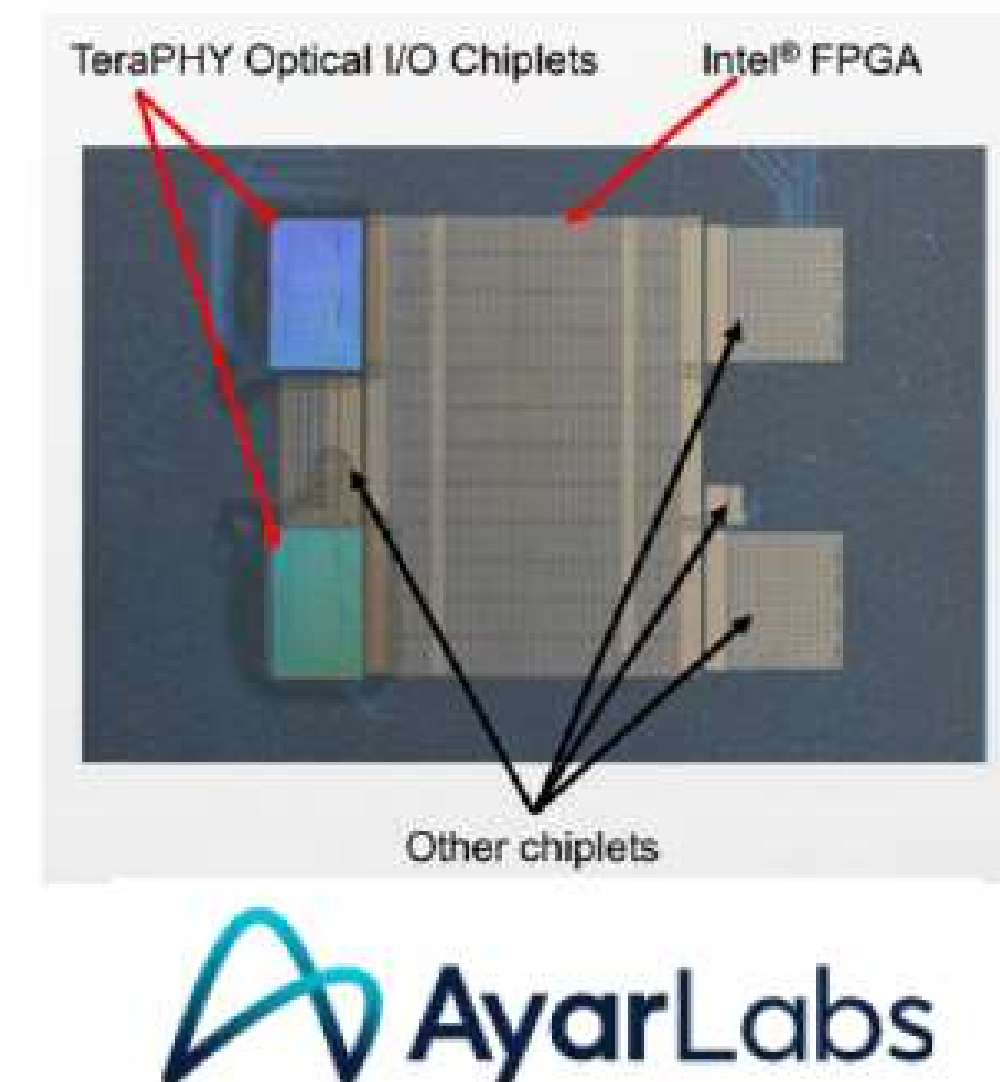


IP as Part of a Large Solution

“How can you participate in and build for a market with a solution that's too large for any one company to handle?”

Focus: What is your unique value?

Partners: Chiplet IP, Device Integrator, System developer, Application developer, End user



Jariet direct RF sampling at up to 64Gsp/s,
ADC/DAC ACT IP is

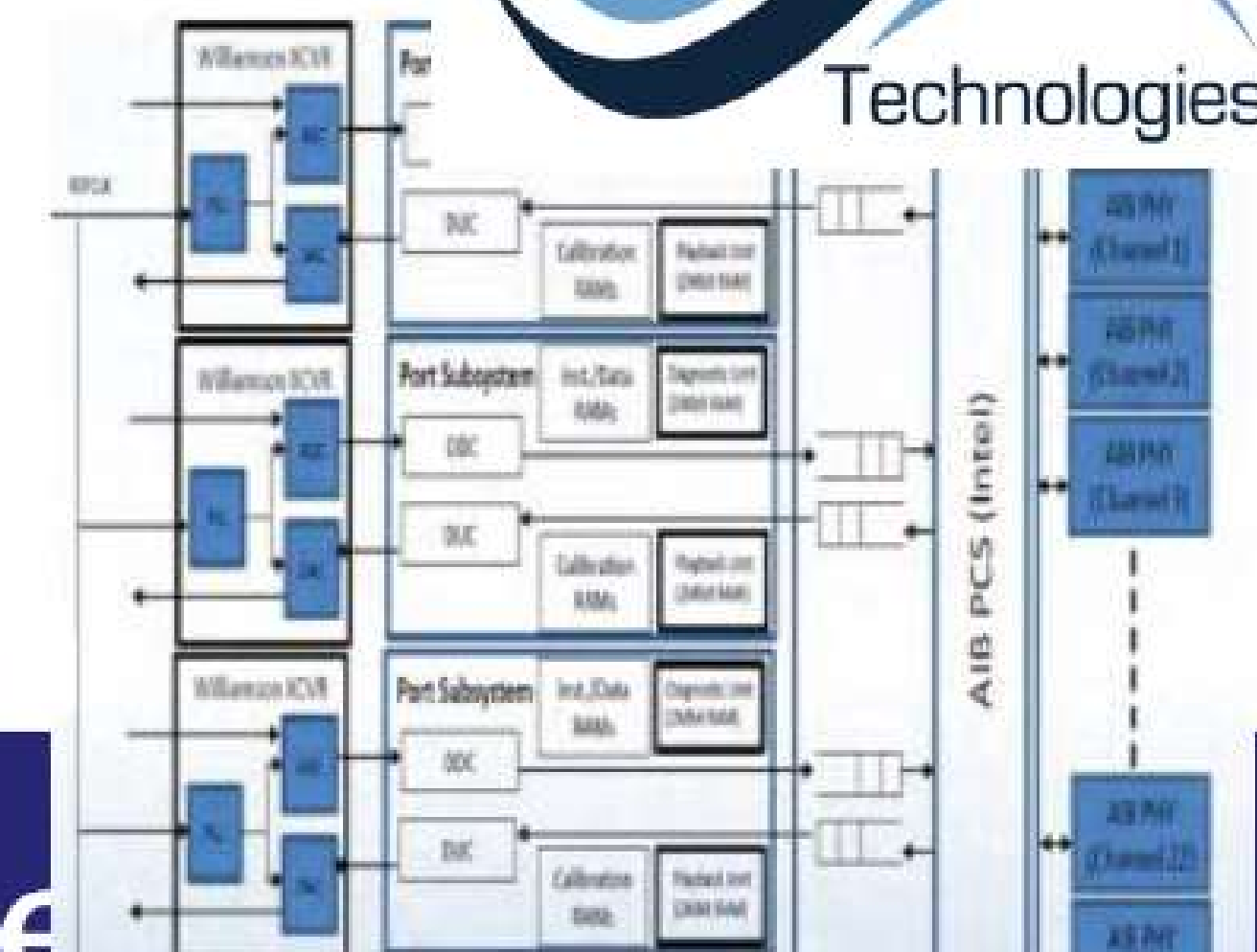


Image sources: Ayar Labs, Jariet Technologies



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