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UBB: Universal Baseboard for OCP Accelerator Module

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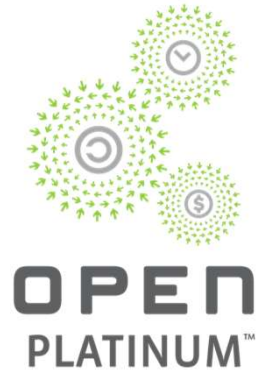

Agenda

- OAI Overview
- Why UBB?
- UBB Spec Overview
- UBB ME Assy.
- UBB Interconnect Topology
- Electrical Spec.
- Call for Action

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Specifications

OAI Overview

- ***OAM*** is an Open Accelerator Module for multiple suppliers
- A multi-OAM, Universal Baseboard (***OAI-UBB***) for various Interconnect Topologies
- Host Interface Board (***OAI-HIB***)
- Power Distribution Board(***OAI-PDB***)
- A Datacenter-ready, System- and Rack-level Security, Control, and Management (***OAI-SCM***) for all Chassis, Trays, UBBs, and OAMs as well as the Hosting Head Node
- OAI Expansion Beyond UBB (***OAI-Expansion***). May include PCIe CEM Slots or similar or may expand directly from UBB or OAM
- ***Tray*** for sliding a collection of OAMs (different UBBs)
- System ***Chassis***, Power, and Cooling (different Trays)

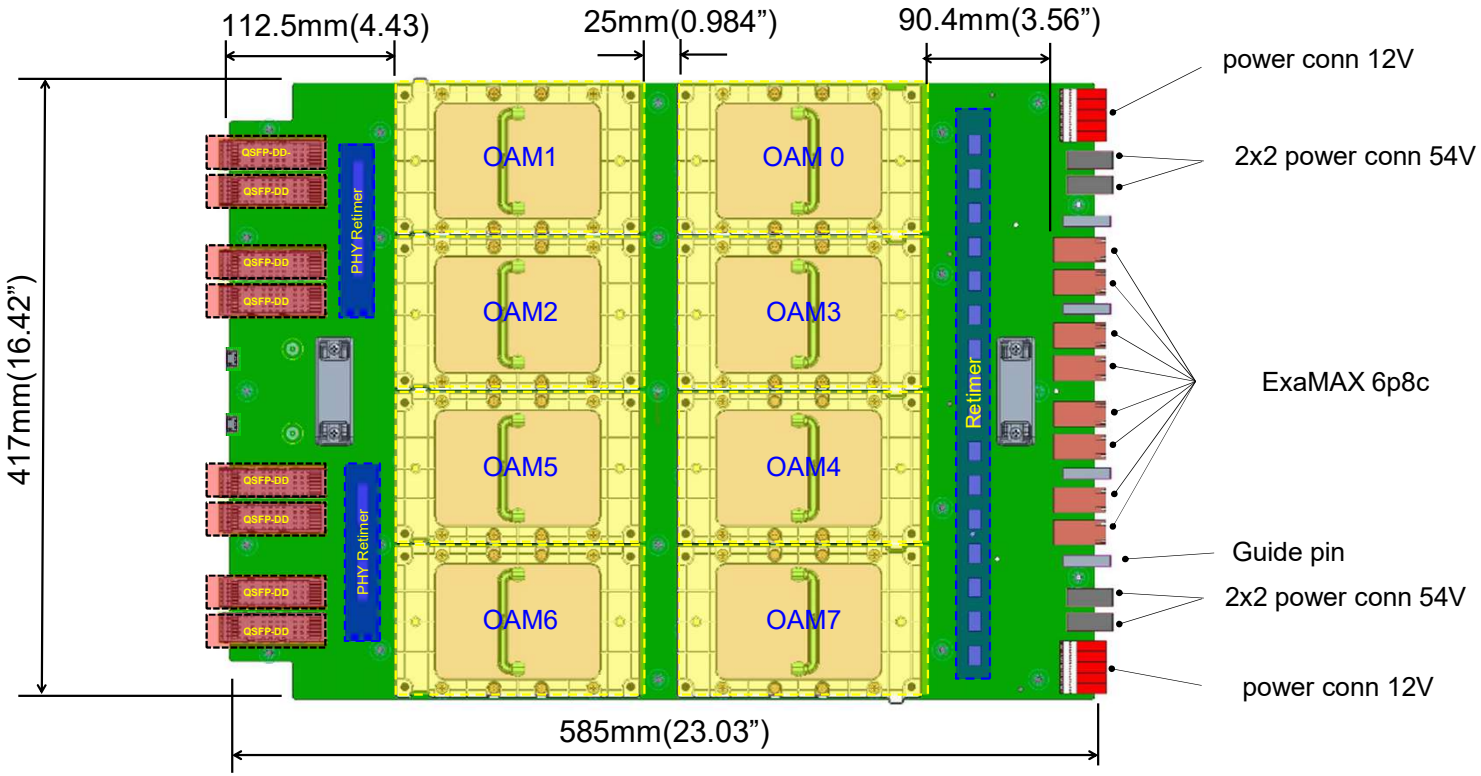
Why do We Need UBB?

- Part of OAI initiative
- Provide common interface for a multi-OAM, various interconnect topology baseboard
- Interchangeable to different OAM reference systems

What do we need to define in UBB

- 8* OAMs in UBB
- Interconnect topology
- Host Interface with retimers
- Scale-out with Phy retimers
- 12V or 54V/48V power delivery
- 19’’ and 21’’ rack compatible
- Debug/management interface

UBB with OAMs

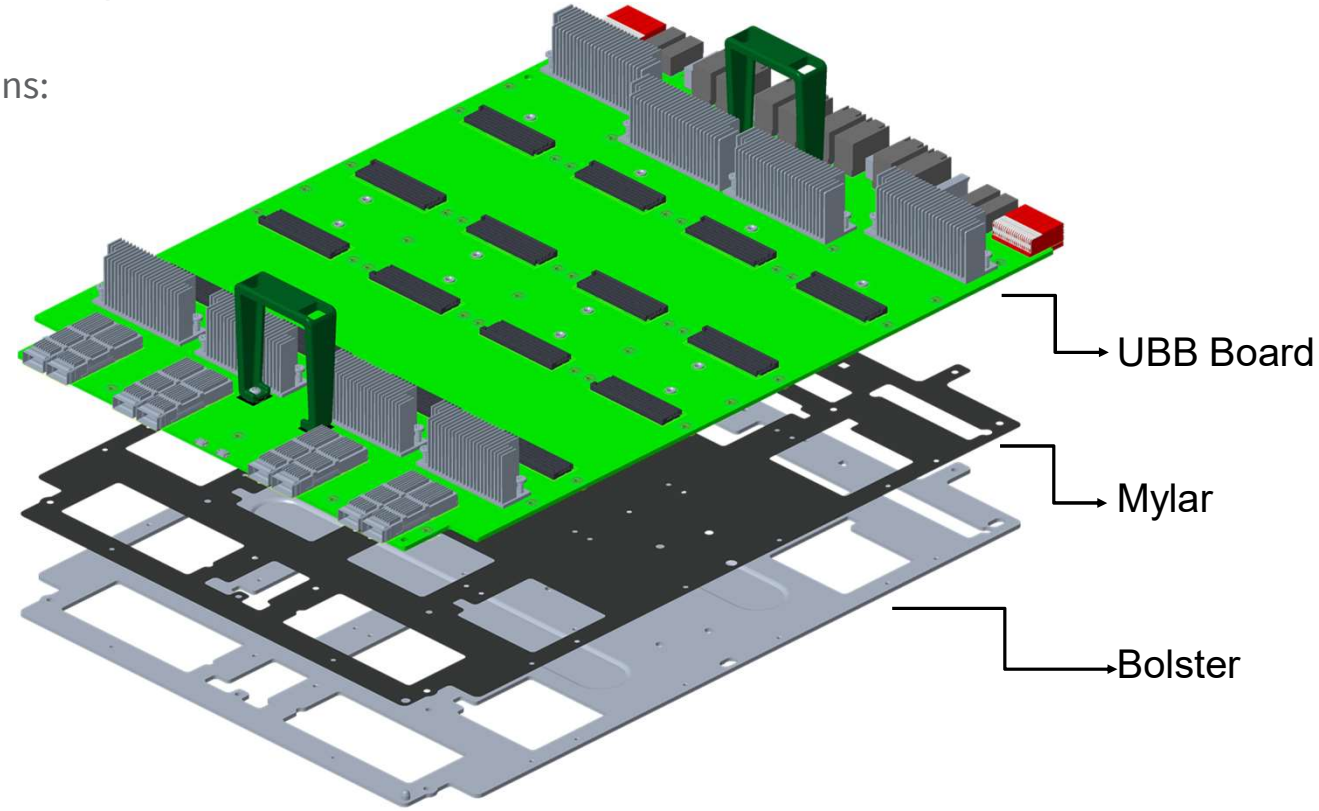


Spec Overview

Item	Feature
UBB Dimension	585mm(L) x 417mm(W) x 3.26mm
OAM	8x OAM 12V up to 300W TDP 54V/48V up to 500W TDP
Host Interface	8 X16 Serdes, with retimers
Interconnect SerDes Speed	Up to 28Gbps NRZ or 56Gbps PAM4
Interconnect Topology	Various *UBB reference designs support FC(Fully Connected) or HCM(Hybrid Cube Mesh)
Connectors to HIB	4x 54V/48V AirMax 2x P12V PwrMax 8x ExaMax (high speed and side bands)
Scale out	8x QSFP-DD with retimers (up to 28Gbps NRZ or 56Gbps PAM4 Serdes interface)
Debug/Management/Security	JTAG/I2C/UART to microUSB2.0/Vendor proprietary

Mechanical Assy.

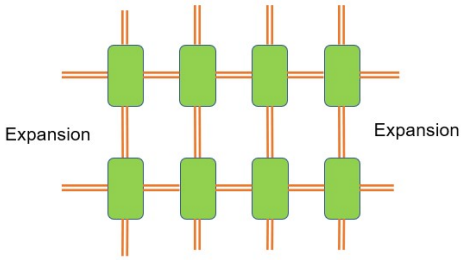
- UBB mechanical assembly contains:
  - UBB
  - Mylar
  - Bolster design illustrated.
    - Bolster is 4mm thickness.

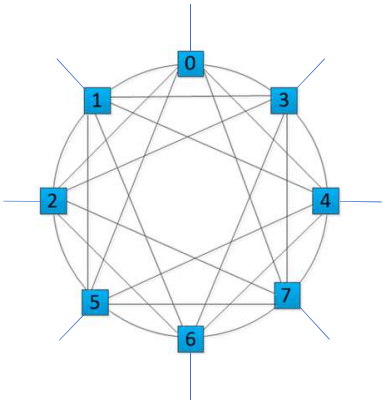


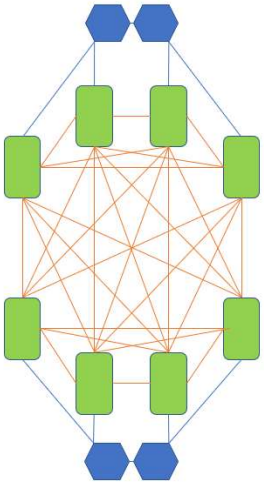
Interconnect Topology

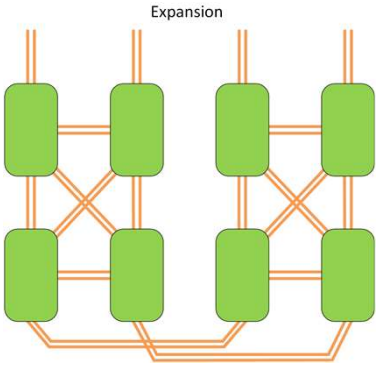
Interconnect Topology

- UBB can support various topologies



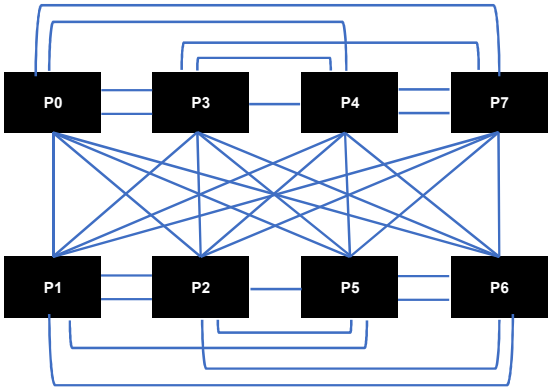


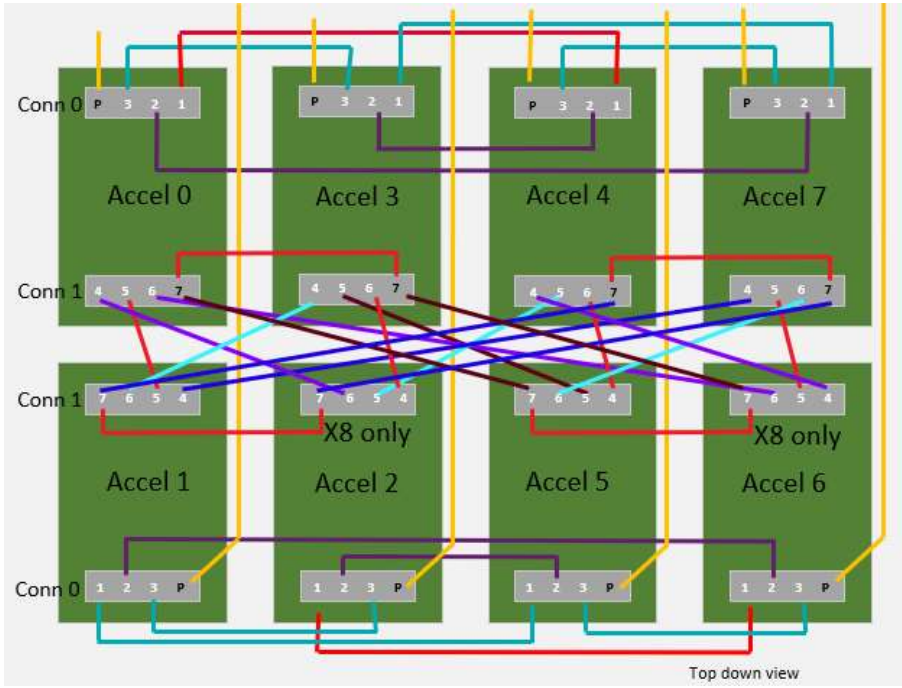




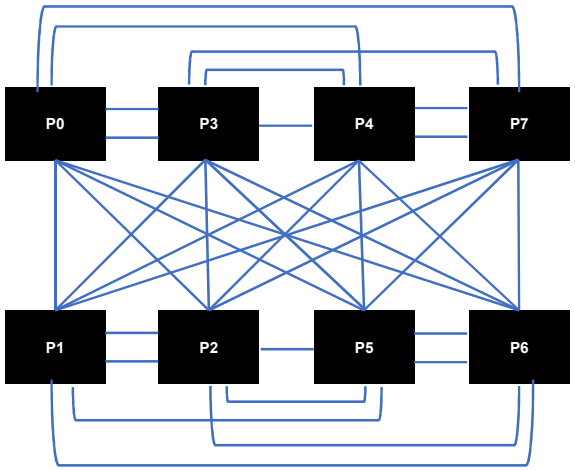
What is UBB Reference Board Topology?

1) Combined FC/6-port HCM Topology

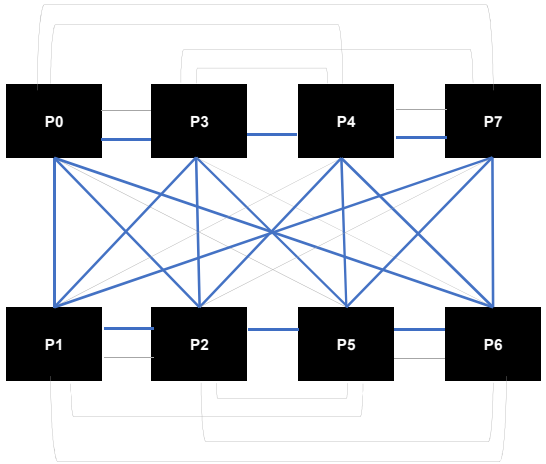




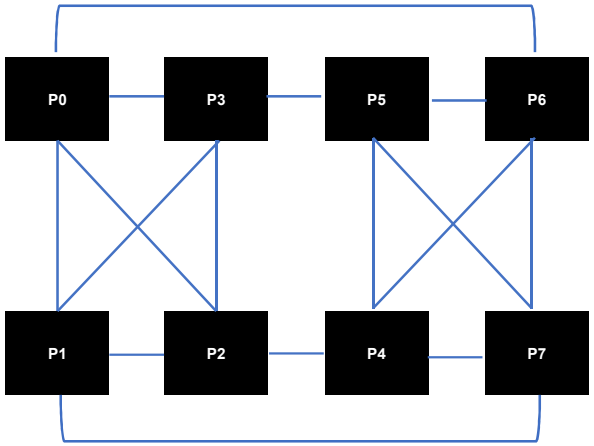
How does HCM Embedded?



Superset topology



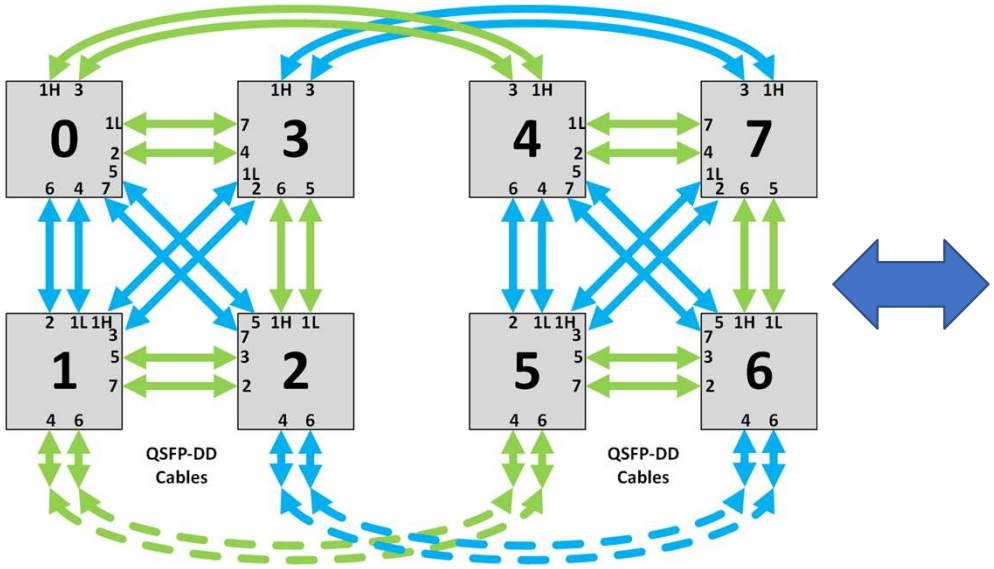
Hide unused links

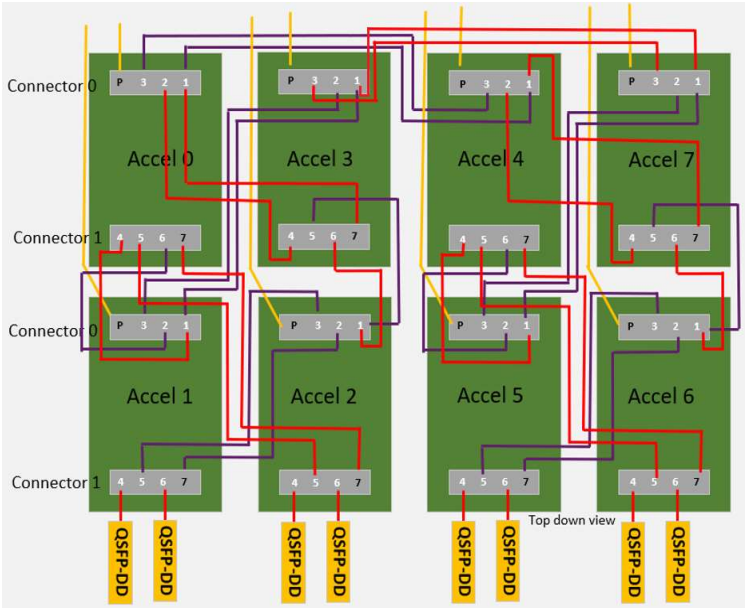


Rotate 4,7,5,6 by 180°
➔ HCM

What is UBB Reference Board Topology?

2) 8-port HCM





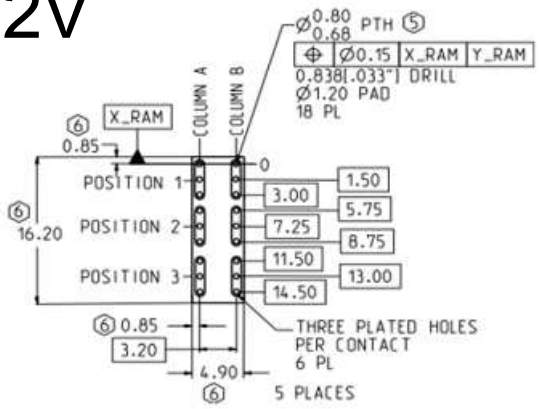
Electrical Spec.

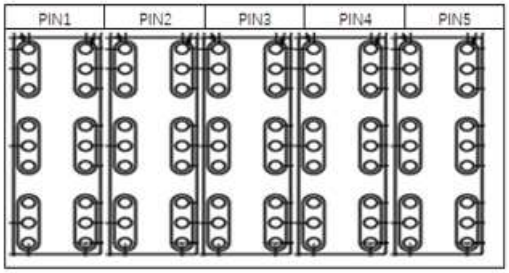
UBB to HIB Signal List

High Speed Examax connector signals							
No.	Signal Function	Diff (Pair)	Single End	Pin Count	Power Source	IO Type	Description
1	Host Bus	256		512	Main	I/O	8 x16
2	Serdes Link Bus	8		16	Main	I/O	Reserve for Serdes Link x4 to Switch
3	Diff Clock	3		6	Main	I	1. PCIe 100MHz Clock 2. Aux PCIe 100MHz Clock 3. 100MHz Clock
4	JTAG		5	5	STBY	I/O	1. BMC JTAG: JTAG_TMS, JTAG_TRST, JTAG_CLK, JTAG_TDI, JTAG_TDO
5	JTAG CTRL		10	10	STBY	I	1. SEL[3:0]: OAM Selection 2. CPLD[1:0] Primary and Secondary JTAG Enable 3. JTAG MUX0/1 Enable 4. JTAG MUX0/1 Selection
6	I2C Bus		10	10	STBY	I/O	1. P12V eFuse and FRU 2. OAM Slave SMBus and I2C GPIO 3. PCIe Retimer and CLK Buff 4. CPLD and UBB Temp Sensors 5. CPLD FW Update
7	EEPROM Write Protect		4	4	STBY	I	1. Retimer: EEPROM[1:0] Write Protection 2. UBB: FRU[1:0] Write protection
8	SMBus ALERT		3	3	STBY	O	1. CPLD and Temp Sensor Alert 2. OAM Slave Alert 3. P12V eFuse Alert
9	FRU SEL		1	1	STBY	I	Accel FRU Selection: OAM and Accel FRU
10	RESET		9	9	STBY	I	1. HIB: OAM PERST#, 2. HIB: OAM WARMRST[3:0]# 3. HIB: SW[3:0] PCIe Reset
11	PWR BRAKE		1	1	STBY	I	PWR_BRAKE#
12	UART		2	2	STBY	I/O	UART for OAM debug via BMC
13	UART CTRL		4	4	STBY	I	1. UART Selection [2:0] 2. UART Mux enable
14	Power Button		1	1	STBY	I	Accel system power control w/o Switch board
15	UBB PRESENT		2	2	STBY	I/O	1. PRSNT1 short to PRST2 in UBB 2. At HIB, PRSNT1 short to GND through 100ohm, PRST2 pull up to 3.3V through 4.7K resistor.
16	P3V3_AUX			4	STBY	P	Standby Power from HIB
17	GND			4		G	P3V3_AUX return path ground
18	GPIO		20	20	STBY	I/O	1. PRI CPLD: GPIO[15:0] between CPLD and BMC in future. 2. SND CPLD: GPIO[3:0] between CPLD and BMC
19	NC			154		NA	
Total Pin Count				768			No include signal return ground

Power Connectors

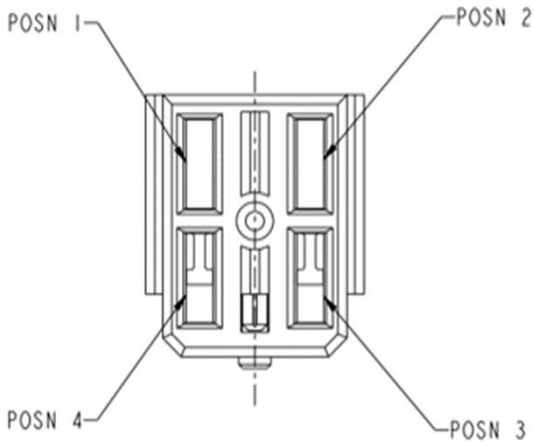
12V





LEFT CONN	PIN 1		PIN 2		PIN 3		PIN 4		PIN 5	
	Column A	Column B	Column A	Column B	Column A	Column B	Column A	Column B	Column A	Column B
POSN3	P12V_0	P12V_0	P12V_0	P12V_0	P12V	P12V	P12V_1	P12V_1	P12V_1	P12V_1
POSN2	P12V_0	P12V_0	GND	GND	GND	P12V	GND	GND	P12V_1	P12V_1
POSN1	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND

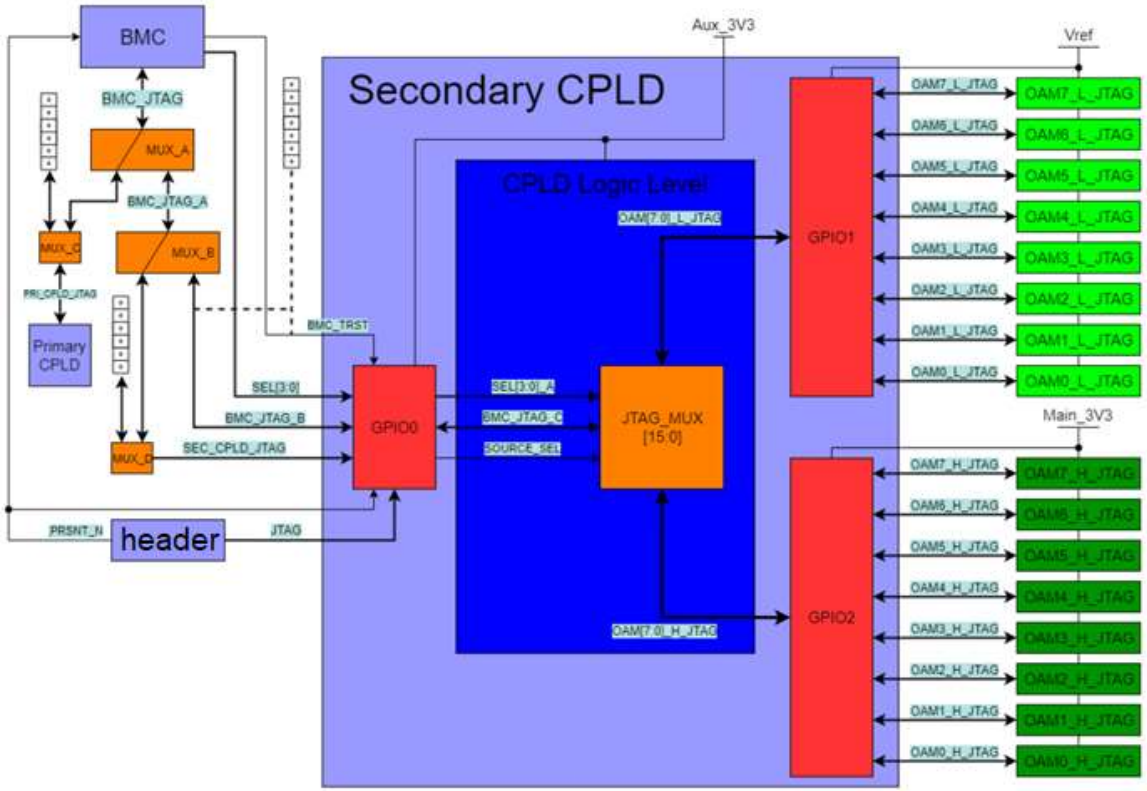
RIGHT CONN	PIN 1		PIN 2		PIN 3		PIN 4		PIN 5	
	Column A	Column B	Column A	Column B	Column A	Column B	Column A	Column B	Column A	Column B
POSN3	P12V_2	P12V_2	P12V_2	P12V_2	NA	NA	P12V_3	P12V_3	P12V_3	P12V_3
POSN2	P12V_2	P12V_2	GND	GND	NA	NA	GND	GND	P12V_3	P12V_3
POSN1	GND	GND	GND	GND	NA	NA	GND	GND	GND	GND



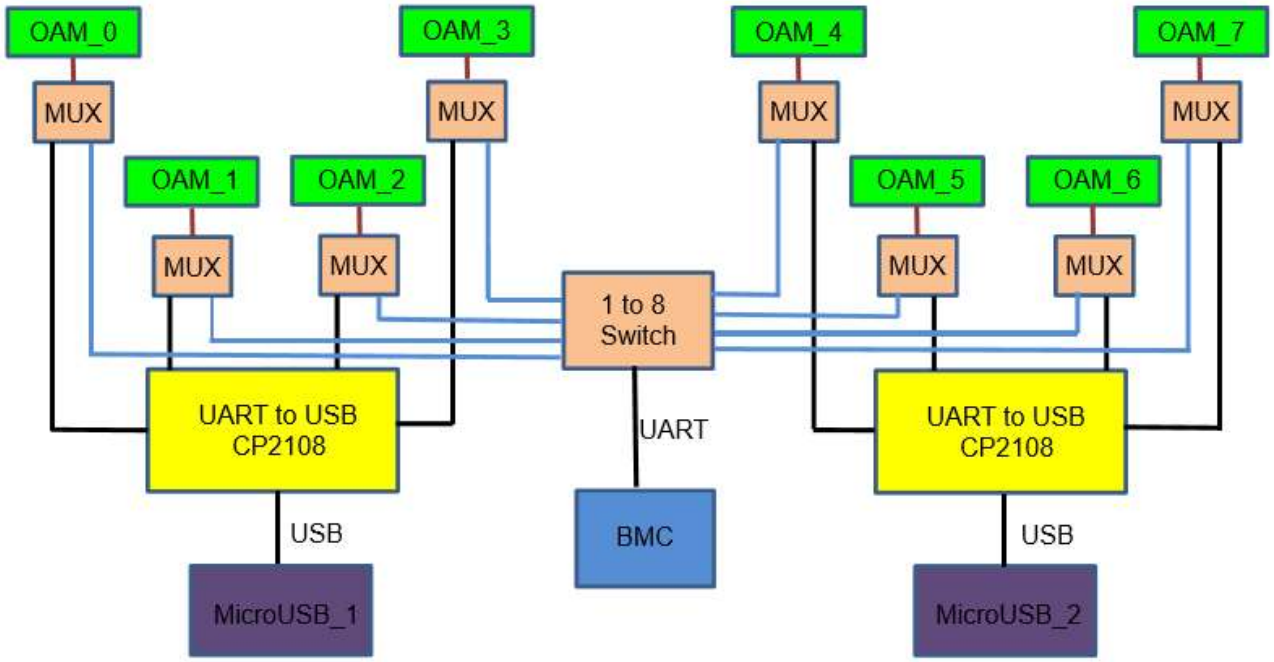
POS 1 & 2	54V
POS 3 & 4	GND

54V/48V

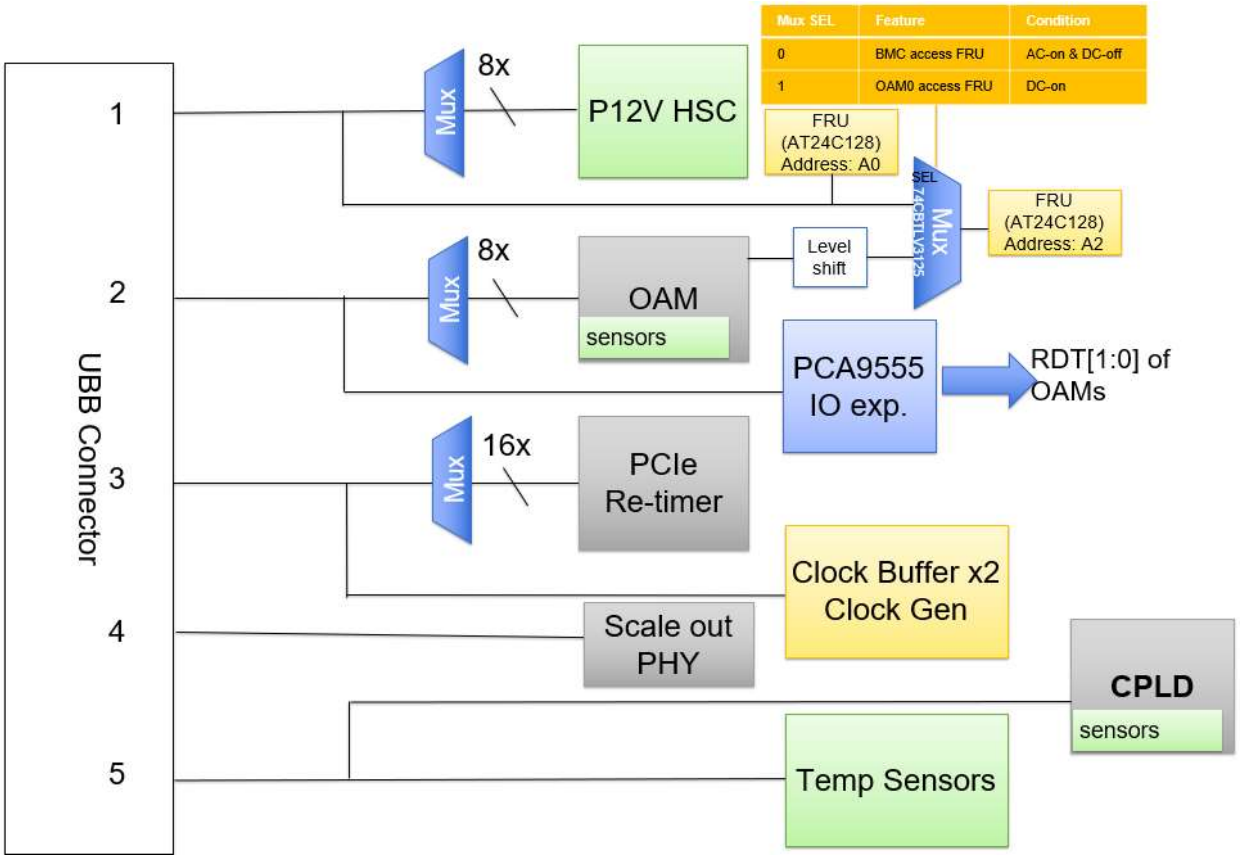
Debug Interface - JTAG



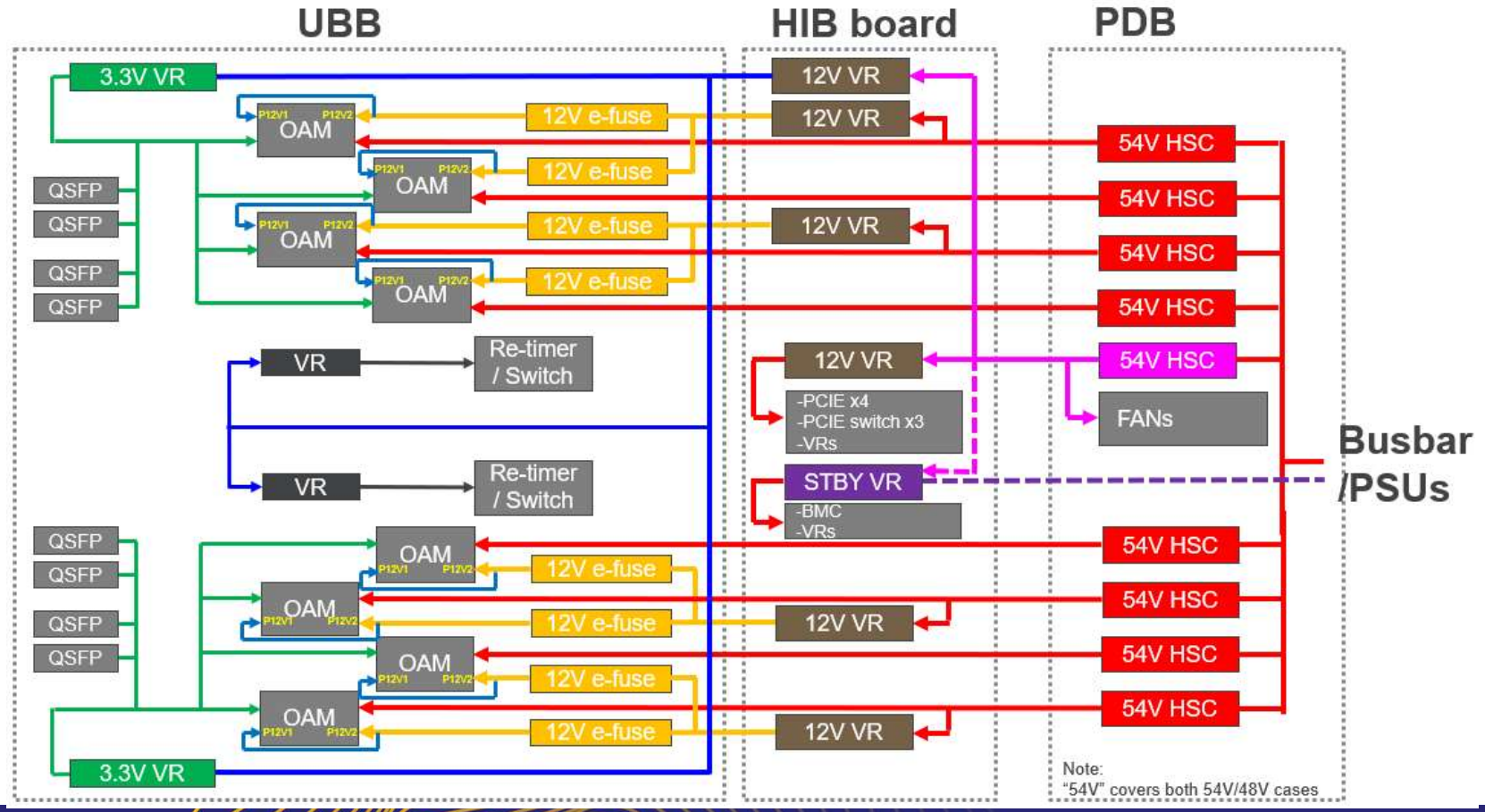
Debug Interface - UART



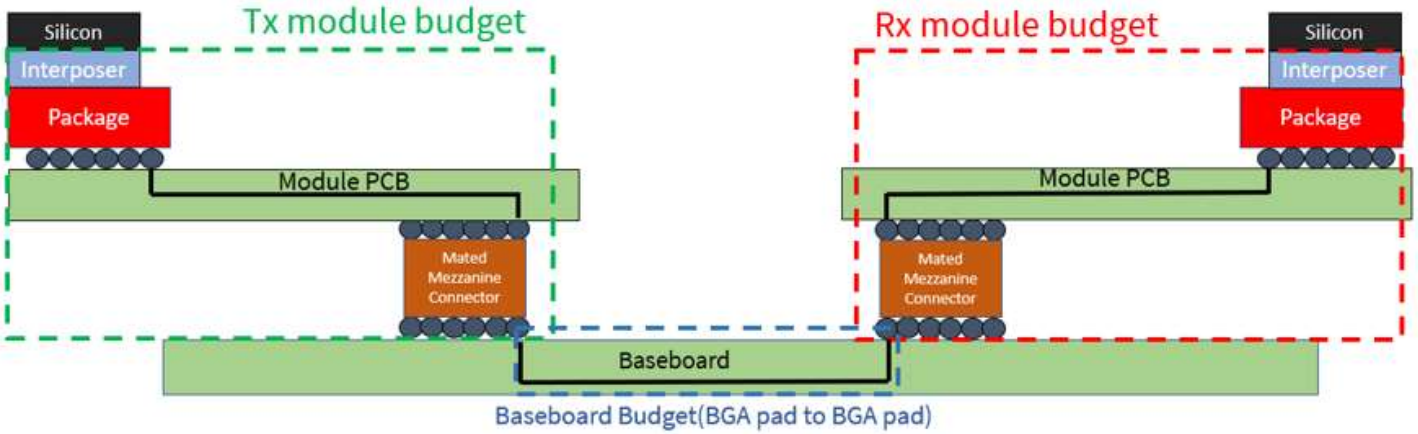
UBB I2C Topology



Power Delivery Block Diagram



Insertion Loss analysis



Total loss @ 14GHz	Hyper Ultra Low loss (dB)	Ultra Low loss (dB)	Low loss (dB)
OAM Module 1	8	8	8
Via 1	0.5	0.5	0.5
PCB TL estimation	**13**	**13**	**13**
Via 2	0.5	0.5	0.5
OAM Module 2	8	8	8

Acceptable length	Hyper Ultra Low loss (inch)	Ultra Low loss (inch)	Low loss (inch)
PCB TL	16.41	13.57	11.44

- Data is based on 14Ghz
- We only have 13 dB loss margin for routing on PCB.
- PCB loss/inch data is from measurement

PCB Stack-up

Layer	Nominal Board thickness 128.4 MIL	Glass type	Thickness (MIL)	Type	SE Zo 45 ohm (Tolerance +/-10%)	SE Zo 50ohm (Tolerance +/-10%)	Diff. Zo 85 ohm (Tolerance +/-10%)	Diff. Zo 90 ohm (Tolerance +/-10%)
	Solder Mask		0.5	Solder mask				
L1	0.5oz+plating		1.9	Signal/PWR	6.0	5.3	5.3 / 5.6	4.8 / 6.1
	PP		2.6					
L2	1oz		1.2	GND				
	Core (1/1)		4					
L3	1oz		1.2	Signal/PWR	5.8	5.0	5.7 / 5.6	5.0 / 6.0
	PP		5					
L4	1oz		1.2	GND				
	Core (1/1)		4					
L5	1oz		1.2	Signal/PWR	5.8	5.0	5.7 / 5.6	5.0 / 6.0
	PP		5					
L6	1oz		1.2	GND				
	Core (1/1)		4					
L7	1oz		1.2	Signal/PWR	5.8	5.0	5.7 / 5.6	5.0 / 6.0
	PP		5					
L8	1oz		1.2	GND				
	Core (1/1)		4					
L9	1oz		1.2	Signal/PWR	5.8	5.0	5.7 / 5.6	5.0 / 6.0
	PP		5					
L10	1oz		1.2	GND				
	Core (1/2)	Dual ply	4					
L11	2oz		2.4	PWR/GND				
	PP	Dual ply	12					
L12	2oz		2.4	PWR/GND				
	Core (1/2)	Dual ply	4					
L13	1oz		1.2	GND				
	PP		5					
L14	1oz		1.2	Signal/PWR	5.8	5.0	5.7 / 5.6	5.0 / 6.0
	Core (1/1)		4					
L15	1oz		1.2	GND				
	PP		5					
L16	1oz		1.2	Signal/PWR	5.8	5.0	5.7 / 5.6	5.0 / 6.0
	Core (1/1)		4					
L17	1oz		1.2	GND				
	PP		5					
L18	1oz		1.2	Signal/PWR	5.8	5.0	5.7 / 5.6	5.0 / 6.0
	Core (1/1)		4					
L19	1oz		1.2	GND				
	PP		5					
L20	1oz		1.2	Signal/PWR	5.8	5.0	5.7 / 5.6	5.0 / 6.0
	Core (1/1)		4					
L21	1oz		1.2	GND				
	PP		2.6					
L22	0.5oz+plating		1.9	Signal/PWR	6.0	5.3	5.3 / 5.6	4.8 / 6.1
	Solder Mask		0.5	Solder mask				
	Total board thicnkness : 128.4 mil							

Note :
1) The board thickness controlled within 128.4mil +/-10% (3.26 mm +/-10%)

- Reference UBBs: 22L
- PCB thickness: 128mil
- Recommended PCB loss criteria for up to 14.5'' routing on UBB:
  - -0.58 dB/inch @8Ghz
  - -0.88 dB/inch @14Ghz
  - -0.96 dB/inch @16Ghz

Call to Action

We invite you to join the OAM subgroup for further collaboration:

Register for the Mailing List:
https://ocp-all.groups.io/g/OCP-OAI

Wiki under OCP Server Project:
https://www.opencompute.org/wiki/Server/OAI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26–27, September, 2019