Advanced Packaging @ IME

Institute of Microelectronics,
A*STAR, Singapore

June 2019

CREATING GROWTH, ENHANCING LIVES

Institute of Microelectronics
A*STAR

Agency for Science Technology and Research -A*STAR

Mission: Advance science and develop innovative technology to further economic growth and improve lives

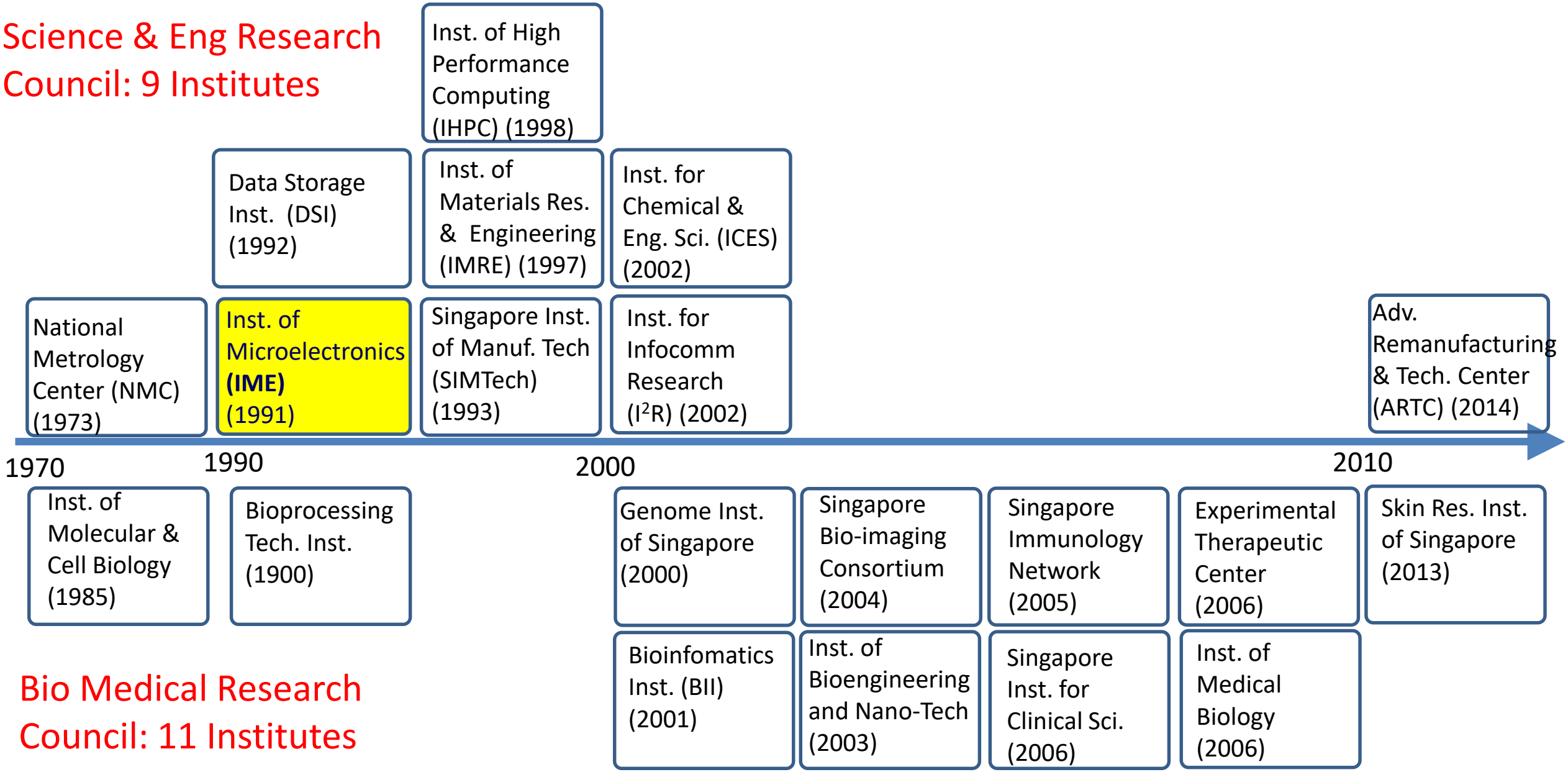
Science and Engineering Research Council (SERC)	Biomedical Research Council (BMRC)	A*ccelerate Technologies Pte Ltd (ETPL)	A*STAR Graduate Academy
9 Research Entities	11 Research Entities	Commercialization	Scholarships

>5,200 STAFF

4,100
Researchers, Engineers & Technical staff

38%
From 64 Countries

A*STAR Research Entities



Institute of Microelectronics

Key Research areas

- Advanced packaging
  - Heterogeneous integration
  - System in package
- Sensors and actuators
- IC Designing
- Memory enabled artificial intelligence
- Advance Optics
- Biomedical device and bio-packaging platforms

Infrastructure

- 12” TSV engineering line
- State-of-the equipment
- 3000m^2 clean rooms
- All metrology facilities

Strategic partnerships

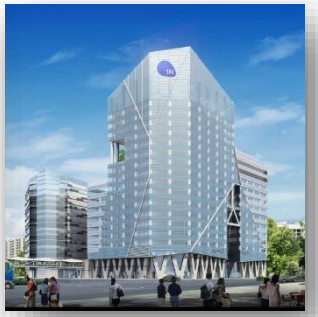
- Fabless, Foundries, IDM, OSAT
- Equipment, Materials makers
- Testing, EDA companies

Business friendly platform

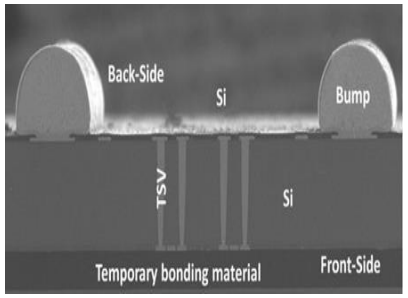
- Stringent controls and compliances
- Big pool of world class R&D talent
- Flexible collaboration models

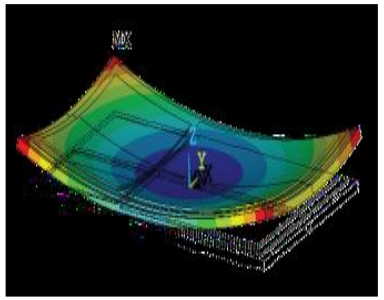
An ISO 9001 and ISO 13485 Certified Organization

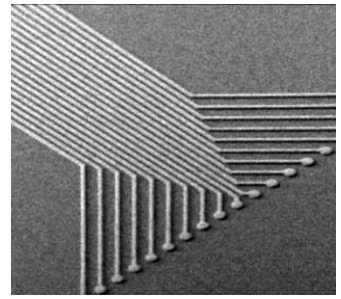
Science Park II

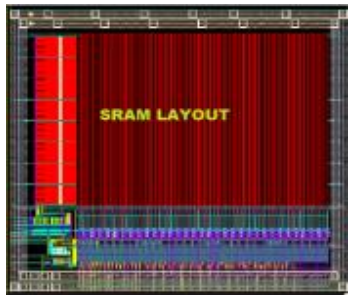


Fusionopolis







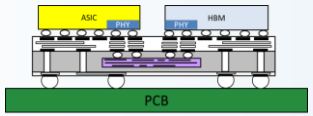


Advanced Package Development Approach

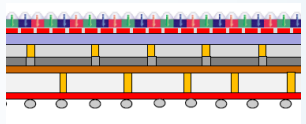
Application/System Requirements

- Data Centre
- IoT, 5G
- Biomedical Elec.
- Automotive Semi

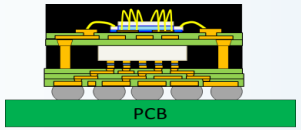
Package Architectures`



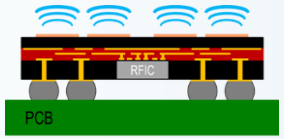
High Density 2.5D Pkg for AI SiP



3D Stack for CIS

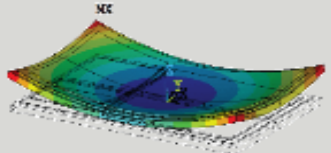


Ultrathin FO-PoP for Mobile/IoT

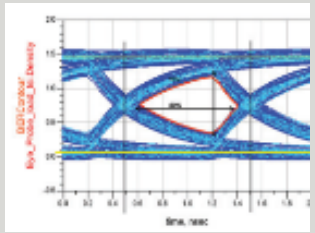


mmWave Antenna in FOWLP

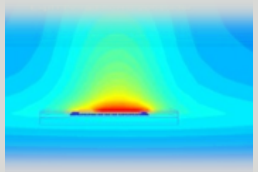
Models, PDK



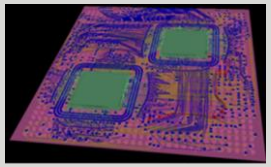
Mechanical



Electrical

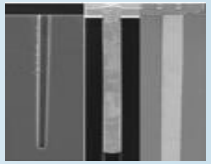


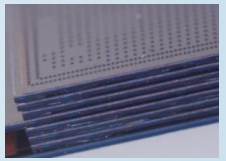
Thermal

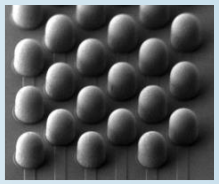


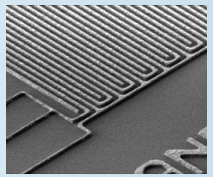
Package Design Implementation

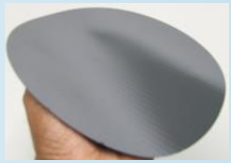
Process Modules



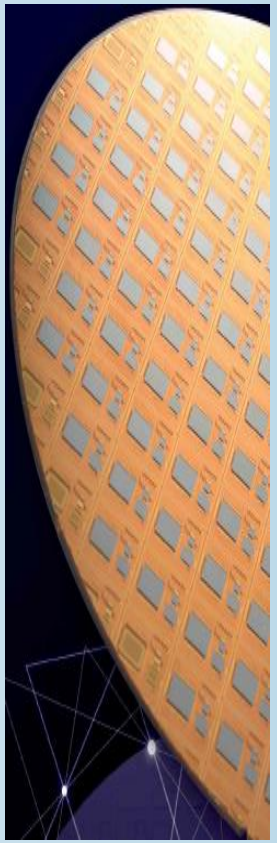




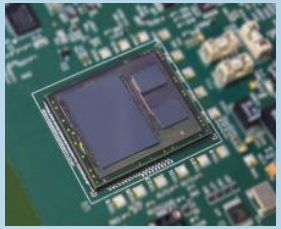




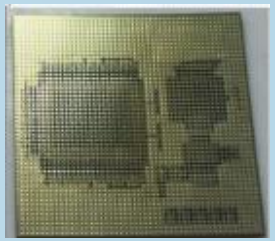
Process Integration, Materials Selection



Packaging Solutions



2.5D/3DIC



FOWLP

IME's Multi-Chip Wafer Level Package Development Line

Seed Layer deposition → Photoresist coating → Lithography → Developing → Plating → PR stripping → Seed etching → Photo-dielectric coating


PVD

PR track


Stepper


Developer track


Cu, Ni, Au, SnAg plating


Wet bench


Spray etcher

PR track

Lithography → Developing → Curing → Descum/etch → C2W bonding → Molding → Wafer Thinning → Carrier de-bonding


Stepper


Developer track


N2 furnace


O2 plasma


Flip-Chip bonder


Molding Tool


Backgrinder


Laser De-bonder

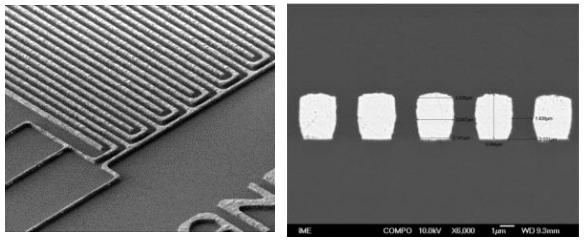
- Laser drilling
- Wafer compression molding
- Warpage adjuster
- High speed electroplating
- Descum tool

- Laser debonding
- Vertical Cu wire bonding
- Vacuum laminator
- Dry Film PR stripper
- Solder ball attachment tool

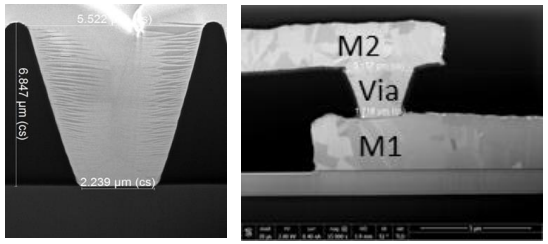
Development of baseline FOWLP Integration for next generation applications:

- *Package-architecture, integration flow, process, tools and materials.*
- *Mold 1st and RDL 1st technologies includes TMV & TMI technologies, Multi-layer fine RDL and dielectric materials, Compression mold and moldable underfill , Thin wafer handling.*
- *Estimate the manufacturability, variability ,reliability, cost an performance.*
- *Data Analytics to accelerate the cycle time for process development*

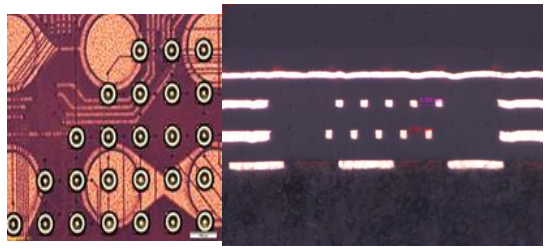
IME's Advanced Packaging Capabilities



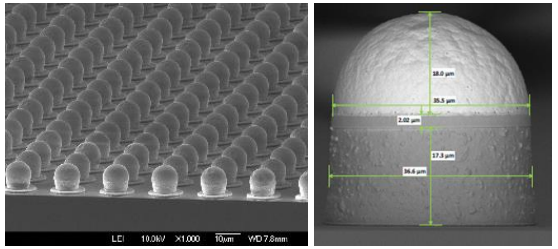
Fine Pitch RDL L/S of 2µm



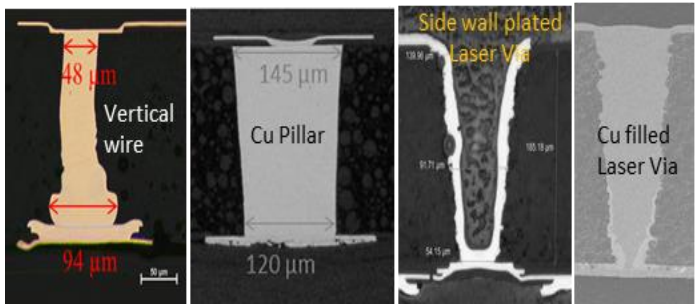
Micro-Via of up to 2µm in polymer dielectric for fine pitch RDL



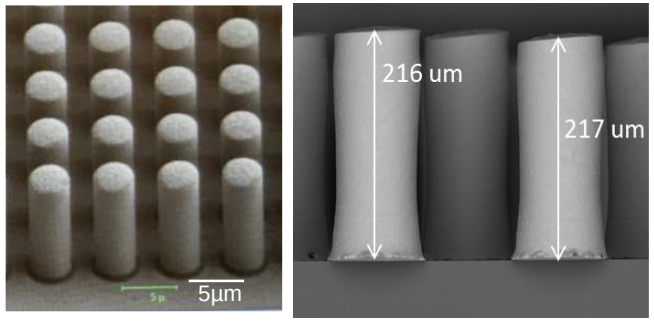
Multi-Layer RDL up to 4 layers



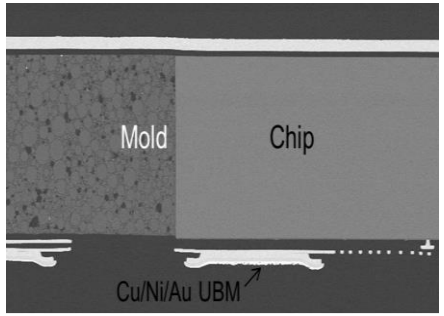
Fine pitch Cu Pillar bumping up to 20µm pitch



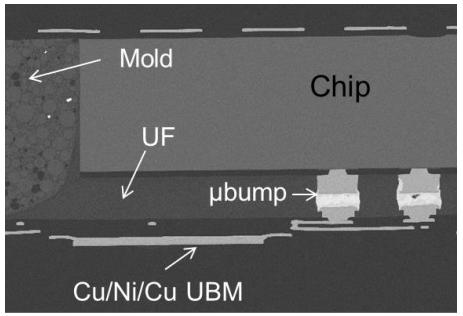
Through Mold Interconnections for FO PoP



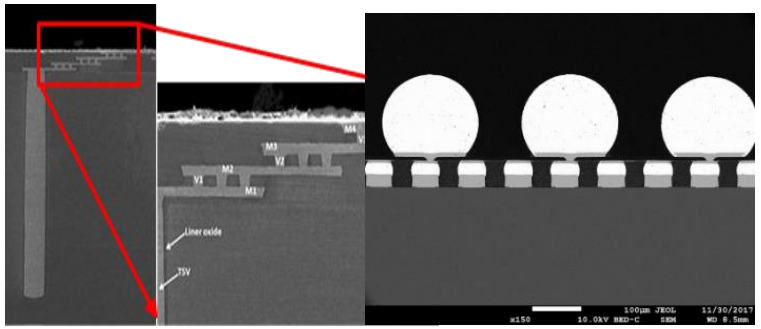
Cu Pillar bumping: Fine pitch up to 6µm pitch & tall pillar of >200µm height



Mold 1st (Die 1st) FOWLP with L/S of 5µm

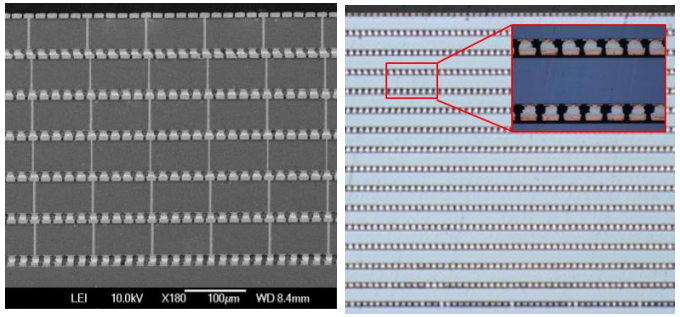


RDL 1st (Die last) FOWLP with L/S of 2µm

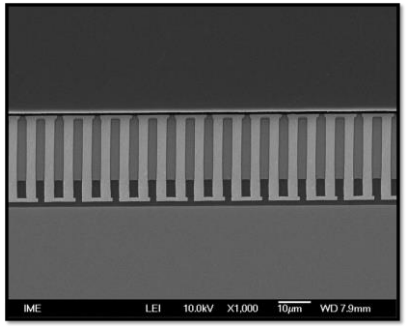


TSV with BEOL RDL for TSV interposer

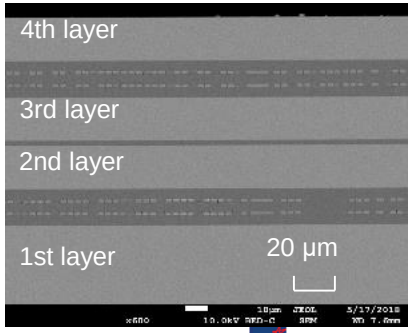
TFI with BEOL-RDL L/S of 0.4µm



3D Chip Stacking (up to 15 dies) using 20µm pitch interconnections



C2W 6µm pitch Cu-Cu bonding



4-stack wafer bonding

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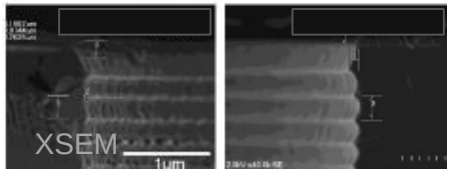
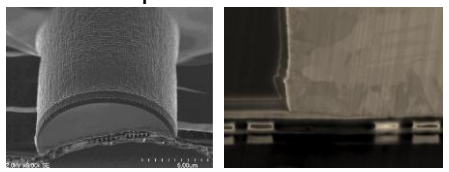
2.5D/3DIC Platform

Building Blocks

TSV Si and liner Etch

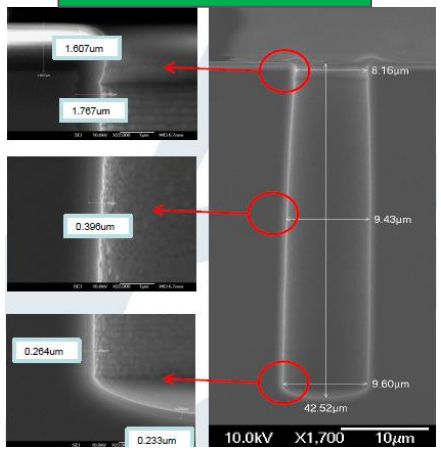


- Scallop size ~20nm



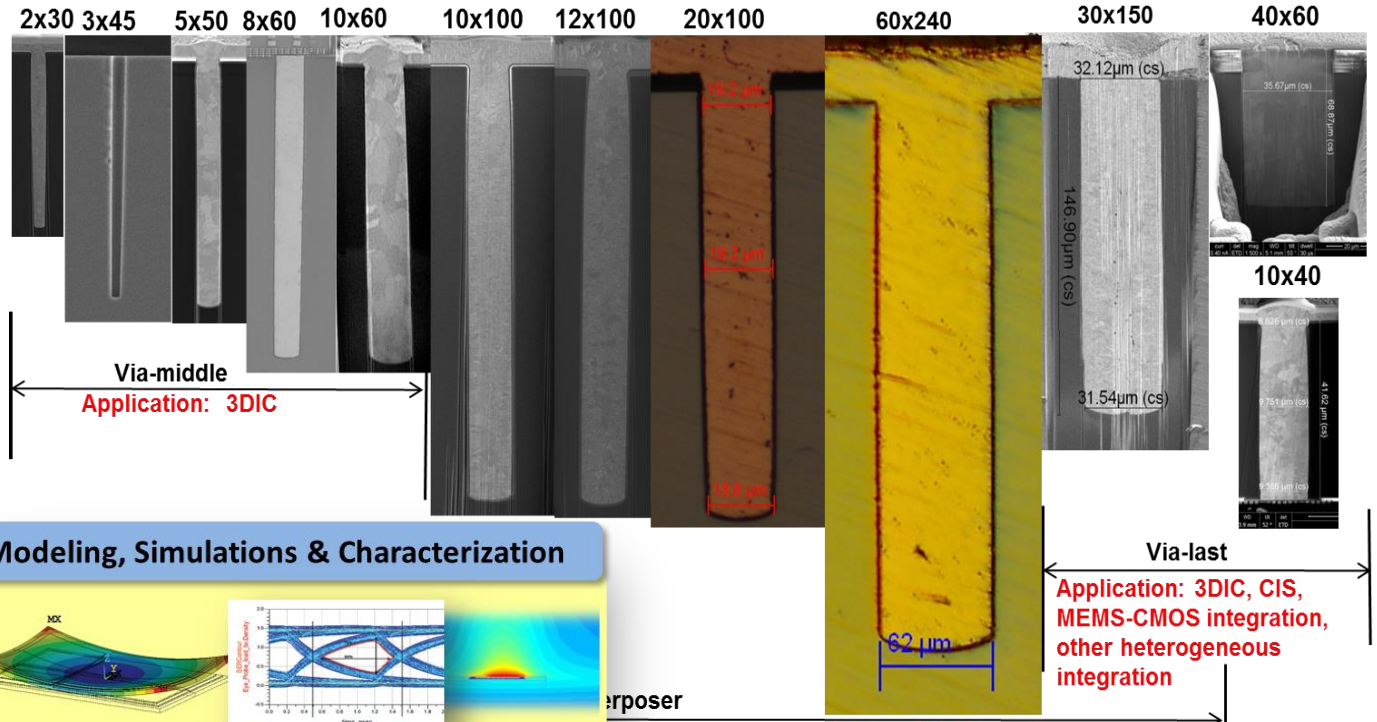
- Minimal notching (<0.5um)

Liner Oxide CVD

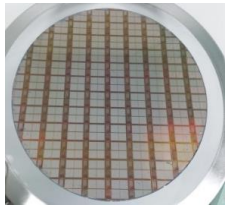


- Liner Oxide CVD Coverage ~15%

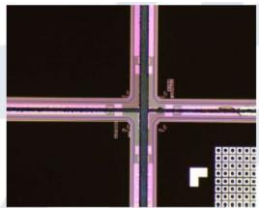
TSV (Via-First/Middle/Last)



Debond / Dicing

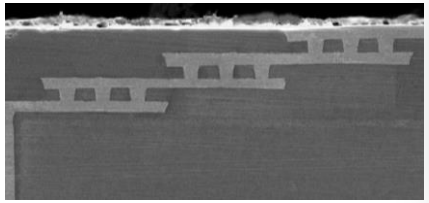


40um thickness



Dicing of 40um thin dies.

Multi-Layer RDL

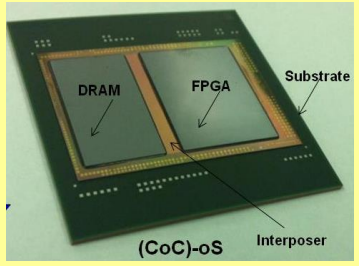


Modeling, Simulations & Characterization

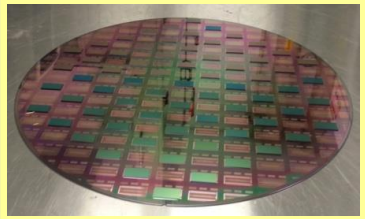
Package Warpage | Electrical | Thermal

Applications

2.5D Heterogeneous Integration (TSI)

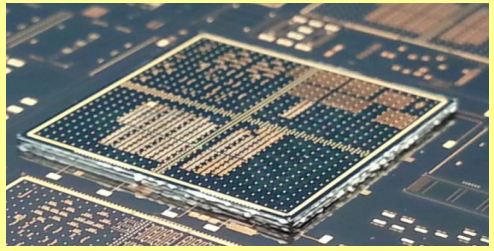


3D-CIS (CoW)

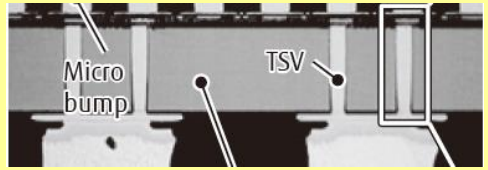


DSP/CIS on glass

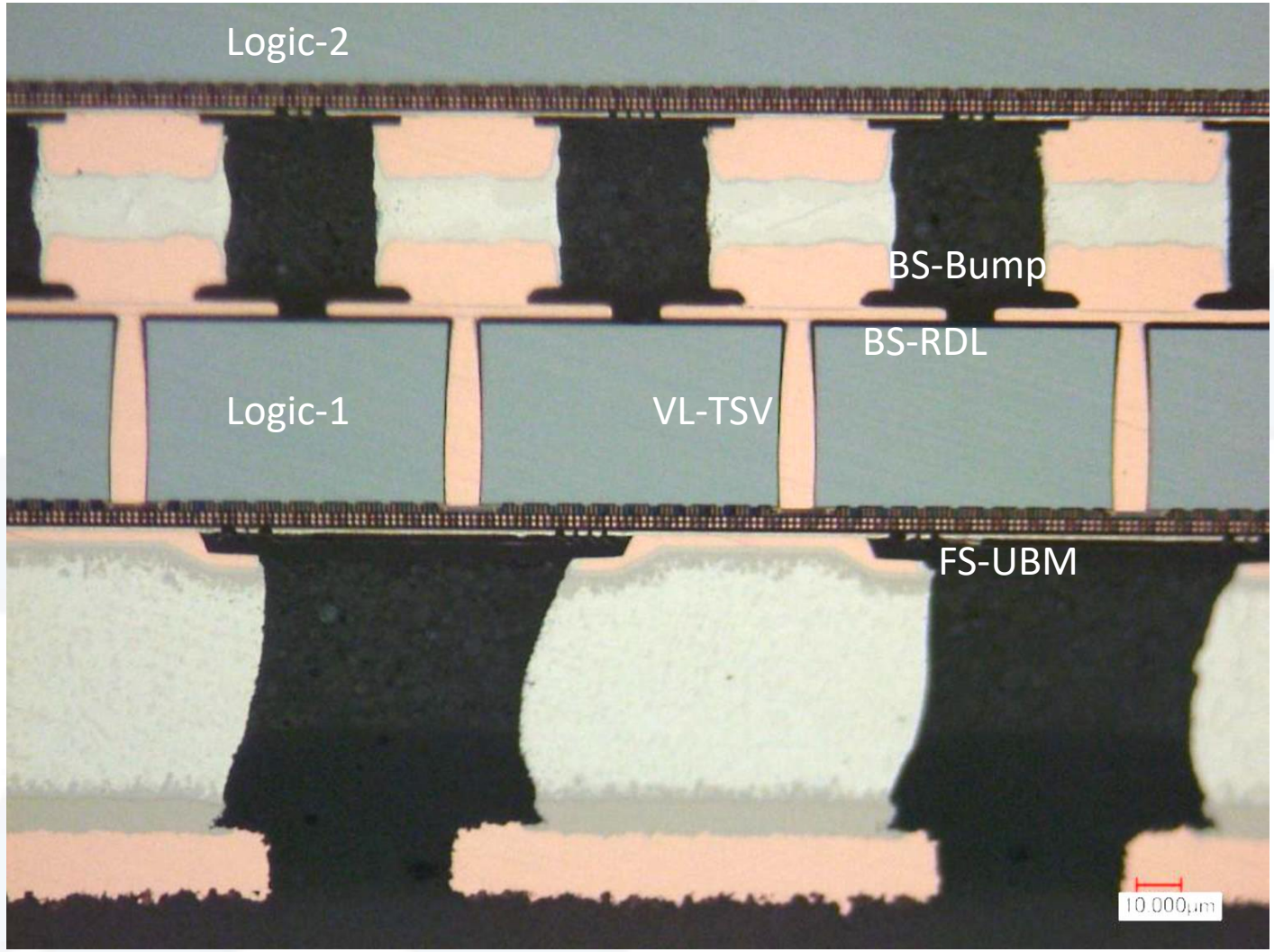
3D Memory



HPC (VL-TSV)



Via-Last from Backside Demonstration for HPC Application

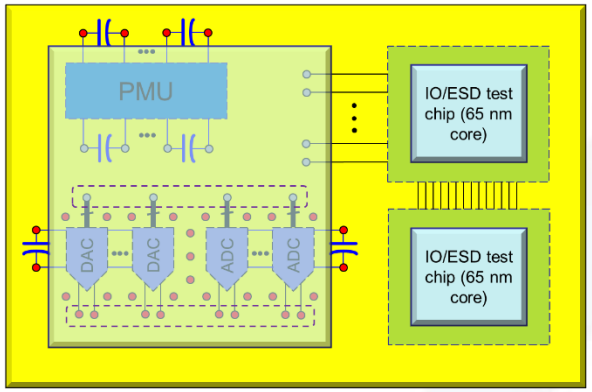


- IME demonstrated FS-UBM, VL-TSV, BS-RDL and BS SnAg/Cu-pillar capabilities on CMOS Logic device wafers.
- 10 x 40um VL-TSV was successfully demonstrated.

- ✓ Good overlay control (back-to-front mis-alignment <1um)
- ✓ Good TSV etch profile (no notching)
- ✓ Good liner coverage (sidewall oxide thickness >200nm)
- ✓ Good connectivity with M1 (no under/over etching)
- ✓ Good TSV Cu filling (no void)
- ✓ Good bump height uniformity control (non-uniformity<5%)

Heterogeneous Integration on Active Silicon Interposer

Active Interposer Design



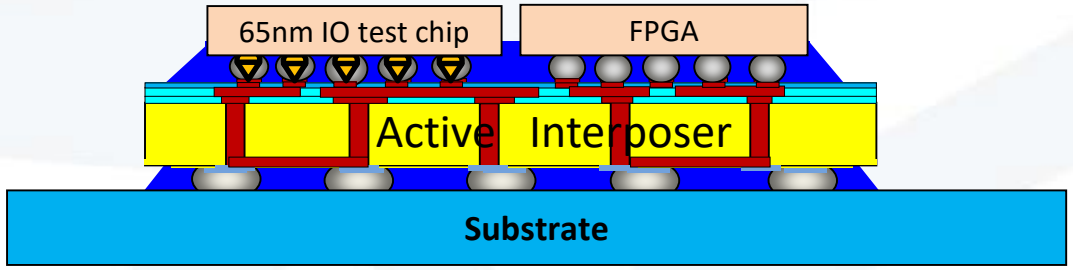
Interposer functions

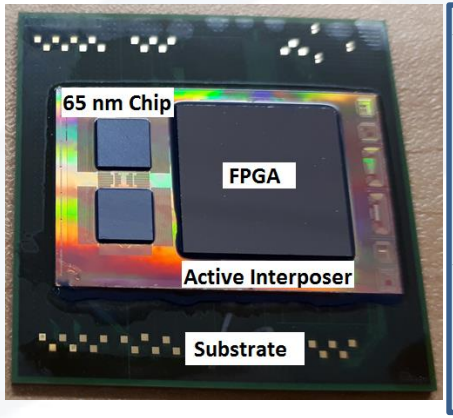
- Power management Unit
- ADC-DAC
- I/O circuits including ESD clamps, De-Caps

Highlights

- Demonstrated Active Si Interposer platform (via last fabrication, assembly & packaging
- Active Interposer function to validate
  1. IO ESD partitioning
  2. System scaling benefits with ADC-DAC and PMU in ATSI
  3. System cost reduction

Active Interposer Package Schematic

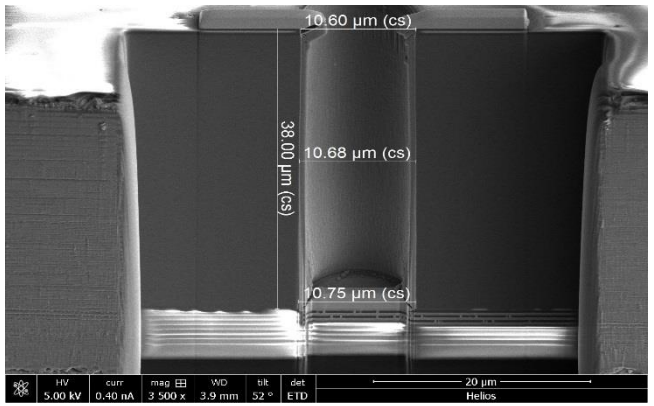


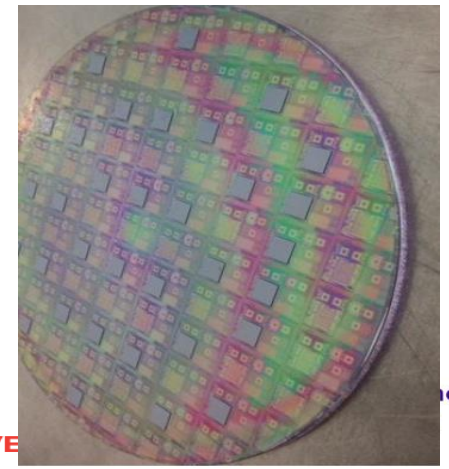


- Heterogeneous Integration of 28nm node FPGA, 65 nm I/O chip and 130 nm ATSI demonstrated
- Assembly capability involving 40µm thickness and 25mmx35mm Interposer.

Via Last TSV Fabrication and Assembly

- 40 µm ATSI functional wafers (AR: 1:4) fabricated via-last from Backside.
- Chip to Wafer bonding of FPGA and I/O Chip.



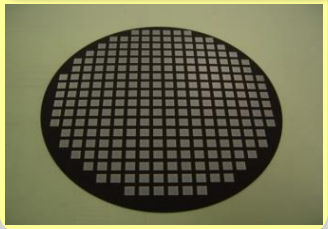


Fan-Out Wafer Level Packaging (FOWLP) Platform

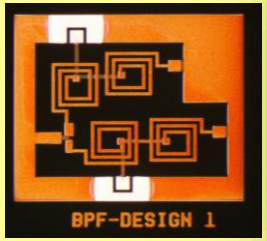
Building Blocks

Reconstruction

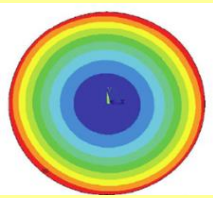
Molding



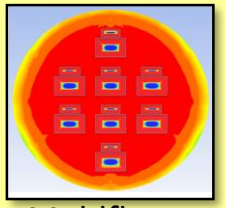
Passives/Antenna



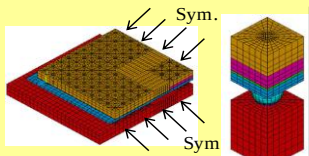
Modeling and Simulations, and Characterization



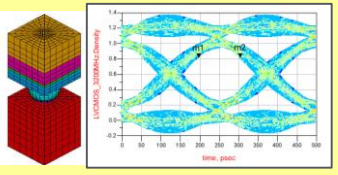
Warpage



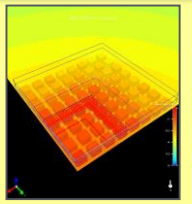
Moldflow



Joint fatigue life

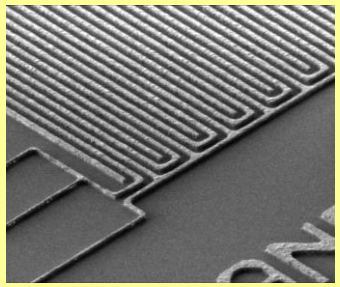


Electrical

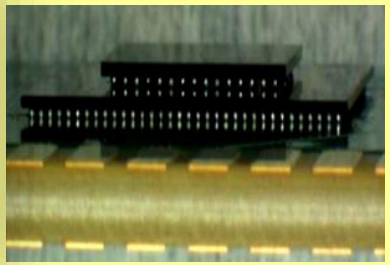


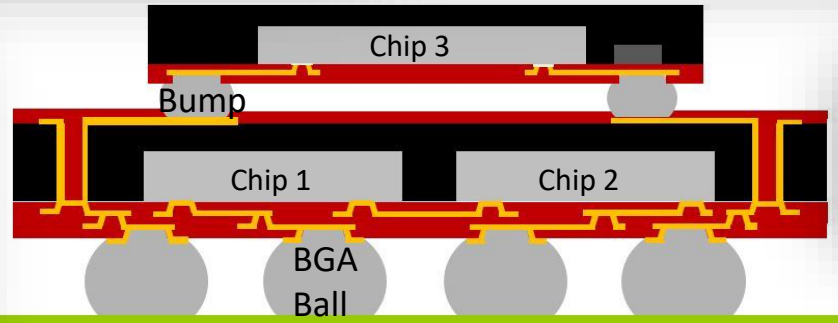
Thermal

Fine-pitch RDL

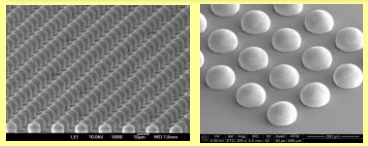


FO PoP

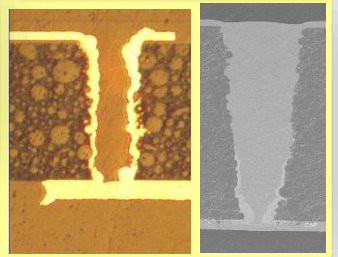




Solder bump



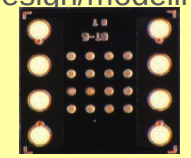
TMV



Applications

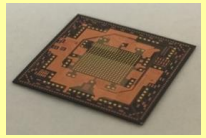
MEMS WLCSP

- MEMS integrated with ASIC
- Interconnect design/modeling



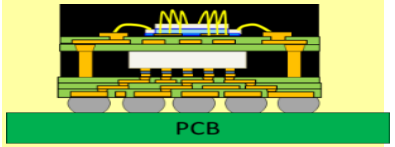
HD-FanOut for Multi-Chip SiP `

- Embedded EFI <2um LS
- Hybrid dielectric for RDL



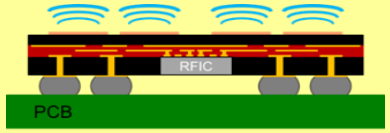
Ultrathin Package A/P

- 2nd level wire bond
- Integrated PoP
- Hemis Cu pillar



5G mmWave AiP

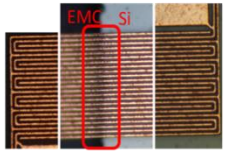
- Low loss materials
- Integrated cooling solution



IVR for

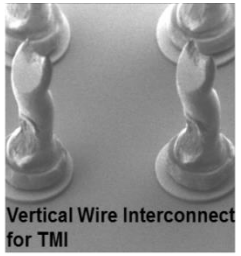
- Multi-thick Cu RDL (7um-20um) solenoid inductor

High Density RDL 1st FOWLP for Multi-Chip Packaging



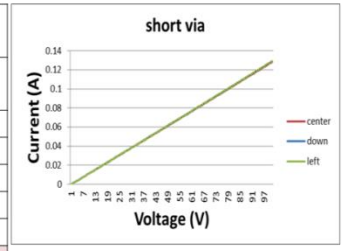
2um Cu RDL trace along Si chip & mold interface without distortion


Fine Pitch RDL and small via opening (3um) in PI


Vertical Wire Interconnect for TMI

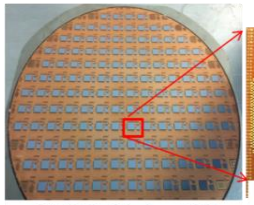

Thick PR patterning for Cu pillar TMI

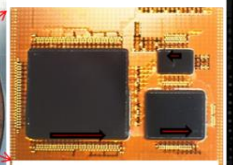
	Meander	Leakage Current (A)
Wafer location	2 um	@0-5 V
center	2.01	3.56E-13
left	2.01	3.71E-13
right	2.02	3.78E-13
top	2.15	3.06E-13
bottom	2.20	3.34E-13
Average	2.07	3.49E-13

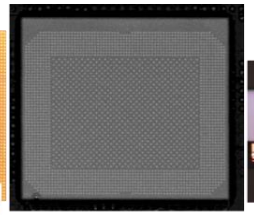


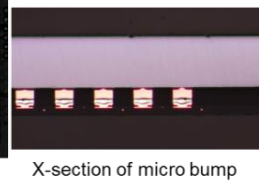
Meander structure: Average leakage current: ~3.5x10-13 Amp @ 5V

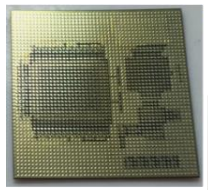
Fine Pitch RDL (L/S:2um/2um) & TMI for PoP

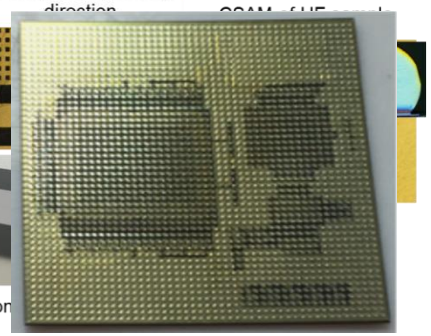

ATV 2 CoW after CUF


"I" shaped dispensing



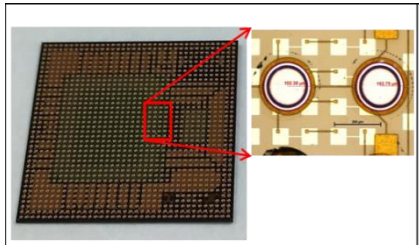

X-section of micro bump

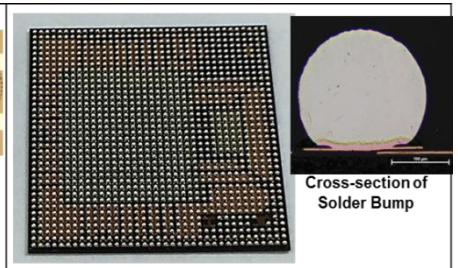



ATV 2 Package after singulation


ATV2 on PCB

Multi-chip FOWLP (20 x 20 mm²) with ~2400 I/Os


ATV1 Package before Solder Ball attachment

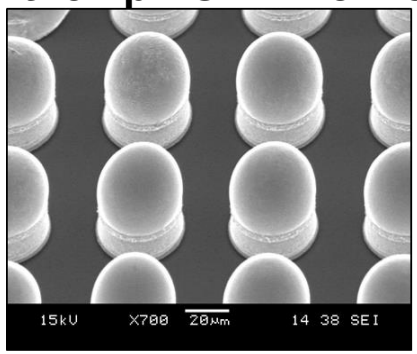


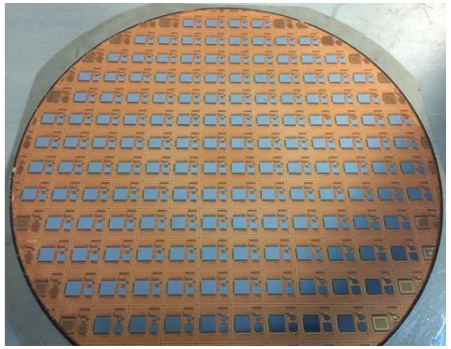
ATV1 Package after Solder Ball attachment

ATV1 assembly on PCB

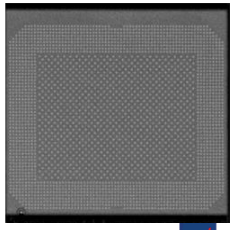

Cross-section of ATV1 on PCB

Multi-chip FOWLP of 15 x 15 mm² with 1367 I/Os





	Test condition	Sample size	Results
15 x 15 mm² size FOWLP	MSL 1	10	Passed (10/10)
	MSL 3	10	Passed (10/10)
	TC	10	Passed 500 cyc (10/10)
	TCoB	10	Passed first TC 100 (10/10).

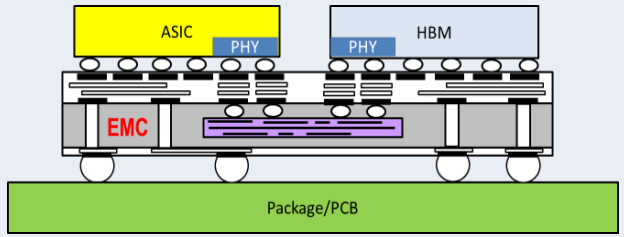


Micro bumping, C2W and Reliability Data

Institute of Microelectronics

Multi-Chip High Density Fan-Out Packaging Applications

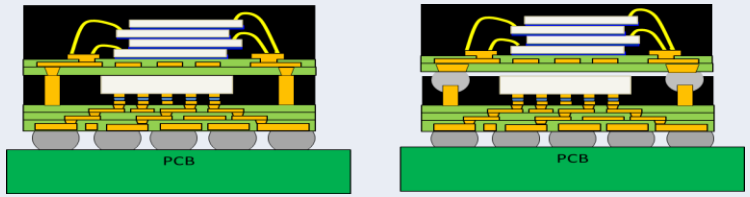
High Density FOWLP For GPU + HBM



Specifications

- Package I/O count: ~2000
- Min. EFI L/S 0.4um/0.4um, 3-4 layers
- Package size: >30mm x 25mm
- Chip size: 21mm x 17mm, 5mm x 7mm

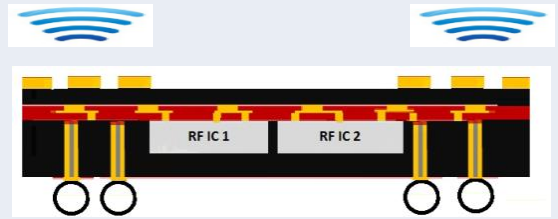
Ultra-Thin FO-PoP for Mobile



Specifications

- Package I/O count: ~1200
- RDL L/S 2um/2um, 2 layer
- Package size: ~15mm x 15mm
- AP size: ~11mm x 11mm
- TMV scaling <300um; Total PoP ~ 0.8mm
- Integrated Thermal Solution

mmWave Antenna in Package for 5G

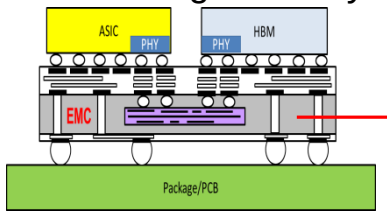


Specifications*

- Package I/O count: 100-200
- RDL L/S: 5um/5um, 2-3 layers
- Package size ~ 10mm x 10mm
- No of chips: up to 4
- Array antenna

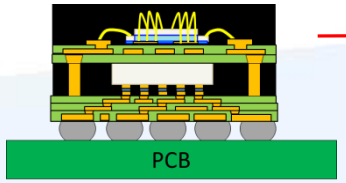
Multi-Chip 2.5D/FOWLP PDK and EDA Reference Flow

2.5D High Density



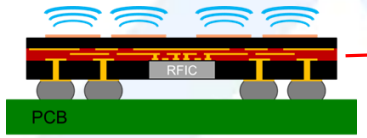
- *Pin optimization between HBM, ASIC & Interposer*
- *High density routing between TX/RX IO's*
- *Multi step parasitic extraction, RDL & Interposer parasitic needs to back annotate for accurate SI analysis*

Ultrathin FO-PoP

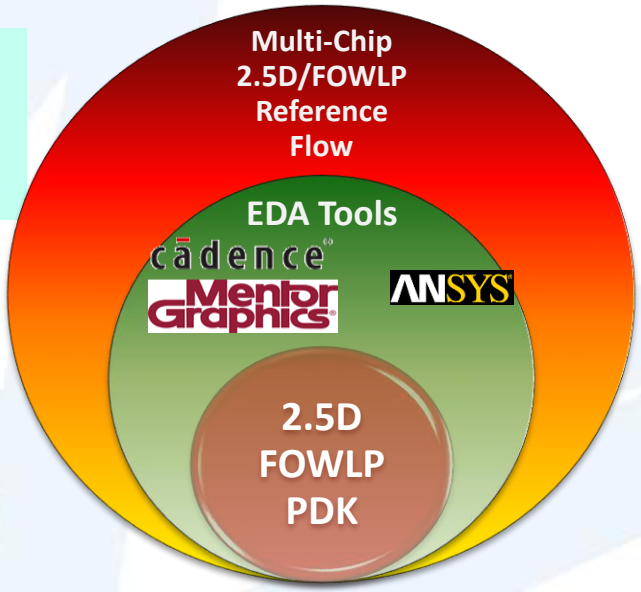


- *3D placement, visualization and checks*
- *Bond wire inductance*

Antenna in FOWLP

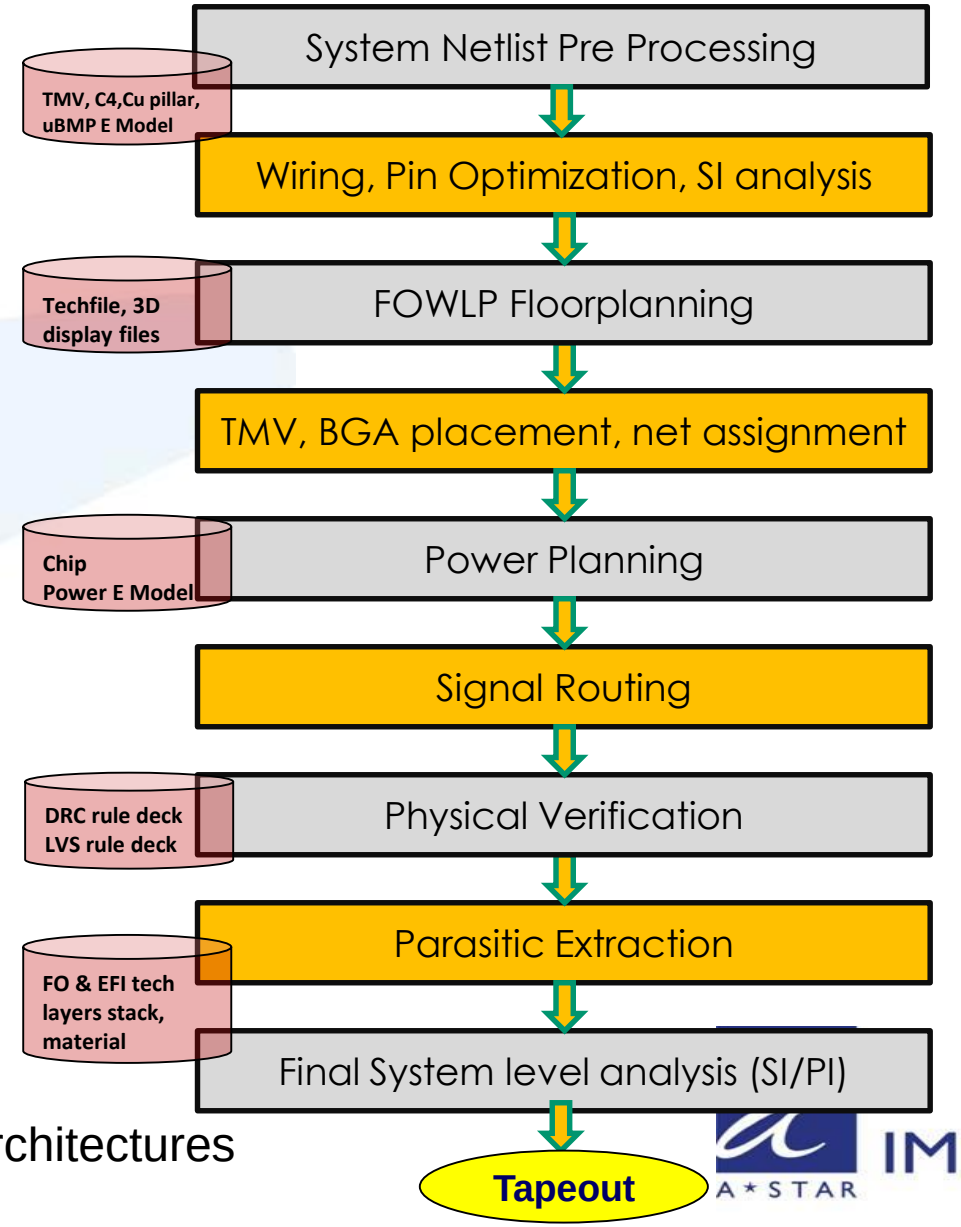


- *Model import/export for 3D EM simulations*
- *Transmission line model for interconnects and antenna feeding networks*
- *Parasitic and coupling effects between antenna elements and routings*



2.5D, FOWLP PDK

Electrical models,
Process stack & material properties,
Automation scripts,
Parasitic extraction decks,
Physical verification decks,
Placement / Routing constraints from mechanical & thermal analysis



Reference Flow and Design Rules for Variety of Advanced Package Architectures

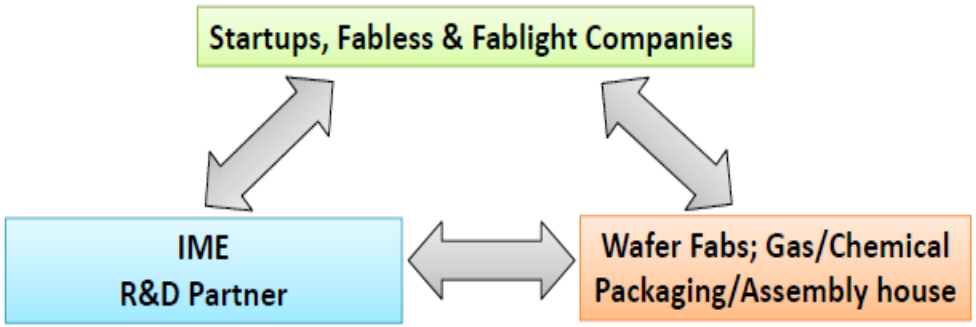
IME A*STAR

IME's Advanced Packaging Business Model

- **IME offers Capabilities and Technology Platforms in 2.5D/3DIC, WLP (300mm and 200mm)**
  - Developing transferable, production-worthy 2.5D, 3DIC, WLP solutions utilizing heterogeneous integration.
  - Demonstrating prototypes for integration into system-boards and products.

- **Critical Mass for Impactful Cost-effective R&D Partnership**
  - Small scale pilot runs to enable customers to bring products to markets quickly

- **Support Multiple-Party Collaborative Model**
  - Bridge gaps between Chip Company, Foundry, Substrate-manufacturer, SAT, Equipment manufacturer to allow for technology to ramp into production.



A*STAR IME

THANK YOU