Chiplet Design Experience Panel

ODSA June 10, 2019

Goal: explore the system performance, power and cost requirements that drive a product to a chiplet-based design.

Moderator: Ramune Nagisetty, Intel

- Sagheer Ahmad , Xilinx
- Sanjeev Joshi, Cisco
- Dave Kehlet, Intel
- Gabriel Loh, AMD
- Carlos Macian, eSilicon

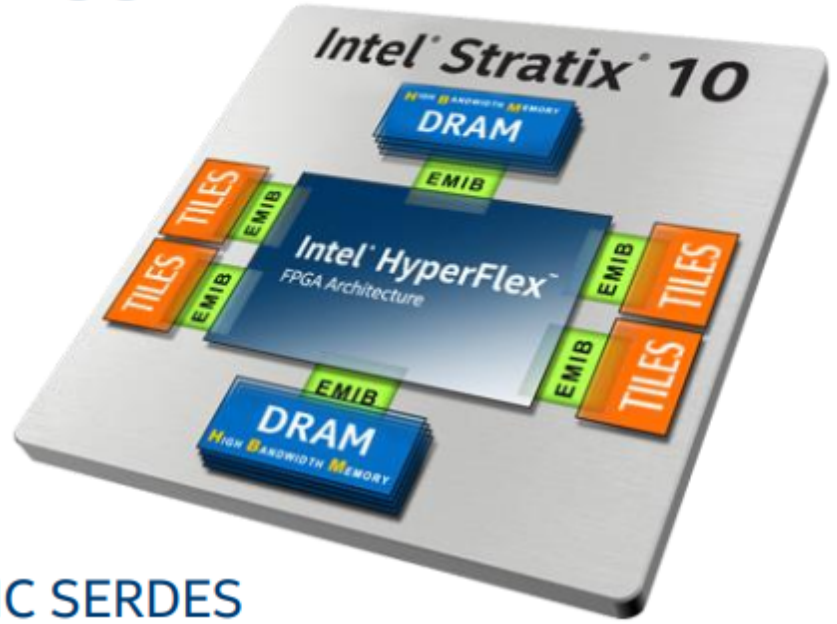
Sagheer Ahmad, Sr Director, Architecture

- Responsible for Silicon Architecture incl. NoC, DDR/HBM Memory Subsystem, and Chip-to-Chip Interconnect.
- Previously worked on SoC, GPU, and CPU architectures & designs at Nvidia, AMD, and Sun Microsystems etc.
- At Xilinx, we have done 2.5D multi-chip integration over interposer
  - Four 28nm FPGA Dice integration based on SSIT (2011)
  - Up to three 28nm FPGA and two SerDes Dice (2012)
  - Up to three 16nm FPGA and two HBM2 Dice (2017)
- Looking at both Parallel (HBI) & Serial (XSR) Chip to Chip interconnects

Sanjeev Joshi, ASIC Director, Cisco Datacenter Group

- Currently driving development of third generation multi-die switching ASICs
- Previously managed development of Algorithmic Memories, Switching ASICs and SoC development at Memoir, Cisco and PMC-Sierra
- Main drivers for chiplet based solutions at Cisco
  - Die area – Feeds/speeds/feature requirements won't fit on a single reticle
  - IO flexibility – 56G/112G serdes, IPO
  - Cost
  - Product Mix

OCP/ODSA Chiplet Design Experience: Dave Kehlet



Stratix 10 / Agilex Tiles

- L-tile: 17G, 24 transceivers, PCI Express Gen3 Hard IP
  - Disaggregation to reuse 20nm TSMC SERDES design
- H-tile: 28G, 50/100G Ethernet MAC, PCI Express with SRIOV
  - Met IP request from a major customer
- E-tile: 56G, 4x100G Ethernet, KRFEC and KPFEC
  - Under-the-radar project (initially) to build with 16nm TSMC SERDES
  - Forked a parallel development team for 2 tiles at a time

All in production, >>100,000 shipped

Divide and conquer (FPGA main die department and Tile department) worked really well

- 4 year FPGA design vs. 2 year E-tile design, went from trailing to FPGA SERDES leadership!

Managed to solve immediate SERDES problem, solution works for 56G, 112G, PCIe Gen4, Gen5

- The forward-looking flexibility was much more valuable that we imagined!

DARPA CHIPS: 2.5D PHY, Protocols, Hardware Open Source, Applications

AMD

Gabriel Loh

Senior Fellow

AMD Research

Current:

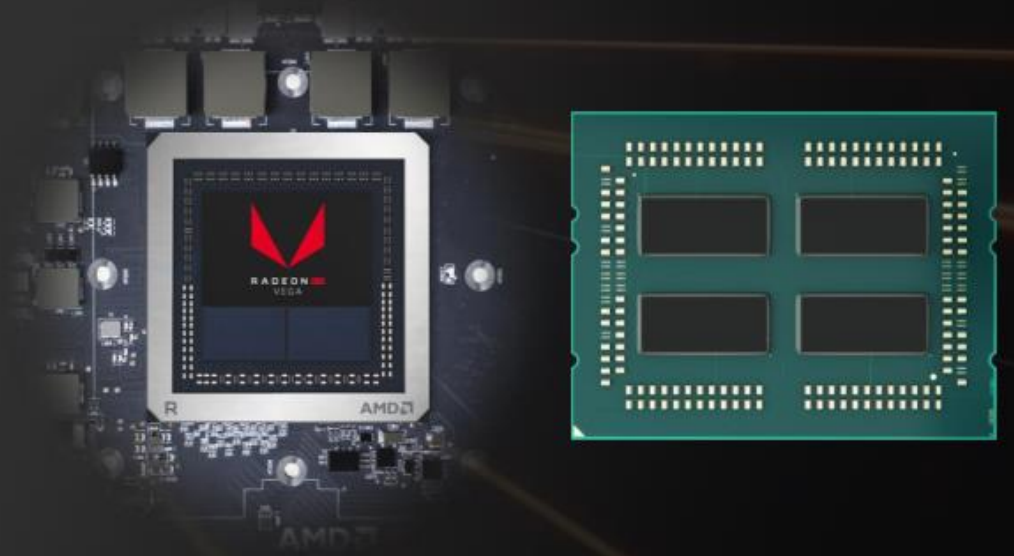
Nine years at AMD Research
Principal Investigator, US DOE PathForward Program
Focus areas: Computer architecture, advanced packaging (2.5D, 3D, chiplets, HBM), interconnects/ NoC, memory systems, HPC

Past:

PhD, Yale University
Visiting Researcher, Microsoft Researcher
Associate Professor, Georgia Institute of Technology
Senior Researcher, Intel

AMD Stacking and Chiplets

- First high-volume GPU with interposer and HBM in 2015
- HBM2-enabled GPUs and interposers
- Quad-chiplet EPYC™ Server CPUs
- Multi-chiplet 2nd-generation EPYC™ Server CPU with different die
- Chiplet-based AMD Ryzen™ processors announced



Carlos Macian, eSilicon and Chiplets

Open-market chiplets or joint venture chiplets?

- Advanced ASIC and IP provider in datacenter networking, HPC, AI and 5G
- Advanced SiP solutions in the 2.5D, 3D and silicon photonics space
- Most paths lead to Rome... For different reasons and in different ways
- Need to go from feasible to mature