Good Morning!
Good Afternoon!
Good Evening!
1st ODSA Chiplet Business Workshop

Ravi Agarwal
Open Domain-Specific Architecture, Chiplet Business Workstream lead
Technical Sourcing, Facebook
THANK YOU

Workshop Sponsors:

FACEBOOK

ASE GROUP
<table>
<thead>
<tr>
<th>Start Time</th>
<th>End Time</th>
<th>Topic</th>
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<tbody>
<tr>
<td>07:30</td>
<td>08:00</td>
<td><strong>Opening Coffee Sponsorship #1</strong></td>
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<tr>
<td>08:00</td>
<td>08:04</td>
<td>Welcome</td>
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<td>08:04</td>
<td>08:08</td>
<td>ODSA how/what/where/why</td>
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<td>08:08</td>
<td>08:16</td>
<td>Need for Establishing a Chiplet Ecosystem</td>
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<tr>
<td>08:16</td>
<td>08:24</td>
<td>Chiplet business challenges for AI accelerator</td>
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<tr>
<td>08:24</td>
<td>08:32</td>
<td>HIR status update (Chiplet Business Challenges)</td>
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<tr>
<td>08:32</td>
<td>08:40</td>
<td>Business Challenges and Opportunities of Chiplets in Heterogeneous Acceleration</td>
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<td>09:23</td>
<td><strong>Chiplet Value Chain Discussion Design--&gt;Build--&gt;Deliver</strong></td>
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<td>08:40</td>
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<td>Design</td>
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<td>Chiplets in Space</td>
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<td>08:48</td>
<td><strong>Moderator: Allan</strong></td>
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<td>Synopsys: Manuel</td>
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<td>Cadence: Rishi</td>
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<td>Alphawave: Tony</td>
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<td>09:23</td>
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<td>Coffee Break Sponsorship #2</td>
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<td>09:38</td>
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<td><strong>Build</strong></td>
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<td>09:38</td>
<td>09:45</td>
<td>Chiplet Economic constraints</td>
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<td>09:45</td>
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<td><strong>Moderator: Andreas</strong></td>
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<td>Samsung: Max</td>
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<td><strong>Deliver</strong></td>
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<td>11:03</td>
<td>Business consideration for Chiplet based compute products</td>
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<td>11:03</td>
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<td><strong>Moderator: David</strong></td>
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<td>Microchip: Anu</td>
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<td>Marvell: Ramin</td>
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<td>Google: Ben</td>
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<td>Alibaba: Weifeng</td>
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<td>FB: Nicolaas</td>
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<td></td>
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<td>Microsoft: Ishwar</td>
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</tbody>
</table>
ODSA Business Workshop.

Bapi Vinnakota
Open Domain-Specific Architecture, Sub-project lead
System Architect, Broadcom
Welcome!

• Our biggest workshop ever!
  − HUUUUGE effort from DJ, Ravi, Rishi, many others

• After the workshop
  − Participate actively, join a work stream!

• ODSA meets Fridays at 8 AM Pacific, work streams meet weekly
  − https://www.opencompute.org/wiki/Server/ODSA

• Next few Fridays
  − BoW Test Chip Proposals
  − Chiplet Market Survey
  − Chiplets from LETI
  − SW PoC workshop
  − Memory
ODSA Charter

Open D2D Interface
Reduce barrier to interoperation

Reference Designs
Starting point for new designs

Reference Workflows
Reusable, open practices

ODSA Activities

Chiplet Marketplace
Integrate best-in-class chiplets from multiple vendors through open interfaces

OCP modular form factors

ODSA Activities

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OCP modular form factors
# ODSA Workstreams

Each group meets weekly, details at [https://www.opencompute.org/wiki/Server/ODSA](https://www.opencompute.org/wiki/Server/ODSA)

<table>
<thead>
<tr>
<th>Workstream</th>
<th>Leader</th>
<th>Participants</th>
<th>Objective</th>
</tr>
</thead>
<tbody>
<tr>
<td>PHY Layer</td>
<td>Robert Wang</td>
<td>IBM, Xilinx, SYNOPSYS, Marvell</td>
<td>PCIe PIPE adapter</td>
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<tr>
<td>Bunch of Wires</td>
<td>Mark Kuemerle</td>
<td>Xilinx, SYNOPSYS, Keysight, Google, IBM, SiFive</td>
<td>Low cost D2D PHY</td>
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<tr>
<td>CDX</td>
<td>Jawad Nasrullah</td>
<td>zGlue, ANSYS, Achronix, Lattice, NXP</td>
<td>Chiplet design exchange</td>
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<td>Biz 9 AM Fridays</td>
<td>Ravi Agarwal</td>
<td>Facebook, cadence, SYNOPSYS, Microsoft, Achronix, Achronix</td>
<td>Chiplet workflow</td>
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<tr>
<td>PoC hardware</td>
<td>JP Balachandran</td>
<td>Facebook, Achronix, Lattice, NXP</td>
<td>PoC board design</td>
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<td>PoC software</td>
<td>Kevin Drucker</td>
<td>Facebook, Samtec, MACOM, Netronome, zGlue, Tamind</td>
<td>Application/Infra software</td>
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<td>Link layer</td>
<td>Open</td>
<td>Xilinx, NXP, Intel, VENTANA MICRO, Microsoft Azure</td>
<td>ODSA Stack</td>
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<td>OpenHBI</td>
<td>Kenneth Ma</td>
<td>Xilinx, IBM, Keysight, Synopsys, Samsung, Marvell</td>
<td>High perf D2D PHY</td>
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<tr>
<td>End user</td>
<td>Dharmesh Jani</td>
<td>Google, Aliabha.com, cadence, Microsoft Azure</td>
<td></td>
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</tbody>
</table>

BoW Test Chip

Attendance and/or participation do not imply corporate endorsement

Sub-project lead: Bapi Vinnakota
Please Help, Join Us!

• Join a work stream, each meets weekly
• Help with the PoC, software, use case dev,
• Review, help complete documents in flight
• Need packaging and test definition and work streams
• Make chiplets with, IP for, the open ODSA stack
• https://www.opencompute.org/wiki/Server/ODSA
Reference
ODSA Progress

1H, 2019

2H, 2019

1H, 2020

2H, 2020

details at https://www.opencompute.org/wiki/Server/ODSA
For More Information

**ODSA Wiki**: All workshops, minutes of weekly calls, workstreams (open access)

**Specification proposals**:  
- Bunch of Wires [GitHub repo](https://github.com/) (open access)  
- PIPE adapter (PCIe over D2D), DiPort (AXI over D2D) (open, but need to request access)  
- [ODSA PoC Demo](https://odsa.github.io/) (open access), [ODSA PoC Implementation Specification](https://odsa.github.io/) (open, but need to request access)

**In-flight**  
- LPIF, LPIF’ proposal  
- ODSA PoC SW  
- Open HBI specification (needs CLA)

**Technical Papers/Talks**  
- [ODSA white paper](https://odsa.github.io/), ODSA Wiki  
- D. Jani, “Musings on Domain Specific Accelerators, Open Compute Project and Cambrian Explosion”, LinkedIn  
- ODSA track at the OCP Global Tech Summit.
Need for Establishing a Chiplet Ecosystem

Javier DeLaCruz, ARM
What is a Chiplet?

A Chiplet is defined by having an **interface** optimized for die-to-die connectivity within a package.

A Chiplet lacks the drive strength to be packaged independently.

Ideally this creates a system that is more efficient than using conventional die or packaged parts.

Mara, ODSA idealized chiplet concept
Drivers and Barriers of Chiplets

• Three main drivers exist for chiplets
  - Reticle Limits, needing more silicon area
  - Cost Savings, partition die to improve overall yield
  - **Heterogeneity**

• Barriers for Heterogeneity
  - Tapeout costs for each chiplet
  - Starting from scratch may not be practical
  - Common interface standards (phy, control, etc.)
  - Worst case interconnect pitch may drive package technology
  - Lack of chiplet marketplace and data (testability, thermal, pitch, interfaces, software, yield coverage, etc.)
  - Who owns chiplet inventory, yield, etc? (not an issue for vertical integration)
It Takes a Village

• Create elements with community reusability in mind
• Not all elements need advanced nodes
• It is likely that at least one device is custom (or an FPGA) and that will tie elements together
• IP vendors likely need to work with partners to market chiplets
• Many chiplet needs in voltage regulation, CPU, memory, etc.
• Opportunity for marketplace development in the industry
Thank You
Chiplet business challenges for AI accelerators

Arvind Kumar
IBM Research
ODSA March 2021 Business Workshop
IBM Research PoV on Chiplet Value Proposition

- IBM Research has developed an AI core optimized for DNN processing

- Many diverse use cases with varying core count, core functionality, memory, power envelope requirements.
  - New SoC for each new application not possible

- Value proposition of Chiplet-based ecosystem:
  Enable right-sized, modular solutions, integrating AI compute, I/O, and memory chiplets.
Different Use Cases have Different Requirements

<table>
<thead>
<tr>
<th>IoT / Sensor</th>
<th>Mobile</th>
<th>Automotive</th>
<th>Data Center</th>
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<tbody>
<tr>
<td>&lt; 100 mW</td>
<td>250 mW to &lt;2W</td>
<td>20-50W</td>
<td>75-300W</td>
</tr>
<tr>
<td>1-5 cores</td>
<td>20-50W</td>
<td>Tens to hundreds of cores</td>
<td></td>
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</table>

<table>
<thead>
<tr>
<th>AI workloads</th>
<th>Mainly inference</th>
<th>Training and inference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core count</td>
<td>Small</td>
<td>Large (even larger for training!)</td>
</tr>
<tr>
<td>Technology</td>
<td>Low power/older node</td>
<td>High performance/leading node</td>
</tr>
<tr>
<td>Power envelope</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Latency / throughput</td>
<td>Latency critical</td>
<td>Both may be important</td>
</tr>
<tr>
<td>Packaging</td>
<td>Low cost</td>
<td>Advanced packaging to support high BW</td>
</tr>
</tbody>
</table>

Chiplets: Composability and Scalability solution for wide variety of use cases
(networks, precision, memory, power envelope)
Chiplet Business Challenges

**Design Challenges:** Prototyping and Design Tools
- End-user applications constantly evolving:
  - New AI Workloads with new networks and different compute/memory balance
  - Need for rapid research prototyping of new AI cores (e.g., reuse nest)
- Chiplet+Package+PCB co-design EDA
  - Standardization of input/output formats across tools
  - Tools to support full implementation/verification flows (including complex CPI, thermal, etc.)

**Build Challenges:** Support for broad variety of IP in chiplet format (memory, I/O, accelerators)
- Open standards for I/O interfaces
- Interfaces and Packaging that can meet latency/bandwidth/power/thermal requirements

**Deliver Challenges:** Multi-vendor flexibility in supply chain
- Interoperability of silicon, package, assembly, test companies and methods to enable flexibility of chiplets and packaging options
Chiplet Business Challenges

A Perspective from Heterogeneous Integration Roadmap (HIR)

March 12th, 2021

William (Bill) Chen

ASE Group

In Collaboration with Heterogeneous Integration Roadmap (HIR) Technical Working Groups Team
Heterogeneous Integration Roadmap (HIR) Chapters
Covering the total Microelectronics Systems Ecosystem

System & Market Applications
- High Performance Computing & Data Center
- Mobile
- Medical, Health & Wearables
- Automotive
- IoT
- Aerospace & Defense

Co-Design + Simulation
- Co-Design
- Co-Simulation

Integration Processes
- SiP & Module
- 3D +2D & Interconnect
- WLP (fan in and fan out)

Building Blocks
- Single & Multi Chip Integration + Substrate
- Integrated Photonics
- Integrated Power Electronics
- MEMS & Sensor integration
- 5G Communication & Beyond

Cross Cutting Technologies
- Materials & Emerging Res Materials
- Emerging Research Devices
- Test
- Supply Chain
- Security
- Thermal Management

HIR Download link: https://eps.ieee.org/technology/heterogeneous-integration-roadmap
**HIR 4th Annual Conference Feb 24 – 26, 2021**

**Day 1 Symposium – Day 2 & 3 Cross TWG Workshop**

- **Symposium – 6 Plenary Speaker - - Vision on Heterogeneous Future**
  - “Future of Microelectronics after the Pandemic” Ajit Manocha President & CEO SEMI
  - “Reimagining Co-Design of HPC Systems for a Heterogeneous Future” John Shalf, LBL
  - “Accelerating Electronics & Photonics Innovations for Revolutionary Microsystems” Gordon Keeler DARPA
  - “Thermal Sciences for the Heterogeneous Future” Ken Goodson, Dept., Stanford University
  - “Charge to Heterogeneous Integration Roadmap Teams” Nicky Lu, CEO & Founder, Etron Technology Taiwan

- **Cross TWG Workshop**
  - 8 min presentation from all 22 TWG teams
  - Invited Chiplet speakers: Raja Swaminathan (AMD) & Bapi Vinnokota (ODSA/OCP & Broadcom)
  - SRC Program Director John Oakley on Heterogeneous Integration Science Programs
  - Cross TWG Workshop Value Proposition – The Whole of HIR Roadmap greater than the Sum of individual Chapters

Accelerating Electronics and Photonics Innovation for Revolutionary Microsystems

Dr Gordon Keeler
DARPA
February 24, 2021

HETEROGENEOUS INTEGRATION

Extending Moore's law and broadening our impact

1st Wave
Geometric Scaling
- DUV Lithography
- 1.0 0.5

2nd Wave
BEOL Scaling
- Low-k Cu Interconnects
- Bus width scaling

3rd Wave
3D Devices
- FinFETs
- High-k dielectric
- Silic engineering
- Multi-core architectures

4th Wave
Heterogeneous Integration
- Alternative materials
- Domain-specific functions
- 3D architectures

RF Phased Arrays – Radar & 5G
Improved Performance and System Scalability

Digital Sensors – Imaging
Scaling Pixel Array Size, Frame Rate, and Power


Facilitating DoD Access: Create an ecosystem for package-level optical signaling, enabling disruptive advances for artificial intelligence, phased arrays, sensors and processing.
• This TWG focuses on the need, requirements and solutions for realizing SYSTEM-IN-PACKAGE that integrate processing elements, accelerators, storage, IO for the following markets:
  • HPC Systems
  • Scale-out Systems
  • Data Centers
  • High-end Networking

• This TWG focuses on the system-level implications related to performance, power management, security, power distribution/conversion issues and others

• Emerging applications demand domain-specific accelerators
  • Analytics/Intelligence on demand
  • Big data processing
  • IoTs and Edge
  • Blockchain processing

• Emerging processing, accelerator and memory technologies, quantum computing driving new system architectures
Fan Out Heterogeneous Package Examples

2D & 3D Fan Out Packaging
- Chip Last Fan Out SiP
- Double Sided Fan Out POP
- Fan Out SiP with Selective Shielding
- Fan Out Antenna in Package (AiP)

Hybrid Fan Out on Substrate Variations
- Chip First Die Down
- Chip First Die Up
- Chip Last High Density
- Chip Last FO w/Bridge

Fan Out SiP

Multi Sourced Die + MEMS, XTALs, Filters, etc + Passives → Fan Out SIP
A Page from the HPC - Data Center TWG Presentation
Acknowledgement: Ken Lanier Feb 25, 2021

Test Technology Working Group, Heterogeneous Integration Roadmap Leadership Team
Dave Armstrong & Ken Lanier: Co-Chairmen

<table>
<thead>
<tr>
<th>Test Area</th>
<th>Leader</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5D/3D device test</td>
<td>Zoe Conroy</td>
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<tr>
<td>Analog and Mixed-signal Test</td>
<td>Don Blair</td>
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<tr>
<td>Cost-of-Test</td>
<td>Ken Lanier</td>
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<tr>
<td>Data Analytics</td>
<td>Ira Leventhal</td>
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<tr>
<td>Logic &amp; SOC Device Test</td>
<td>Marc Hutner</td>
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<tr>
<td>Memory Test</td>
<td>John Caldwell</td>
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<td>Photonic Test</td>
<td>Dave Armstrong</td>
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<td>Tom Brown</td>
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<td>Sylwester Latkowski</td>
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<td>RF Test</td>
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<td>System Level Test</td>
<td>Harry Chen</td>
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<td>Specialty Device Test</td>
<td>Wendy Chen</td>
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<td>Wafer Probe and Device Handling</td>
<td>Jerry Broz</td>
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The 2020 update to the test roadmap is output from a team of more than 120 test experts hailing from more than 50 companies world-wide. The leadership team for this effort is shown above.
IEEE Press Release 10-10-2019
PISCATAWAY, N.J.--(BUSINESS WIRE)--IEEE, the world's largest technical professional organization dedicated to advancing technology for humanity, today announced the 2019 release of the Heterogeneous Integration Roadmap (HIR), a roadmap to the future of electronics identifying technology requirements and potential solutions. The primary objective is to stimulate pre-competitive collaboration among industry, academia and government to accelerate progress. The roadmap offers professionals, industry, academia and research institutes a comprehensive, strategic forecast of technology over the next 15 years. The HIR also delivers a 25-year projection for heterogeneous integration of emerging devices and materials with longer research-and-development timelines.

- Sponsored by 3 IEEE Societies (EPS, EDS & Photonics) together with SEMI & ASME Electronics & Photonics Packaging Division
- Comprehensively covering microelectronics technology ecosystem
- Articulates state-of-the-art Advances in Technology & Science, Future directions, Significant roadblocks & Potential solutions
- Volunteers (60% industry, 30% Academia, 10% Research Institute)
Wrap-Up

• Since the HIR release Oct 10, 2019, Heterogeneous Integration Roadmap is making its mark in the global electronics ecosystem. Heterogeneous Integration Roadmap journey is off to a strong start

• ODSA & HIR share common objectives in fostering Chiplet Technology & accelerating Chiplet business implementation

• Packaging technologies for Heterogeneous Integration, serve as the crucial link for the design-build-deliver collaboration between the Wafer Foundry and the System Integrator

• AI & ML across stake holder collaboration & data sharing will build trust & mitigating risk across supply chain.
Thank You

william.chen@aseus.com

Acknowledgement : Heterogeneous Integration Roadmap Technical Working Groups Team

HIR Download link https://eps.ieee.org/technology/heterogeneous-integration-roadmap
Heterogeneous Acceleration

• Computational requirements are growing exponentially,
  • Driven by ML/DL/AI advances
• Application and algorithmic diversity is growing, and
• Loss of general purpose processor perf improvements
  – Due to diminishing Process technology benefits
    • $/Transistor is increasing
• Architectural innovations to keep pace
  • Resulting in Heterogeneous acceleration

• Potential for Splitting Functional Blocks into Chiplets
Silicon Design Flow

• 4 year design cycle with a delivery cadence of ~18 months
  - Requiring 1.5X team

• Tape out and Wafer costs, EDA tool costs continue to grow
  • Rightfully due to growing complexities

• ~150k Volume with ~50% margin needed to break even
  • Irrespective of size or complexity of the Chip

• Economies of Scale required often from broader set of Chips
  • Very hard to succeed on a single chip design

• Bottomline: There is little slack in Silicon Business
  • Proof is almost all the current Silicon companies

• CHIPLETS NEED to improve one or more of the above Business Risks
Chiplets: Use Cases, constraints

• Overcome Reticle limit
  • Perf sensitive
  • Functional, symmetric/perf breakup
  • May require parallel D2D interfaces and custom silicon interposer,

• Bringing Board/System into Package
  • Cost sensitive
  • Serial D2D and organic interposer may be sufficient

• Two distinct issues
  • Silicon companies broadly adopting Chiplets even within their own ecosystem
    - If reticle limit is not an issue, does Chiplets truly provide Perf/TCO?
    - Limitations of EDA Tools, Arch/design space exploration tools that take Chiplets into account
  • Relying on third party Chiplets
Chiplet Tax

- Increased design complexity
- Useful area vs Perimeter area
- Increased Power and latency of On-Die data movement going Off-Die
- Built in redundancy to ameliorate KGD problem
- Increased packaging costs
- Some upfront increased NRE and per Chiplet Tax
- Gov Initiatives and Industry consortium efforts help to establish the Chiplet Ecosystem: DARPA, HIR etc.
Standards vs Innovation

• Premature standardization can kill innovation
  • Standards are antithetical to innovation?
    ▪ If right boundaries/Interfaces are not chosen

• Standards cannot be least common denominator

• Too many open standards is as if no standard
  • Recent serial interface standards effort is the best example
    ▪ CCIX, GenZ, OpenCAPI
      ▪ Finally some convergence to CXL
        • Any lessons learned?
SW Ecosystem for Chiplets

- Mechanical, thermal, power delivery and IO standards
  - Chiplet Architecture Definition Language (cADL?)
- Chiplets management, monitoring SW
- Chiplet Debug SW
Chiplets: Challenges

- Well known Known Good Die (KGD) and all the related issues
- Who owns life time guarantees, Field debug
  - End users may have to share risk at least initially?
- Risk of relying on a third party Chiplet component for shipping a product
  - Marketplace with multiple choices could solve this problem
    - Chicken and Egg
- Companies of Different Breadth and Depth makes the Chiplet marketplace complicated
  - Key is to reduce risk, cost, time across the whole silicon design flow
  - Real or perceived value transfer could hinder Chiplet marketplace participation
Chiplets: Opportunities

• Enables separation of Concerns
  • High Complexity, low perf Block can be split off
    - Avoids taping out the whole SoC in case of a bug
    - Can be reused over multiple Gen
Thank you.
Chiplets for the Masses
Enabling a Vibrant Chiplet Design Ecosystem

Common language lowers design & cost barriers

**Standard D2D Interfaces**
Different use cases: One size does not fit all
- Parallel & Serial I/F
- Package technology (2D / 2.5D / 3D)
- NoC-to-NoC solution
- Security, Interoperability

**Unified 2.5D/3D IC Design Environment**
Package / Die co-design and verification tools
- Floor planning / Sims
- Signal & Power Integrity / Thermals

**Standard Test Infrastructure**
KGD & beyond
- Testability for KGD
- Hierarchical intra- & cross-die testability

Packaging & Assembly directions

**Access to Advanced Packaging**
3D not for the masses (yet?)
- Fanout reduces cost barrier
  - Access to “design kit” for design

Business Consideration for Chiplet based compute products

Rishi Chugh, Cadence Design
Business Consideration - Chiplet Based Modular Design

- Leverage SoC design investments across organization to **Optimize overall BOM cost**
- Optimize investment based off “**Node**” and “**SoC Application**” requirement
- Accelerate market adoption by **Standardization** specific to Chiplet designs:
  - Electrical / Functionality / Features
- Chiplet based design flow for **Predictability**
  - Methodology / Testability / Integration
- Foundry partner collaboration – **Yield & Integration**
- Leverage Chiplet design concept for next generation **SiP partitioning**
Serial or Parallel?

Disintegrated Design with Chiplets

- **External Connectivity Chiplet**
- **Node Ynm**
- **SoC Block Chiplet**
- **Node Xnm**
- **Stacked DRAM**

**Organic substrates**
- Yes
- No

**High Bandwidth**
- Yes
- No

**Complex interface**
- Yes
- No

**Higher power, latency**
- Yes
- No

**Low power, latency**
- Yes
- No

**Simple interface**
- Yes
- No

**Requires interposers for high density**
- Yes
- No

**Complex routing**
- Yes
- No
Chiplet Economic Constraints

--A Builder’s Perspective

Moderator: Andreas Olofsson, Zero ASIC
Panelists: Eelco Bergman, ASE
          Max (Sunghwan) Min, Samsung
          Regan Mills, Teradyne
          Swami Prasad, JCET
ODSA Goal Restated

Chiplets In Production Today! (...but only in vertically integrated form)

In AMD, INTEL, XILINX

NEW: 3rd Party Chiplet Players

Product Owner

Chiplet Catalog

Secret Sauce Block Design

System Design

Foundry

OSAT

The semiconductor zero sum manufacturing game grows from 3 players to 3+N players
## Builder Business Models

<table>
<thead>
<tr>
<th>Input</th>
<th>IP</th>
<th>Foundry</th>
<th>Assembly &amp; Test</th>
<th>PCB Assembly</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input</strong></td>
<td>“ideas”</td>
<td>Raw material Design</td>
<td>Wafers, substrates, interposers, raw materials, test</td>
<td>PCB, packaged parts, raw materials, test program</td>
</tr>
<tr>
<td><strong>Output</strong></td>
<td>IP</td>
<td>Wafers</td>
<td>Good parts</td>
<td>Good boards</td>
</tr>
<tr>
<td><strong>Market Size</strong></td>
<td>$5B</td>
<td>$80B</td>
<td>$30B</td>
<td>$4001B</td>
</tr>
<tr>
<td><strong>Gross Margin</strong></td>
<td>96%</td>
<td>54%</td>
<td>15%</td>
<td>7%</td>
</tr>
<tr>
<td><strong>Setup Costs/Margin</strong></td>
<td>0</td>
<td>$100,000 - $10M</td>
<td>$1,000 - $1M</td>
<td>$1,000 - $100,000</td>
</tr>
<tr>
<td><strong>Value of Unit Shipped</strong></td>
<td>N/A</td>
<td>1X</td>
<td>1.1X - 2X</td>
<td>2.1X - 4X</td>
</tr>
<tr>
<td><strong>Factory Test</strong></td>
<td>N/A</td>
<td>Wafer Acceptance Test</td>
<td>In circuit testing, AOI</td>
<td>In circuit testing, AOI</td>
</tr>
<tr>
<td><strong>Design Rules</strong></td>
<td>N/A</td>
<td>Fixed</td>
<td>Variable</td>
<td>Variable</td>
</tr>
<tr>
<td><strong>Yield</strong></td>
<td>N/A</td>
<td>10 - 99%</td>
<td>99%</td>
<td>90 - 99%</td>
</tr>
<tr>
<td><strong>Bad Unit Cost</strong></td>
<td>N/A</td>
<td>$0.1 - $150</td>
<td>$0.1 - $1,000</td>
<td>$1 - $10,000</td>
</tr>
<tr>
<td><strong>Yield Ownership</strong></td>
<td>Customer*</td>
<td>Customer*</td>
<td>Customer*</td>
<td>Customer*</td>
</tr>
<tr>
<td><strong>Warranty</strong></td>
<td>Up to license</td>
<td>New Wafers</td>
<td>Variable</td>
<td>Rework/Replacement</td>
</tr>
</tbody>
</table>
1. Advanced technology is hard and expensive.

2. Advanced technology & high volume is REALLY hard and expensive.

3. Advanced technology & high yield & low cost is “MOORE’S LAW” hard.

Model: $1/chiplet, $5/assembly.
Foundry View

- Max (Sunghwan) Min, Samsung
**CUBE for Enabling Chiplet** (Samsung Foundry View)

- CUBE is a device (interposer) connecting small and large chiplet(s) horizontally and vertically

```
Logic DRAM
---
PCB
---
HBM + Logic TSV  + D2W Cu–Cu  + D2D IP  + Logic chiplet (?)
```

- Challenges to be addressed for enabling chiplet
  - Heterogeneous (logic A/B + memory 1/2 + D2D α/β + decap + …) integration with OSAT and IP partners
  - Lots of test vehicles (MTV, TTV, FTV, CPI, …) confirming PPA (W, Hz, mm²) feasibility
    - Thermal & mechanical integrity
    - Signal & power integrity
    - Form factor
  - Known good chiplet and CUBE (yield)

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Known good active interposer</td>
<td>HBM2/2E/3 (HBM CUBE)</td>
</tr>
<tr>
<td>Logic on Logic (X CUBE)</td>
<td></td>
</tr>
<tr>
<td>Known good SI interposer</td>
<td>Thinned Si interposer (I CUBE)</td>
</tr>
<tr>
<td>TSV-less known good interposer</td>
<td>RDL interposer (R CUBE)</td>
</tr>
<tr>
<td>Flexible pitch/layer interposer</td>
<td>Embedded bridge (E CUBE)</td>
</tr>
</tbody>
</table>

[Diagram of CUBE with Logic and DRAM connections]
Assembly & Test

• ASE – Eelco Bergman
• JCET– Swami Prasad
• Teradyne – Regan Mills
Converging Solutions & Business Models
OSAT & EMS

1990's
2000's
2010's
2020's

Disaggregated SoC
SoC w/ Integrated IP
Monolithic SoC

Virtual SoC
3rd Party IP Chiplets
KGD/KGC
Homo/Hetero Int.
3DIC / Hybrid Bond
Organic or Si substrate

Wearable SiP
Smartphone System Board
PC Mother Board

MCM
KGD
2D Flip Chip
Bare die

PCBA
Tested Components
SMT
Packaged Die

Single Die
Probed Die
Wire Bond
Die Integration

MCM
KGD
2.xD Flip Chip
Pkg Integration
Single Die/Current Business Flow

- POR: Package, Test Specs provided by the customer
- Silicon, Memory Package/s are consigned
- Substrate, Passives can be consigned or purchased
- Process Flow - Wafer Sort, Assembly, Final Test/System Level Test
Chiplet Business Flow

1. Product Ownership
2. Source of PO
3. End Customer or Semi Provider
4. Liability considerations
5. Technology
6. Cost Options
7. Design
8. Test Methodology
9. Quality
10. Supply Chain
11. OSAT as Integrator
12. Sourcing
13. Commercial Engagements
Value of Quality – A Shift with Chiplets

Monolithic Silicon – Single Die, Single Package

- Fab
  - Wafer Test
  - Fail/Scrap
- Pkg
  - Pkg Test
  - Fail/Scrap
- System Level Test
- Shipments

Chiplet Heterogeneous Solution – Multiple Die, Single Package

- Fab
  - KG
  - D
- Assembly to Substrate
  - Test
- Assembly to Substrate
  - Test
- System Level Test
- Shipments

Cost Factors

- SLT req’d for some devices to achieve AQLs
- Potential to move SCAN in SLT to reduce cost

Cost Factors

- Rapidly accumulating costs as die are mounted
- No/Limited rework capability (different than PCB assembly)
- Cost of bad die drives KGD methodology
- Possible need for intermediate test of assembly to maximize yield at final stage
- Pre-combinations of die (single supplier cubes) viable to reduce the multiplicative impact of yield

Cost Pressure to push Quality Upstream
Comprehensive Cost Model for Optimization
Chiplet Manufacturing
Packaging and Test Technical Considerations Directly Impact Economics

Quality - Known Good Die
- Who is responsible for quality of die?
- What is the economic model for an escaped bad die? Cost of a simple IP chiplet may be insignificant to the cost of the ruined assembly.
- How to ensure quality of substrate?
- Testability concerns with IP blocks which are designed to be verifiable but not testable in stand-alone manufactured state; additional die area (cost adder) may be required for testability

High Speed Interfaces
- Driver strength limited for cost reasons, need test bumps and drivers
- Die loopback & adequate design margin for economic wafer test to support KGD
- HBM-like redundancy viable in some cases

High Speed Interconnects
- Substrate a key part of system performance => is substrate test required?
- Full system level test likely required to find 2nd order interactions between die and substrate -> full system simulation environment key to yield at EOL

Interoperability
- Extension of existing test standards required to allow efficient test setup for interface/interoperability testing
- Industry adoption of test standards will drive test costs down
Thank You
Deliver / Business Panel

- **Moderator**: Dave Greenfield - Intel
- **System Integrator**
  - Microchip: Anu Ramamurthy
  - Marvell: Ramin Frajadrad
- **End Users**
  - Google: Ben Kerr
  - Alibaba: Weifeng Zhang
  - FB: Nicolaas Viljoen
  - Microsoft: Ishwar Agarwal
Chiplet Business Collaboration

Dave Greenfield – Intel Corporation
Agenda

- What’s the problem?
- Scope the opportunity
- Case Study: identify key challenges
- Additional “learning
### Use Case I/O Power Example

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Sub-6GHz NR</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF frequency</td>
<td>3.5-6GHz</td>
</tr>
<tr>
<td>Number of TR</td>
<td>64T/64R¹</td>
</tr>
<tr>
<td>IBW (MHz)</td>
<td>200</td>
</tr>
<tr>
<td>JESD204C lanes²</td>
<td>53</td>
</tr>
<tr>
<td>JESD power now (W)³</td>
<td>106</td>
</tr>
<tr>
<td>JESD power future(W)³</td>
<td>53</td>
</tr>
<tr>
<td>AIB power now (W)⁴</td>
<td>5.3</td>
</tr>
</tbody>
</table>

There must be a **compelling** reason to use MCP vs. discrete option!
**Intel Disaggregated Design**

- Intel developed POC with DARPA CHIPS program partnering with external supplier
- Intel released analog FPGA technology announcement in Q4-2020 to enable future products
- Intel Programmable Solutions Group (Altera) leader is disaggregation strategy


Business Case for MCP

• What’s the cost to productize the MCP (probably not 6-digit cost)?
  • Who’s doing the work?
  • How extensive is validation work?
  • How many units needed for volume validation?

• Do the chiplets exist (off-the-shelf vs. development project)?
  • Significantly different set of challenges if 2nd party needs to develop new chiplet
  • Why bring in development partner?

• What’s the market opportunity?
  • Size the market, assess the risk, estimate time to productize . . .
FPGA Case Study

• How do we share the revenue?
• How handle IP ownership?
• How address supplier risk (acquisition / continuity of supply)?
• How connect with supply team?
• How address funding challenge (development & productization)?
The “Deal”

- **Key Term Sheet Details**
  - NRE to accelerate product development
  - KGD deal with escrow provisions
  - IP: define ownership & license rights
  - Define exclusivity terms
  - Define impact of schedule delays (who takes on product risk)?
  - What if known good die isn’t actually good? Yield fallout (chiplet could be low % of high MCP cost) – define acceptable defect density & resulting terms?
Extra Provisions (Stuff We Learned Along the Way)

- Units for test (need a large amount of die) – who pays & what price?
- Who owns IP rights to packaging IP between chiplets?
- How much uncertainty on technical issues with SOW can we live with?
Summary

• Find a pathfinding opportunity for business model and KGD exploration
• Easier to deal with revenue sharing challenges in market where there is ample margin to share than in cost sensitive market
• Identify a compelling technology solution (size, weight, power, cost, yield . . .) vs. finding a market that wants to save area
Chiplet Business Enablement
‘Deliver Panel’

Anu Ramamurthy – Microchip Technology
March 2021
Chiplet Business Problems to Solve

**Cost Reduction**
- Re-use existing silicon
- Reduce R&D cost
- Fast product SKU development

**Fast Innovation**
- Ability to innovate at different process nodes – no soup to nuts in 3nm
- Impact operation costs via smaller die and improved yields
- Adding 3rd party IP into Microchip IP library (spanning 300nm-6nm)

**Standardization**
- D2D interface supporting variety of packaging options
- Pin templates for multi-vendor integration

**Operations**
- Agreed upon KGD tests to allow foundries to ship to OSATs for assembly and integration
- Common security protocols across supply chain
- Solid Supply chain

**Solid Supply chain**
- Allows for more players in the market and creates a viable ecosystem

Anu R
Anu.ramamurthy@microchip.com
Microchip Technology
Delivering Chiplet-based Products

Ramin Farjadrad
CTO & VP of Automotive/Networking PHYs
Marvell
Chiplet-based use cases

- **Large SoC Disaggregation**
  - Partition large die to improve yield
  - Reduce development cost & time-to-market
  - Use optimized process technology per functions

- **System-in-Package (SiP)**
  - Higher performance systems
  - Smaller footprint
  - Lower power
**Building systems with chips vs chiplets**

Chiplet-based Systems can be built similar to systems with Chips today

**Conventional System OEMs**
- Receive good Chips screened at production test
- Connect good Chips together with **Interoperable Standard interfaces**
  - **PHY Layer**: PCIe, DDR Bus
  - **MAC Layer**: CXL, DDR Controller
- Test the final system

**System-in-Package OEMs**
- Receive known-good-die (KGD) screened at wafer test
- Connect KGD Chiplets together with **Interoperable Standard interfaces**
  - **PHY Layer**: XSR, BoW, HBM
  - **MAC Layer**: AXL, CXL, HBM Controller
- Test the final System in Package (SiP)

---

*Proprietary interfaces are perfect options for vertical integration/Captive Systems*
Interface routability is the KEY

- **Without D2D routability, all Chiplets need to perfectly match side by side**
  - Cannot have *one-size-fit-all* Chiplets
    - Exceptions: New ASICs that can be designed to fit nicely with all Chiplets

- **Proper D2D routability is required to enable SiP implementation with off-the-shelf Chiplets**
  - Chiplets-based SiPs should have PHYs with reasonable reach (~1 inch)
    - Similar to conventional systems,
Interface routability is the KEY

- Without D2D routability, all Chiplets need to perfectly match side by side
  - It defines the purpose of Chiplet-based systems, if we need to build several Chiplets per function with different dimensions optimized for target system
  - Exceptions: New ASICs that can be designed to fit nicely with all Chiplets

- Proper D2D routability is required to enable SiP implementation with off-the-shelf Chiplets
  - Similar to conventional systems, Chiplets-based SiPs should have PHYs with reasonable reach (~1 inch)
High-coverage screening is a necessity

Chiplet screening challenge:
- KGD screening must happen at Wafer level
- Wafer-level test coverage must be high
  - Yield target >99%

The μ-bump challenge:
- Wafer probe limitations with μ-bump limits screening coverage
- High-speed interconnect coverage
  - At-speed full-link test not possible
Summary

- Chiplets can be potentially marketed/sold like traditional Chips
- Similar key processes need to exist
  - Standardization of Interface for Inter-Chiplet links
  - Routability of links for practical Chiplet placements
  - Wafer-level screening with high defect coverage
    - A challenge for Chiplets with μ-bumps
- Support to be similar to today’s SoC/System model. SiP vendors
  - will be responsible to support their direct customers
  - work with their Chiplet providers to resolve their SiP issues
Disclaimer

SLIDE CONTENT REPRESENTS THE COLLECTIVE VIEW OF ALL ODSA END USER WORK GROUP MEMBERS, AND DOES NOT REPRESENT THE POSITION OF ONE SPECIFIC MEMBER.
Enabling a Chiplet Marketplace

• The Need for Chiplets

• “Gaps” and “Gives”
  • Business and Commercial
  • Technical
  • Software and Management

• Chiplet Opportunity
The Need for Chiplets

• Critical system IPs are not scaling at the same pace as logic
• Large, monolithic die yield badly
• Fab cycles are longer at advanced nodes
• Faster time-to-market leveraging proven chiplets
• Clear need to enable a chiplet marketplace ecosystem
## Business and Commercial

<table>
<thead>
<tr>
<th>Gaps</th>
<th>Gives</th>
</tr>
</thead>
<tbody>
<tr>
<td>● Multi-source die available from &gt;1 supplier</td>
<td>● Known-Good Die (KGD) supply model</td>
</tr>
<tr>
<td>● Supply chain guarantees</td>
<td>● Broad IP availability</td>
</tr>
<tr>
<td>● OSAT complexity, inventory, availability and capacity</td>
<td>● Established distribution channels</td>
</tr>
<tr>
<td>● Business model innovation</td>
<td></td>
</tr>
</tbody>
</table>
## Technical

### Gaps

- Open Chiplet Specification (work in progress)
  - Common die footprints with multiple form-factors
  - Die-to-die interfaces
    - ODSA BoW and OpenHBI physical layer
  - Protocol adapters
  - Datasheet parameters
  - Design collateral

- Reference designs for characterization and interoperability
## Software and Management

<table>
<thead>
<tr>
<th>Gaps</th>
<th>Gives</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Robust and secure chiplet discovery mechanism</td>
<td>- Simple out-of-band hardware interface</td>
</tr>
<tr>
<td>- Chiplet telemetry data</td>
<td>- Open management interface and protocol</td>
</tr>
<tr>
<td>- Managing package-level resources</td>
<td>- Common, extensible management API</td>
</tr>
</tbody>
</table>

**Open Chiplet Specification**
End-User Chiplet Applications

• BoW to PCI-Express
  ➜ External interface and self-contained end-point (backup)

• BoW to many other high-speed interfaces
  ➜ Usage in data-comms (LAN & WAN), tele-comms (5G/OpenRAN), proprietary intra- and inter-rack comms

• Enabling system expansion through SKU modularity

• Advanced interconnect solutions
Chiplet Opportunity

• Chiplet marketplace TAM is potentially very large

• “Gives” are well understood and there are many development threads are in flight within ODSA

• “Gaps” are solvable - the industry already knows how to do this
  – Open Chiplet Specification

• The chiplet marketplace ecosystem momentum is building...
Backup

Available for reference during panel session
PCI-Express Chiplet Solutions

**#1: PCIe PHY**

- **CPU**
- PCIe Root Complex or End Point

**#2: PCIe Expansion**

- **CPU**
- PCIe Root Complex

---