OCP FUTURE TECHNOLOGIES SYMPOSIUM

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Wide Parallel LED-Based Optical Links for Chip-to-Chip Applications

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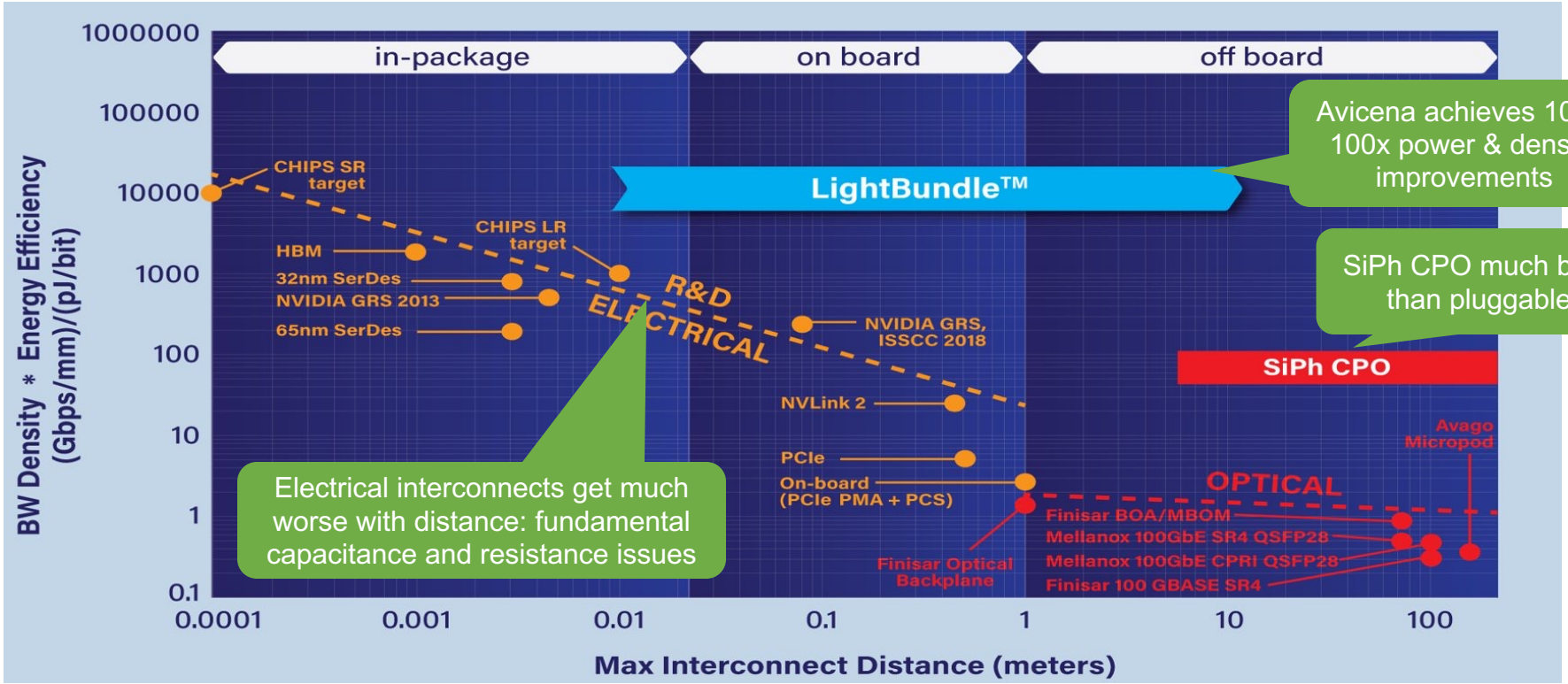
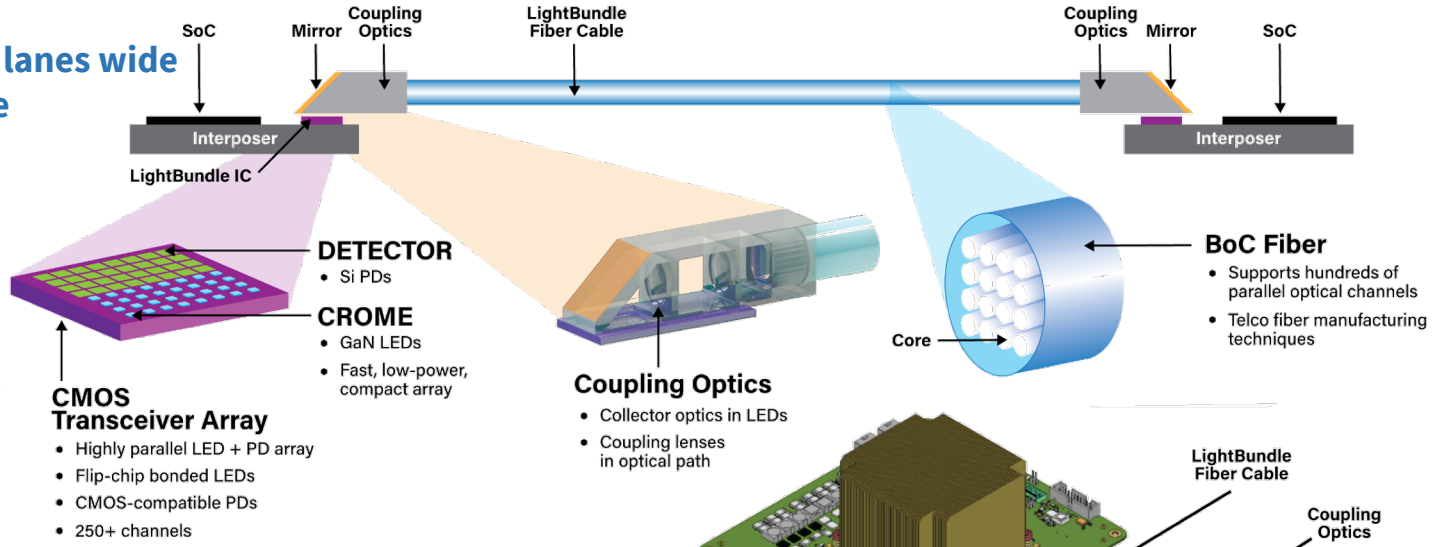
Problem: Interconnect Power and Density Limits

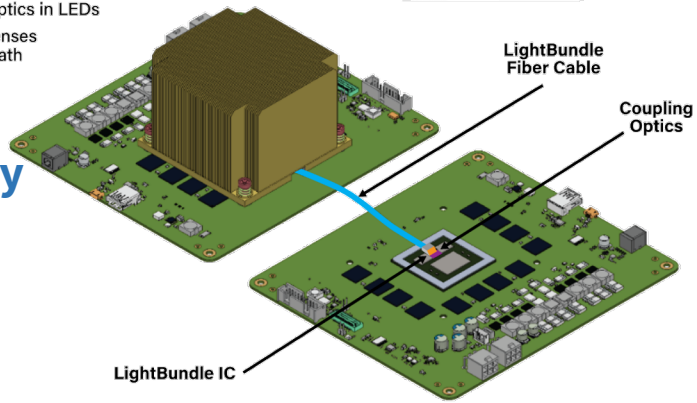


LightBundle™ – Highly Parallel Optical Links

- 100s – 1000s of lanes wide
- 1 – 10Gbps/lane
- N x 1Tbps links



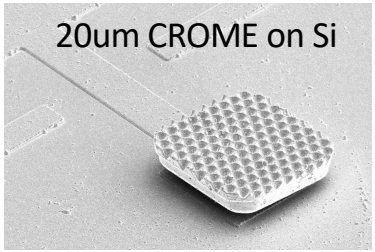
Using a "display" to move data



Remarkable power efficiency and density

- < 0.5pJ/bit
- > 10Tbps/mm^2
- > 1Tbps/mm

Key Points

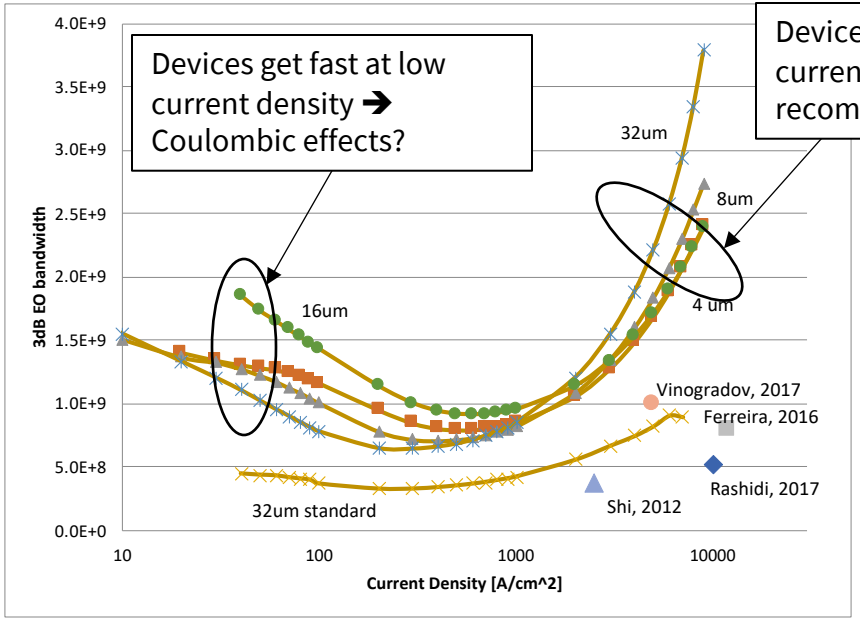


- **CROME™** (Cavity-Reinforced Optical Micro-Emitter): Optimized GaN LED enables 10Gbps/lane using blue light (λ ~ 430nm)
- **Si PDs:** Great in the blue: very short absorption length enables very low C CMOS-compatible detectors
- **BoC™** (Bunch of Cores) **fiber**: Hundreds of multimode cores (~50um core diameter) in ~1mm diameter fiber
- **Highly parallel links:** Typical is 256 lanes x 4Gbps/lane = 1Tbps
- **Relaxed packaging alignment:** Tolerances ~ +/-5um support passive alignment

Keys to Very Low Power Dissipation

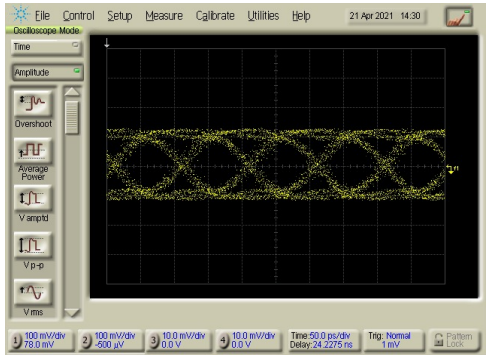
- Very small (~10um x 10um) OE devices have very low CV^2 power
- LEDs have no threshold current so can be operated at << 1mA
- OE devices can be integrated close to/onto SoCs being interconnected
  ➔ very low electrical interconnect power to optical transceivers
- No need for high-speed SerDes, FEC, ….

Transmitters using CROMEs

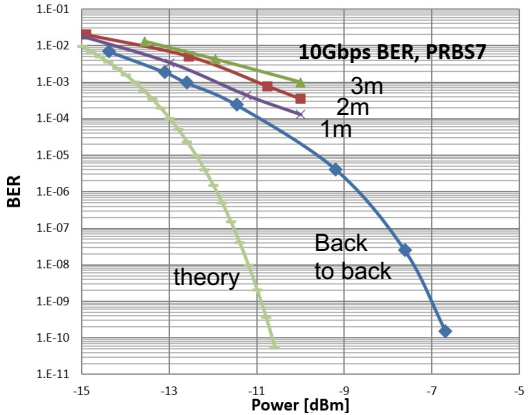


- World's fastest LEDs!
- Data rates up to 10Gb/s so far (with 6dB equalization)
- Devices are fast at high current density ($J > 1kA/cm^2$) due to increased non-radiative recombination (e.g. Auger)
- In high-quality epi, also can be fast in low current density ($< 100A/cm^2$) regime
- Can trade off efficiency and modulation BW
  - Lighting LEDs can be 90% efficient so lots of efficiency to give …

Link Performance

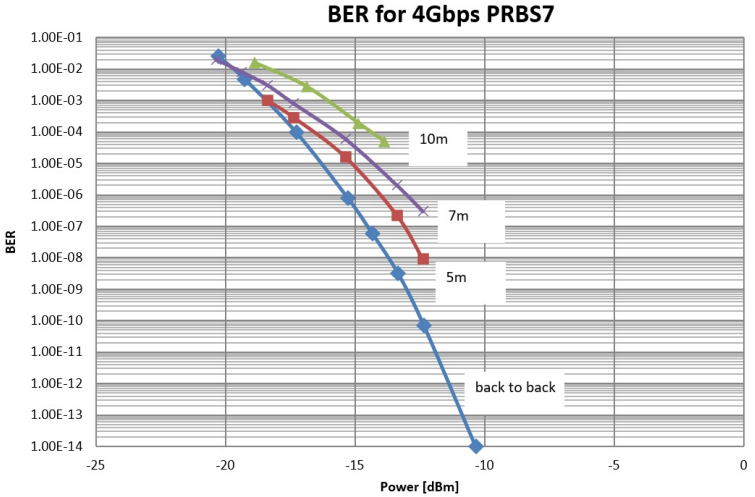


10Gb/s eye (~6dB equalization)



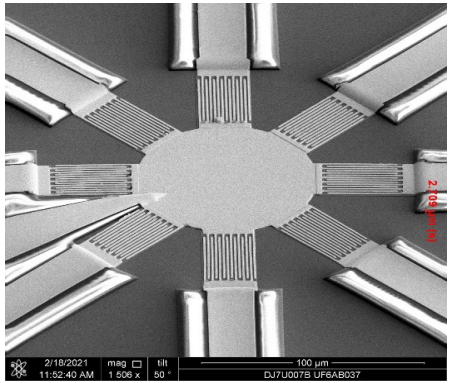
10Gb/s BER

- No error floors down to BER < 1e-15
- Dispersion penalties
  - Modal and chromatic dispersion contributions
  - 10Gb/s, 3 meters: 3dB penalty



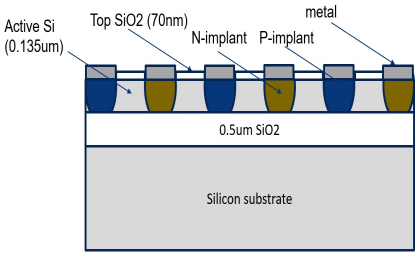
Excellent Blue PDs in Silicon

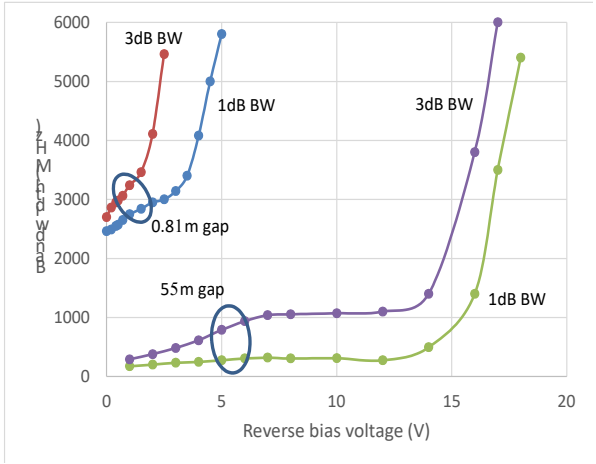
- Blue light is absorbed very fast in silicon – allows large, low capacitance detectors
- Interdigitated structure can be made CMOS-compatible



8-element PD array using interdigitated p-i-n structure

CMOS-compatible PD structure



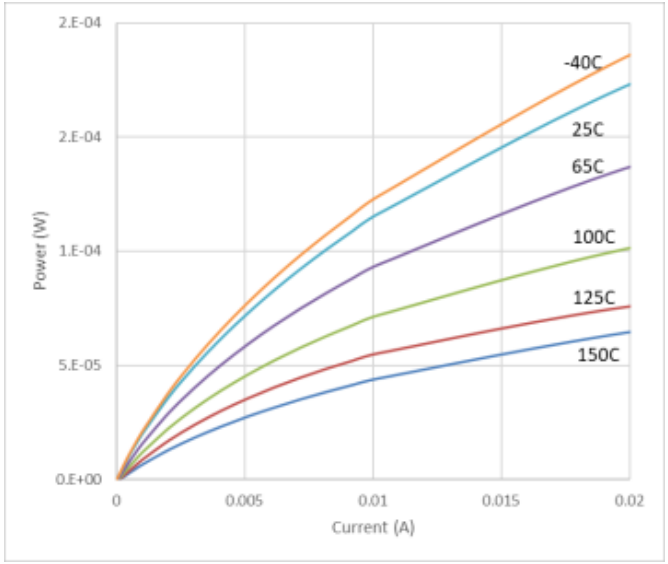


S21 detector measurements

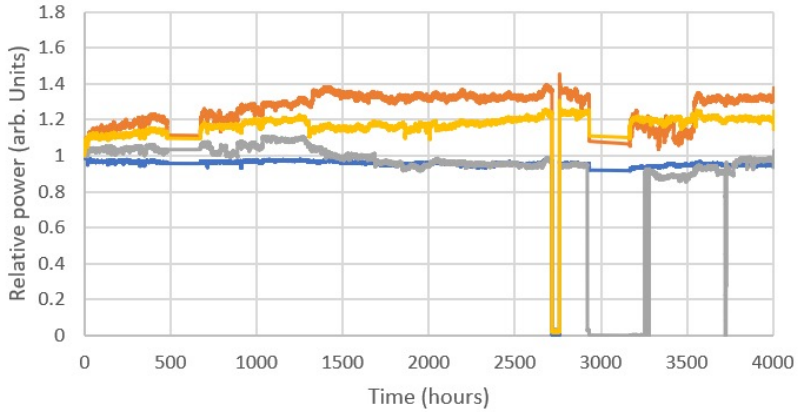
- Speed limited by 6GHz instrument
- Estimate C < 10fF for 30µm diameter

Temperature Performance and Initial Reliability

- Much less sensitive to temperature than lasers
- Initial life test of handful of devices looks OK



L-I from -40˚C to 150˚C



Life test at 100˚C heatsink and 1.5kA/cm^2

BoC Fiber

- Based on “imaging” fiber with thousands of cores ➔ each optical lane can be carried in multiple cores
- Fiber optimized for LightBundle links needs only a few hundred cores ➔ 1 core per lane

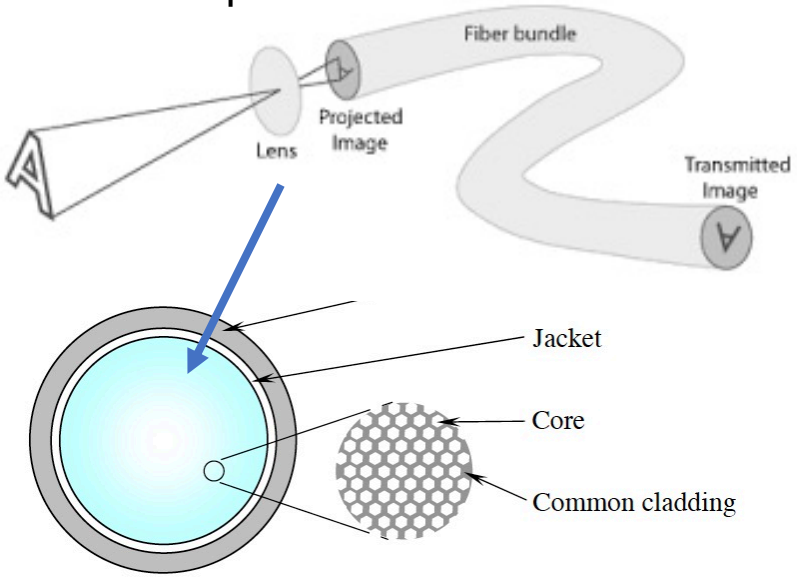
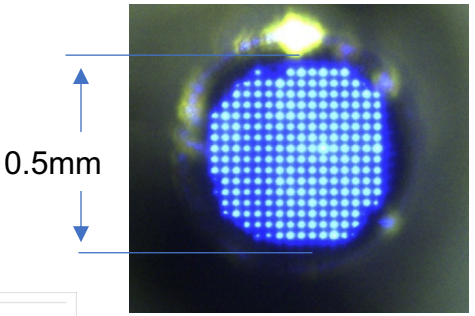
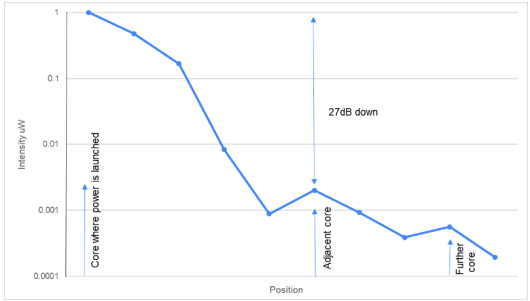


Image of output facet of the fiber

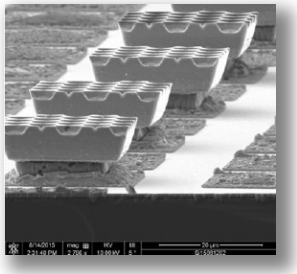




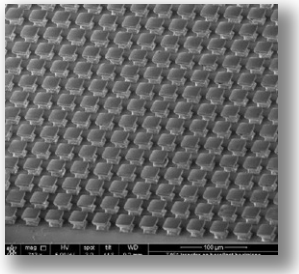
Measured crosstalk between adjacent cores < -27dB

Leverage MicroLED and Lighting Ecosystems

- Massive GaN lighting industry
- Massive upcoming GaN uLED display production volumes
  - Apple, Samsung
  - Transferring/assembling uLEDs onto silicon backplane
- Mature optical fiber manufacturing industry



20um LEDs on CMOS



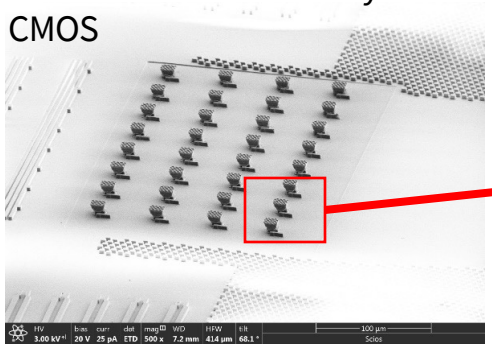
Large array transferred to substrate

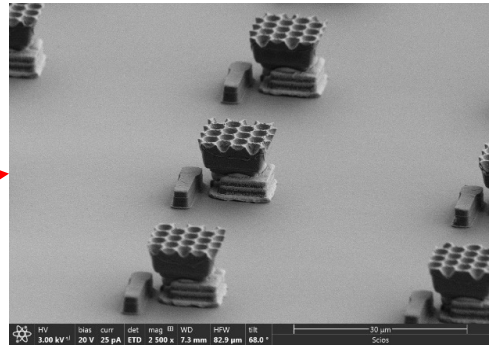
Commercial laser lift-off (LLO) system transfers GaN LEDs from sapphire to Si substrate

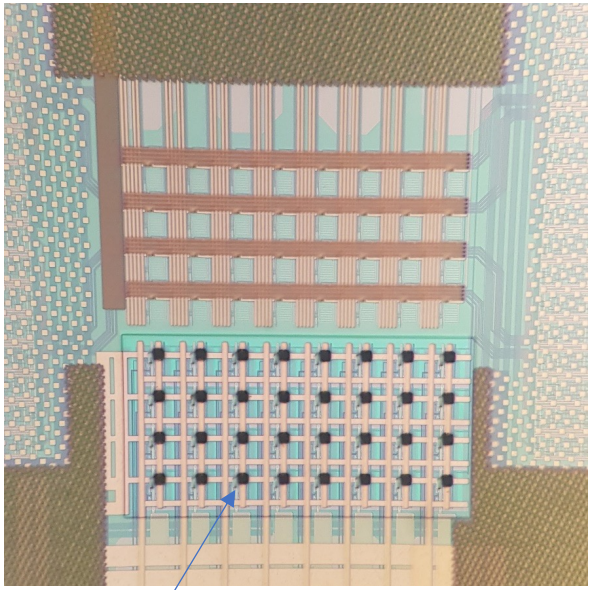
Status

- Testing ASIC with various arrays up to 128 Tx + 128 Rx x 2Gbps (130nm CMOS)
- Arrays of CROMEs transferred to ASIC using laser lift-off
- Developing higher performance product ASIC for in 16nm CMOS
- Working with supply chain partners on volume manufacturing of CROMEs, BoC fiber, packaging

32 element CROME array on CMOS







Lifted-off devices on 130nm ASIC

A truly revolutionary new paradigm

- Highly parallel optical links with > 10x improvements in power dissipation and density over any approach on the horizon
- Multimode packaging tolerances
- Very low cost components

➔ Will GPUs, CPUs, and Memory have LightBundle interfaces in the future?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