ODSA POC Mara Baseboard Specification

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Mara Baseboard Spec Overview

- Baseboard FF: FHFL PCIe card as defined by SNIA
- Three Pchiplet slots with two Molex mirror Mezz connectors per slot
  - Pchiplets interchangeable across slots
  - Support variety of Chiplet use cases
  - Support for Server Host, Network and Storage interfaces
- Protocol Agnostic Full Mesh HSIO Wiring Topology for Pchiplets
  - Support Embedded, Common clock and Source Synchronous clocking modes
  - Low loss links supporting very high data rates
- Dedicated Management Links for Pchiplet / Peripheral Management
  - Secure boot, Voltage Sequencing, Configuration, Status Monitoring
- Interface support for Test and Bringup
- 200W Power Budget with 12V and 3.3V Power rails
Pchiplet Connector Interface

**Signaling**

<table>
<thead>
<tr>
<th>Ethernet 4-lanes</th>
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<tbody>
<tr>
<td>PCIe 4</td>
<td>PCIe G3/4 x4 EP</td>
<td>PCIe G3/4 x8 (x4) RC</td>
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<td>PCIe 3</td>
<td>PCIe G3/4 x8 (x4) RC</td>
<td>PCIe G3/4 x16 (x8) EP</td>
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<td>PCIe 2</td>
<td>PCIe G3/4 x8 (x4) RC</td>
<td>PCIe G3/4 x16 (x8) EP</td>
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<tr>
<td>PCIe 1</td>
<td>PCIe G3/4 x4 EP</td>
<td>PCIe G3/4 x8 (x4) RC</td>
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2x Molex Mirror Mezz Connectors with 76 diff pairs (J1 and J2)

- **Pchiplet detects its slot**
- **Pchiplet announces its slot to others**
Inter-Pchiplet traces are capable of up to 100G signaling with controlled impedances. Can support multiple HSIO signaling and clocking (PCIE, ETH, LVDS and BoW).

18 Layer EM891 Low Loss Dielectric
Test and Bring up Interfaces

Daisy chained JTAG Interface for Pchiplet Boundary Scan

Pchiplets UART Interface for Pchiplet Bringup / debug
Reset and Clocking Scheme
Power Supply Scheme

2 x 4 AUX PWR CON

2 x 4 AUX PWR CON

Linear Tech Module

DC-DC Converter

LTM4620A

12V

12V

3V3, 26A

50W PCHIPLET-A

50W PCHIPLET-B

50W PCHIPLET-C

QSFP Modules

FPC202 x2

M.2 SSD x2

PWR LED

Open. Together.
Thank You