ODSA POC Mara Baseboard Specification

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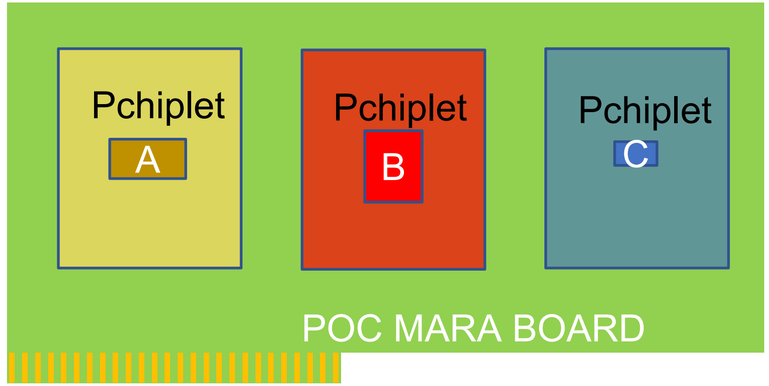
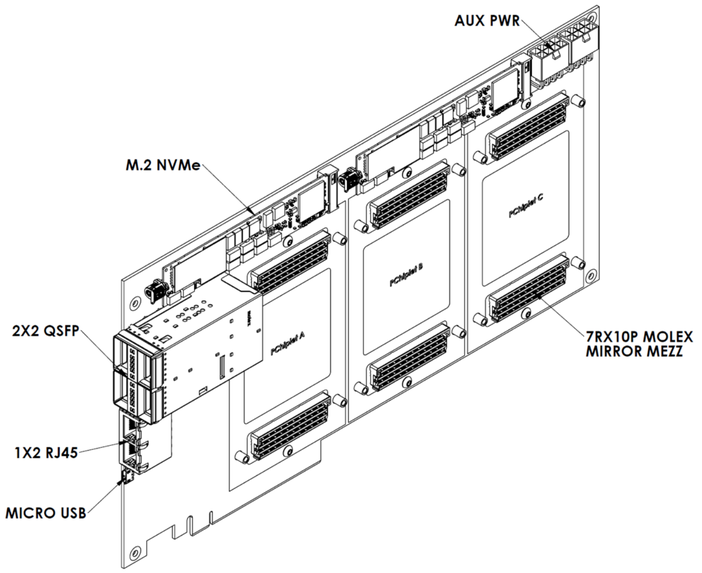
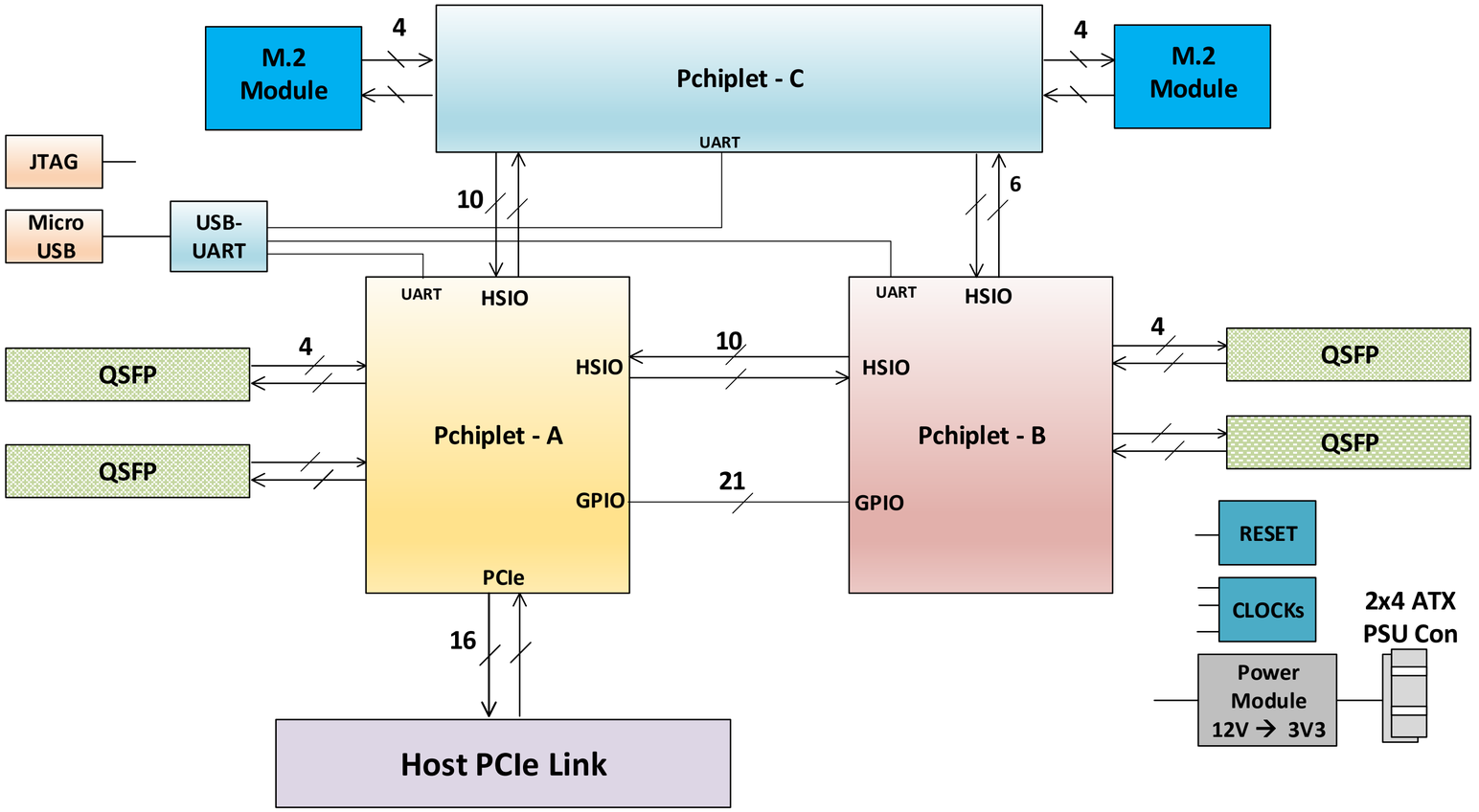
Mara Baseboard Spec Overview

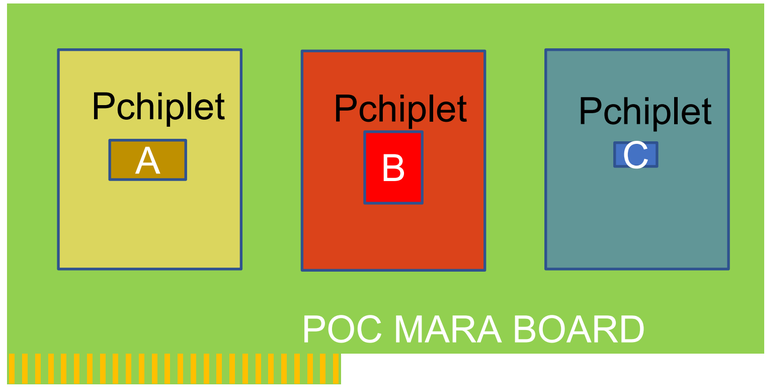
- Baseboard FF: FHFL PCIe card as defined by SNIA
- Three Pchiplet slots with two Molex mirror Mezz connectors per slot
  - Pchiplets interchangeable across slots
  - Support variety of Chiplet use cases
  - Support for Server Host, Network and Storage interfaces
- Protocol Agnostic Full Mesh HSIO Wiring Topology for Pchiplets
  - Support Embedded, Common clock and Source Synchronous clocking modes
  - Low loss links supporting very high data rates
- Dedicated Management Links for Pchiplet / Peripheral Management
  - Secure boot, Voltage Sequencing, Configuration, Status Monitoring
- Interface support for Test and Bringup
- 200W Power Budget with 12V and 3.3V Power rails





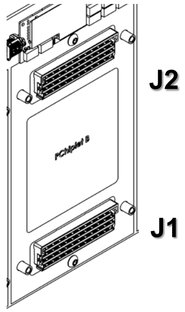
Mara Baseboard Architecture





Pchiplet Connector Interface

Signaling



LSIO

PWR / GND
UART / JTAG
GPIO
Presence/SlotID
I2C
I2C
I2C

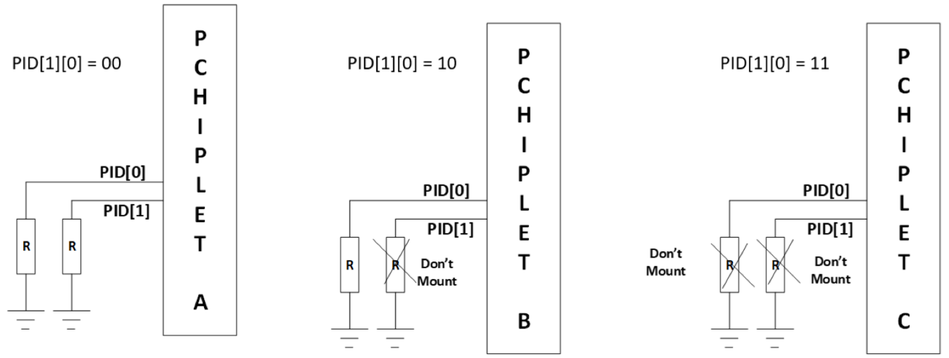
HSIO

Eth 3	Ethernet 4-lanes
Eth 2	Ethernet 4-lanes
Eth 1	Ethernet 4-lanes
PCIe 4	PCIe G3/4 x4 EP
PCIe 3	PCIe G3/4 x8 (x4) RC
PCIe 2	PCIe G3/4 x8 (x4) RC
PCIe 1	PCIe G3/4 x16 (x8) EP

2x Molex Mirror Mezz Connectors with 76 diff pairs (J1 and J2)

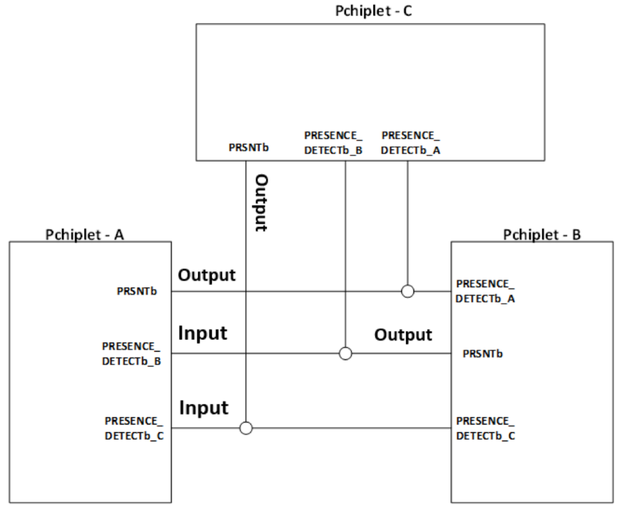
J2	64	63	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20
A			G	G	ETH2_RX1P	ETH2_RX1P	G	G	ETH2_RX2P	ETH2_RX2P	G	G	ETH2_RX3P	ETH2_RX3P	G	G	ETH2_RX4P	ETH2_RX4P	G	G	ETH3_RX1P	ETH3_RX1P	G	G	ETH3_RX2P
B			12V	GPIO_1	G	G	UART_Rx	UART_Tx	G	G	NC	NC	G	G	NC	NC	G	G	NC	NC	G	G	P1REFCLKN	P1REFCLKP	G
C	12V	12V	G	G	ETH2_TX1P	ETH2_TX1P	G	G	ETH2_TX2P	ETH2_TX2P	G	G	ETH2_TX3P	ETH2_TX3P	G	G	ETH2_TX4P	ETH2_TX4P	G	G	ETH3_TX1P	ETH3_TX1P	G	G	ETH3_TX2P
D	G	G	12V	ID[1]	G	G	P1RX2N	P1RX2P	G	G	P1RX4N	P1RX4P	G	G	P1RX6N	P1RX6P	G	G	P1RX8N	P1RX8P	G	G	P1RX10N	P1RX10P	G
J	12V	12V	G	G	P1RX1N	P1RX1P	G	G	P1RX3N	P1RX3P	G	G	P1RX5N	P1RX5P	G	G	P1RX7N	P1RX7P	G	G	P1RX9N	P1RX9P	G	G	P1RX11N
K			12V	ID[0]	G	G	P1TX2N	P1TX2P	G	G	P1TX4N	P1TX4P	G	G	P1TX6N	P1TX6P	G	G	P1TX8N	P1TX8P	G	G	P1TX10N	P1TX10P	G
L			G	G	P1TX1N	P1TX1P	G	G	P1TX3N	P1TX3P	G	G	P1TX5N	P1TX5P	G	G	P1TX7N	P1TX7P	G	G	P1TX9N	P1TX9P	G	G	P1TX11N

J1	64	63	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20
A			G	G	ETH1_TX3N	ETH1_TX3P	G	G	P4TX1N	P4TX1P	G	G	P4TX3N	P4TX3P	G	G	P2TX1N	P2TX1P	G	G	P2TX3N	P2TX3P	G	G	P2TX5N
B			ETH1_TX2N	ETH1_TX2P	G	G	ETH1_TX4N	ETH1_TX4P	G	G	P4TX2N	P4TX2P	G	G	P4TX4N	P4TX4P	G	G	P2T2N	P2TX2P	G	G	P2TX4N	P2TX4P	G
C	ETH1_TX1N	ETH1_TX1P	G	G	ETH1_RX3N	ETH1_RX3P	G	G	P4RX1N	P4RX1P	G	G	P4RX3N	P4RX3P	G	G	P2RX1N	P2RX1P	G	G	P2RX3N	P2RX3P	G	G	P2RX5N
D	G	G	ETH1_RX2N	ETH1_RX2P	G	G	ETH1_RX4N	ETH1_RX4P	G	G	P4RX2N	P4RX2P	G	G	P4RX4N	P4RX4P	G	G	P2RX2N	P2RX2P	G	G	P2RX4N	P2RX4P	G
J	ETH1_RX1N	ETH1_RX1P	G	G	P1_TXVD_N	P1_TXVD_P	G	G	P4REFCLKN	P4REFCLKP	G	G	GPIO3	GPIO4	G	G	GPIO9	GPIO11	G	G	GPIO15	GPIO16	G	G	P2REFCLKN
K			P1_TXVC_N	P1_TXVC_P	G	G	P1_TXVB_N	P1_TXVB_P	G	G	GPIO1	GPIO2	G	G	GPIO7	GPIO8	G	G	GPIO13	GPIO14	G	G	GPIO19	GPIO20	G
L			G	G	P1_TXVA_N	P1_TXVA_P	G	G	G_PORT_LED	G_PORT_LED	G	G	GPIO5	GPIO6	G	G	GPIO10	GPIO12	G	G	GPIO17	GPIO18	G	G	GPIO21



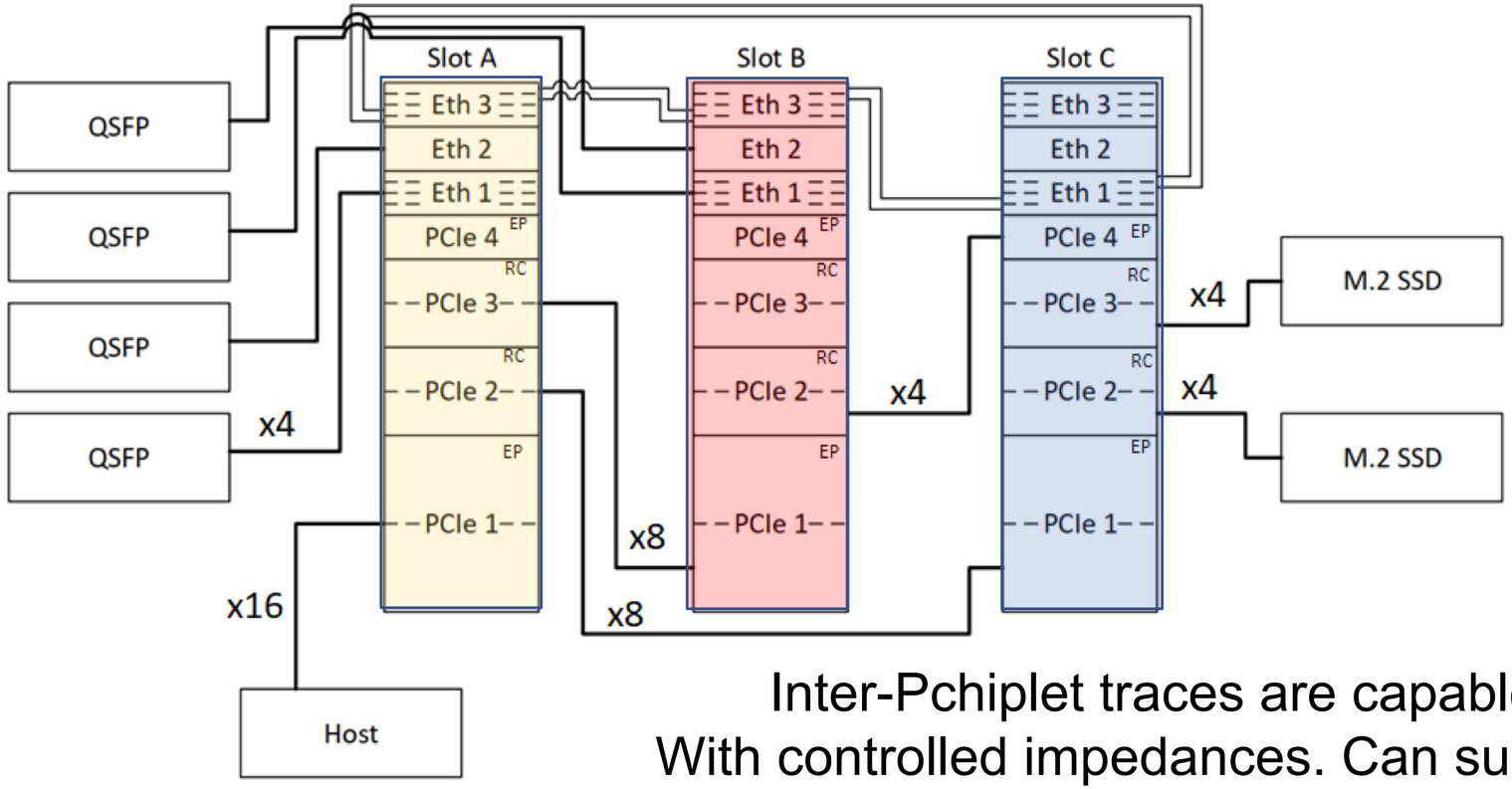
PID[0], PID[1] will be pulled up by default inside each Pchiplet

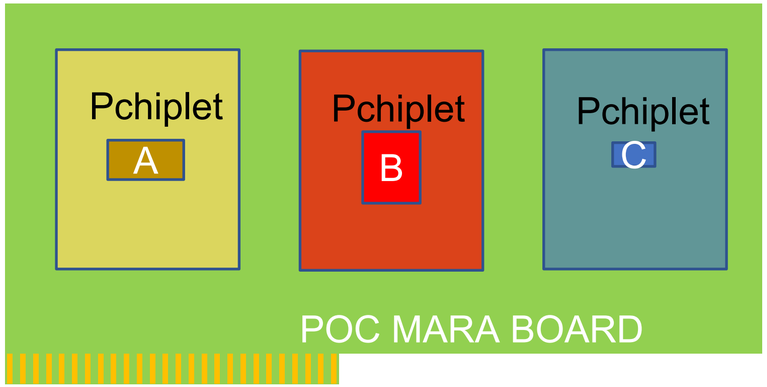
Pchiplet detects its slot



Pchiplet announces its slot to others

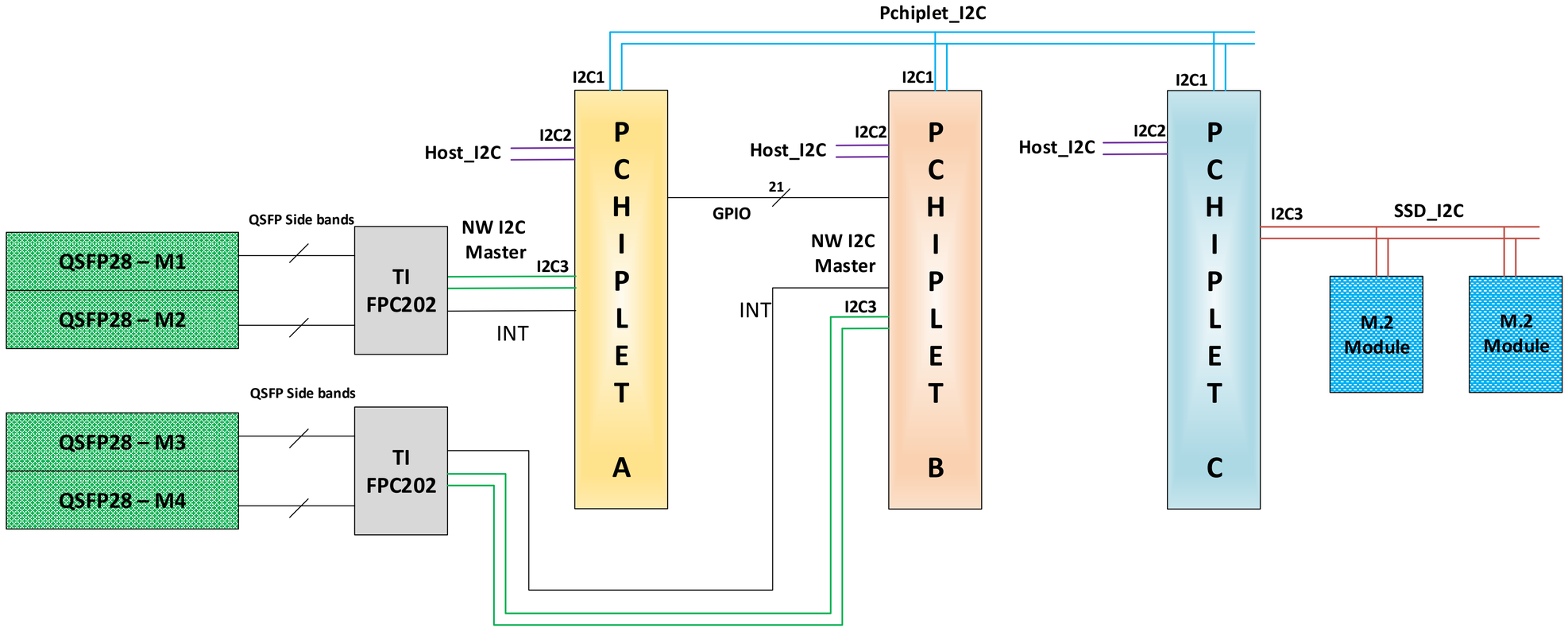
Baseboard Interconnect Architecture



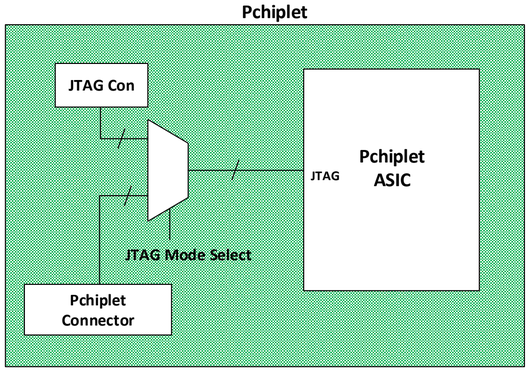


Inter-Pchiplet traces are capable of upto 100G signaling
With controlled impedances. Can support multiple HSIO signaling and clocking (PCIE, ETH, LVDS and BoW).
18 Layer EM891 Low Loss Dielectric

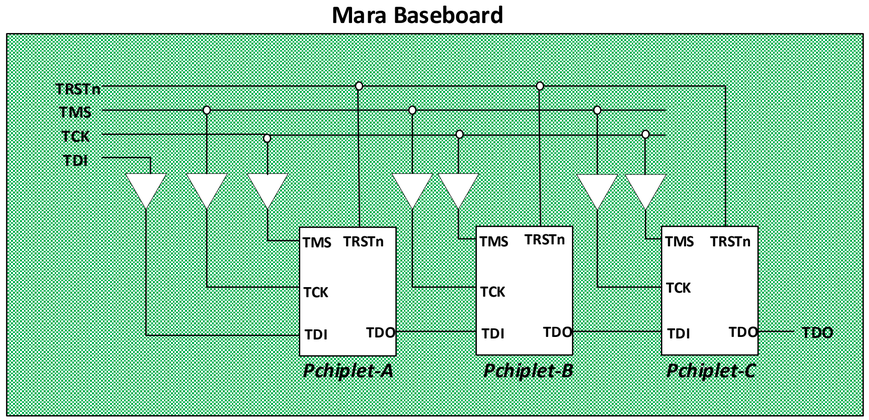
Baseboard Management



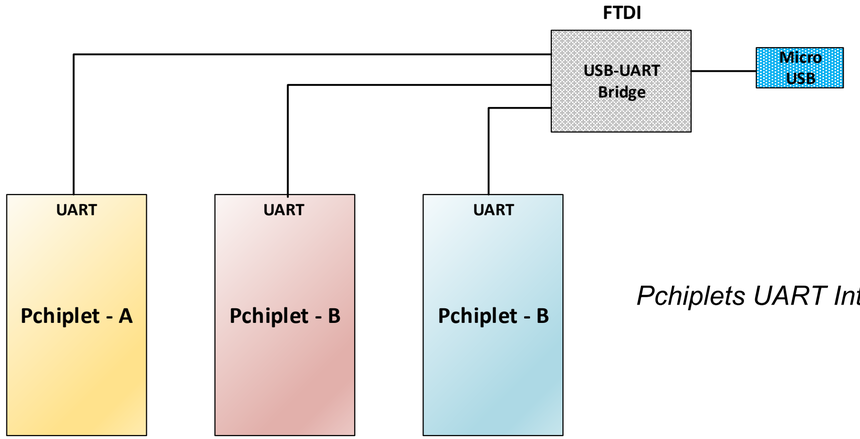
Test and Bring up Interfaces



JTAG for Pchiplet Bringup / debug

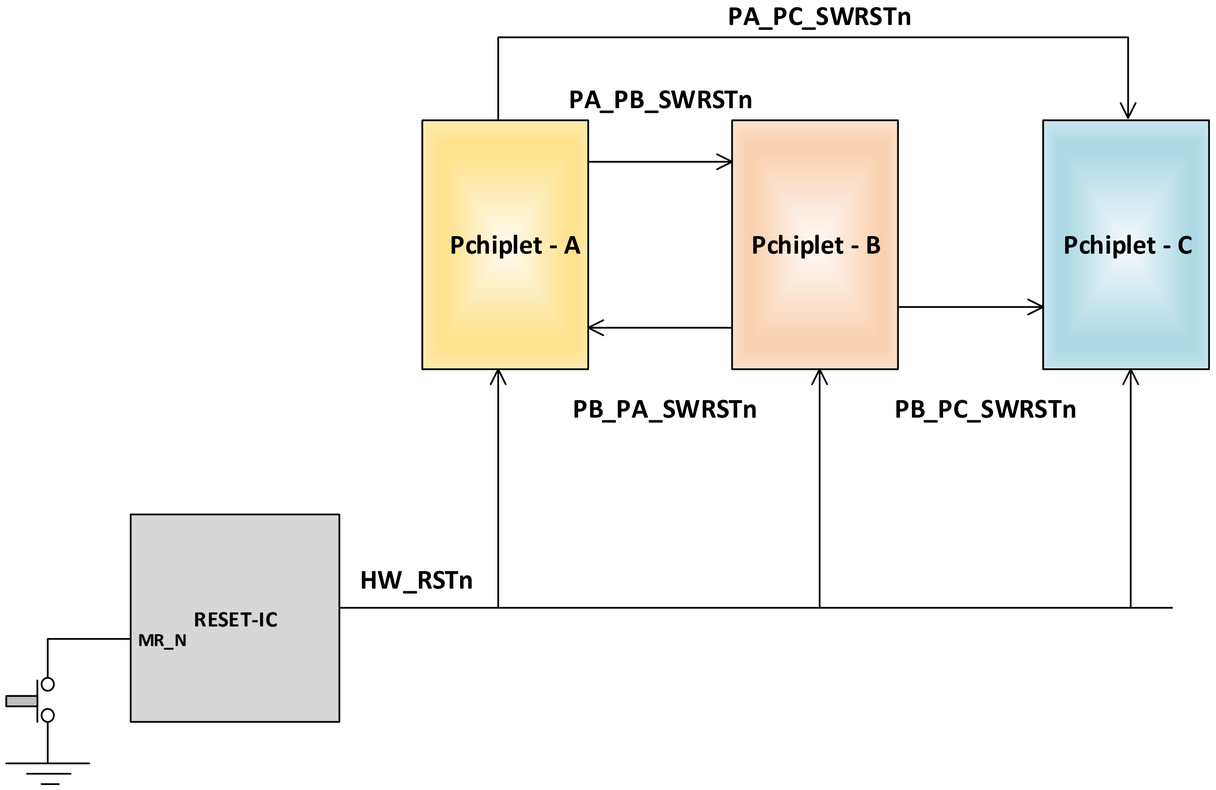


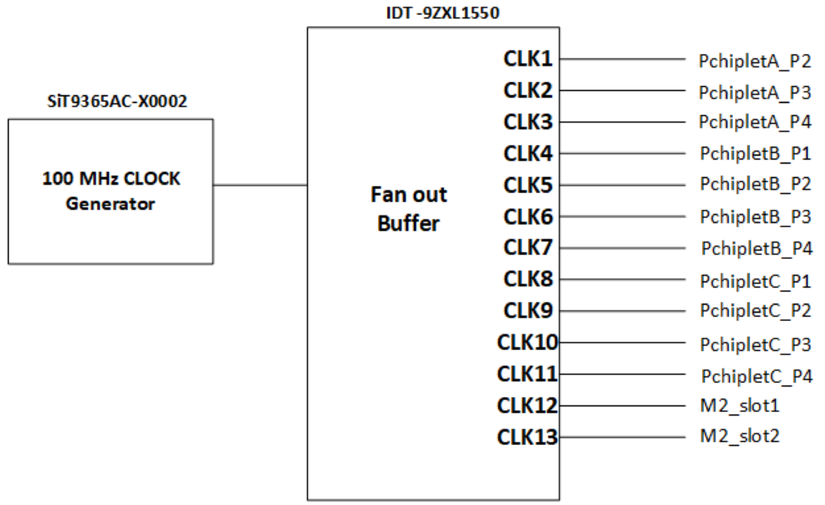
Daisy chained JTAG Interface for Pchiplet Boundary Scan



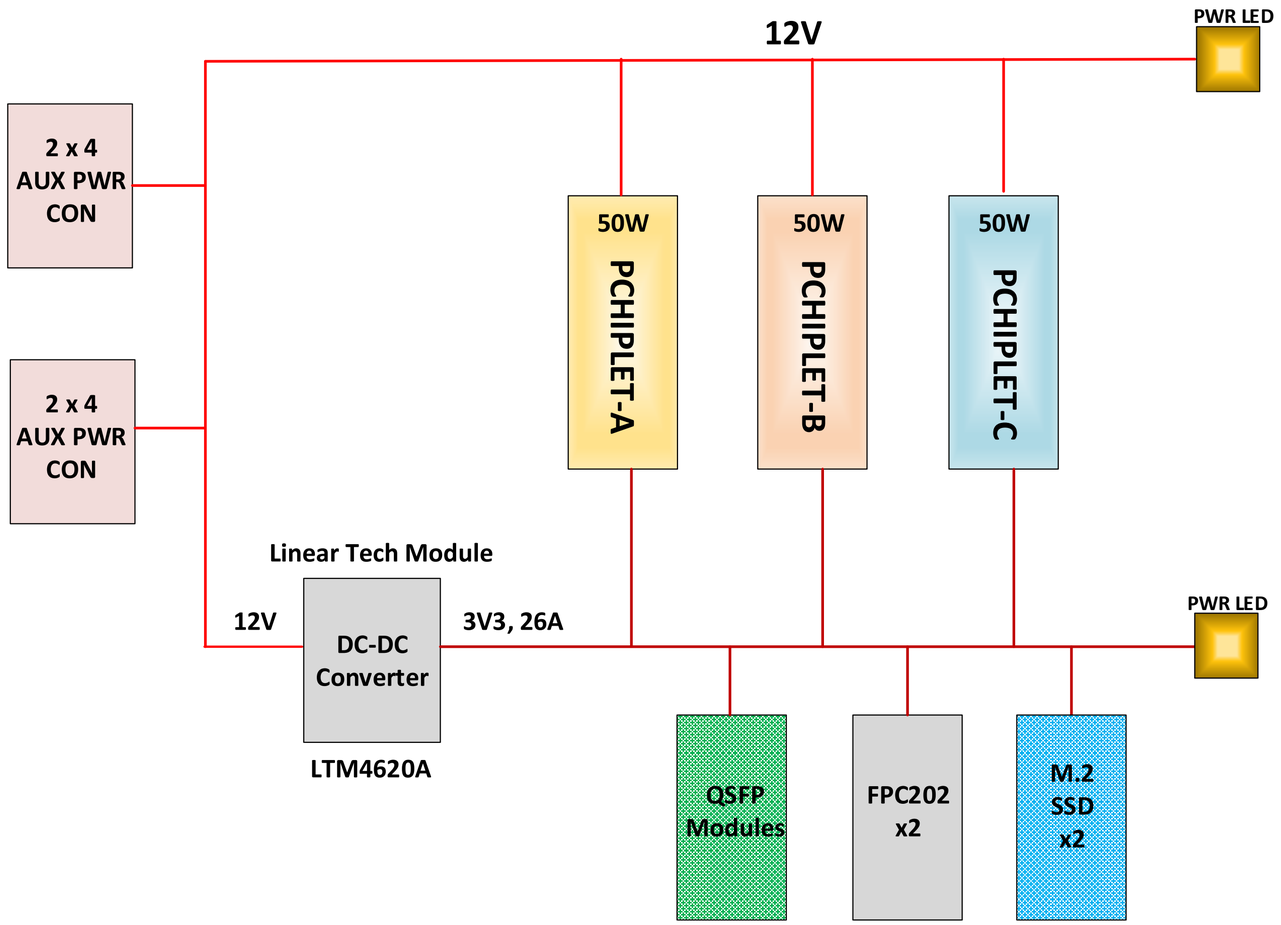
Pchiplets UART Interface for Pchiplet Bringup / debug

Reset and Clocking Scheme





Power Supply Scheme



Thank You