Community Led Hyperscale Open Innovation

Announcing a Proven SoC Disaggregation Interface Specification

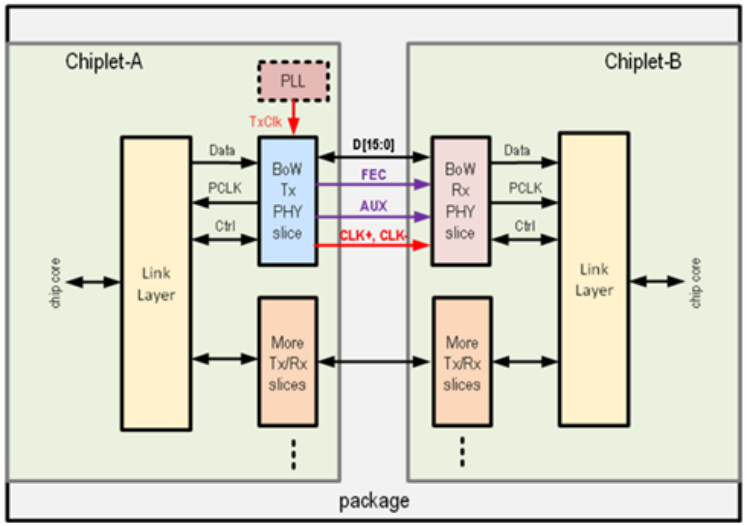
What is being Announced Today

- A New Open PHY Specification for SoC Disaggregation (BoW)
  - Optimized for both commodity (organic laminate) and advanced packaging technologies
  - Cost and energy efficient, high-performance across a wide range of process nodes
  - Authored to allow many use cases driving significant economies of scale
- Part of OCP ODSA Project's March Towards an Open Chiplet Ecosystem
  - Expands on OCP ODSA OpenHBI PHY targeting High Bandwidth Memory
  - Over 10 products are already being developed using BoW
  - Significant collateral (design guides, best practices) is freely available to the public
  - Open license available to anyone

Bunch of Wires (BoW): A Simple Parallel, Clock-forwarded PHY

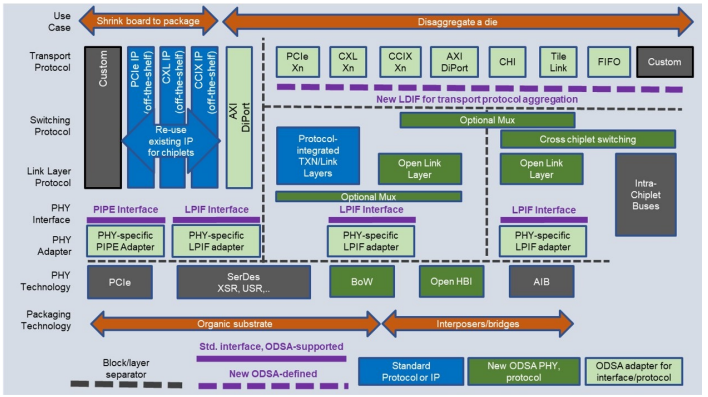
- Key Attributes for Economies of Scale
  - Cost and energy-efficient (0.25 -0.5pJ/bit)
  - High-performance (2-16Gb/s/line) across wide range of process nodes (65nm – 5nm)
  - Use cases (25mm reach, <1e-15 BER)
- Specification Optimized for Maximum Applicability
  - Minimalist approach to required features
  - Single logical unit (16 lane slice) applies to all package options
  - No direct requirements on channel loss or crosstalk, conformance based upon error rates
  - Specifies signal ordering at the Chiplet edge, rather than explicit bump maps

BoW block diagram



An ODSA Open Chiplet Ecosystem has already Formed

- Participation in ODSA includes Meta, Google, IBM, AMD, Xilinx, Samsung, Cisco, Keysight, Cadence and more.
  - Weekly calls average over 25 participants
- BoW Prototypes (5, 6, 12, 16, 22 and 65 nm process nodes)
  - NXP, Blue Cheetah Analog Design (BCA),
  - d-Matrix AI, eTopus
- Chiplet-based products (Networking, AI, FPGA, and Processors)
  - DreamBig, d-Matrix AI, Netronome, QuickLogic,
  - Ventana Microsystems



What is Next?

- Standardized, lightweight link layer definition suitable for low latency on-die buses such as AXI and CHI
- BoW-384 (24Gb/s/line) and BoW-512 (32Gb/s/line)
  - Support applications with critical bandwidth density requirements
  - Contain the degradation in energy-efficiency to <50% as compared to BoW-256.
- Scalability for rates of up to 64Gb/s/line (BoW-1024) is under evaluation
  - Provide improved energy-proportionality without sacrificing bandwidth density, control wire free idle/clock gating modes are being defined
- Additional features targeting improved yield, PHY footprint optimization, test, and security.
- Interoperability between BoW and other parallel D2D PHY standards

BoW Use Case Details

Sample BoW Use Case Presentations

- Blue Cheetah family of BoW-based D2D solutions
- eTopus/Quicklogic/Comira - BoW/FPGA/Ethernet I/O
- NXP BoW256 PHY development
- BoW PHY Interoperability Testing
- DreamBig BoW based Chiplet Platform for SmartNIC's
- Netronome Fourth Generation SmartNIC
- D-Matrix BoW D2D Interface for Multi-Chiplet AI System
- Ventana Micro Systems RISC-V CPU using BoW