Open. Together.
Open Domain-Specific Architecture

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ODSA: Open Domain-Specific Architecture

Domain-specific architecture: Programmable devices optimized for specific applications or class of applications. Meet the demands of high-intensity workloads in the data center and at the edge – e.g. machine learning, video processing.

Chiplets: Implement an integrated product as a collection of die in a single package, instead of a single die. Each die is a chiplet. Can reduce development and manufacturing costs.
The Open Domain-Specific Architecture

An open interface for inter-chiplet communication

Chiplets for accelerators:
- Shrink a board into a package
- Disaggregate a complex or large die
ODSA Goal: Chiplet Marketplace

ODSA Activities

OCP Use cases
ODSA Announcements at the Regional Summit

All activities involve broad and active participation from multiple members

OCP: Significant progress and growth in the ODSA

Avera: Releasing a 0.7 draft proposal for a Bunch of Wires (BoW) interface – at [https://www.opencompute.org/wiki/Server/ODSA](https://www.opencompute.org/wiki/Server/ODSA)

Achronix: A design for the proof-of-concept software development platform and a mock up (go see it)

zGlue: The formation of a workstream to specify chiplet physicals, the Chiplet Design eXchange
Our Session: The making of an Open Interface

DJ/FB: Why do we care about chiplets and accelerators
Steve/Achronix: How do we use chiplets – The PoC
Mark/Avera: How do we wire chiplets together – BoW
David/Intel: How do chiplets exchange bits – Link Layer
Jawad/zGlue: How do we describe chiplets - CDX
Wolfgang/Avera: How do package chiplets – Packaging
Panel (Thursday): How do we work together on chiplets?
Please Help! Join a Workstream

**Join the PoC, Build fast:** (Quinn Jacobson/Jawad Nasrullah/Jayaprakash Balachandran)

**Join Interface/Standards:** (Mark Kuemerle/Ramin Farjad/Robert Wang/David Kehlet)

**Join Business, IP and workflow:** (Sam Fuller/Dharmesh Jani)

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**Provide ODSA chiplets**

**Provide FPGA IP**

**Develop Packaging + Socket, Dev Board**

**Provide PHY Technology**

**Provide Chiplet IP**

Workstream contact information at the ODSA wiki
## Active Projects

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| PHY Analysis           | PHY requirements  
PHY analysis  
Cross-PHY abstraction (PIPE) | Alphawave, AnalogX, Aquantia, Avera Semi, Facebook, Intel, Kandou, Netronome, zGlue,         | PHY Analysis paper (published at Hot Interconnect)                                      | PIPE abstraction                                                      |                                                                     |
| BoW Interface          | No technology license fee, easy to port inter-chiplet interface spec       | Aquantia, Avera Semi, Netronome                                                              | BoW Interface proposal (published at Hot Interconnect)                        | BoW specification 0.7 End September, 2019                      | Test chips, Chiplet library supporting interface                   |
| Prototype              | product that integrates existing die from multiple companies into one package | Achronix, Cisco, Netronome, NXP, Samtec, Sarcina, zGlue, Macom, Facebook                   | Decomposable design flow.                                                       | Committed schedule                                               | End user End user participation ~30% funding is open                |
| Chiplet design exchange| Open chiplet physical description format.                                 | Ayar, NXP, zGlue,                                                                             | Draft spec                                                                  | ZEF Exchange format draft specification                         |                                                                     |
| Link and Network Layer | Interface and implementations – requirements and proposals                | Achronix, Avera Semi, Intel, Netronome, NXP, Xilinx                                          |                                                                               |                                                                     |                                                                     |
| Multi-chiplet test     | Test requirements for an open-chiplet interface                            |                                                                                              |                                                                               |                                                                     |                                                                     |
| Chiplet monitoring     | Monitoring infrastructure for chiplet operation                           |                                                                                              |                                                                               |                                                                     |                                                                     |
| Business workflow      | Formalize learnings from prototype effort                                |                                                                                              |                                                                               |                                                                     |                                                                     |

### Engineers from:
Achronix, AnalogX, ASE, Avera Semi, Ayar, Cisco, Facebook, Ferric, Intel, Kandou, Macom, Marvel, Netronome, NXP, On Semi, Samtec, Sarcina, Synopsys, Xilinx, zGlue
