Xilinx  Chip-to-chip Interface

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Xilinx Chip to Chip Interconnect History

> Multiple FPGA Dies Integration (Virtex-7 2000T)
  >> Four homogeneous 28nm FPGA Dies over Interposer
  >> 10000s of signals system-synchronous interconnect
  >> Announced: 2011

> Multiple FPGA & SerDes Chiplets (Virtex-7 H870T)
  >> Up to three FPGA and two 28G SerDes Chiplets
  >> 10000s of signals system-synchronous interconnect
  >> Announced: 2012

> Multiple FPGA & HBM Dies (Virtex US+ VU3xP)
  >> Up to three FPGA and two HBM2 Chiplets
  >> 10000s of signals system-synchronous interconnect
  >> 2x HBM2 DDR interconnect (~3500 interface signals)
  >> Announced: 2017
Chip-to-chip Interconnect echo-system Motivation

> Integration
  >> Dis-similar process technologies with high BW interface need
  >> Cost effective new class of solutions with higher BW between modules from different vendors
  >> Lower latency, lower power
  >> Smaller Form factor
  >> E.g., CPU $\leftrightarrow$ FPGA/GPU/ASIC and HBM;
     FPGA $\leftrightarrow$ HBM, Processor SoC, ASICs, Optical modules

> Disaggregation of Monolithic Die into Chiplets
  >> Different functions separated into modular chiplets for re-use
  >> Initially may be done in the context of one company design decision – still highly desirable to be based on interoperable eco-system driven standard
  >> 3rd Party chipset eco-system develops over time.
  >> E.g., FPGA $\leftrightarrow$ CPU & Domain-specific functions chiplets

Creating a broad adoption chip-let interface standard requires careful evaluation to avoid fragmentation
## Use Cases

<table>
<thead>
<tr>
<th>Eg. chip-lets</th>
<th>BW</th>
<th>Substrate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory dies</td>
<td>HBM</td>
<td>Interposer</td>
</tr>
<tr>
<td>Streaming interface</td>
<td>ADCs, optical modules</td>
<td>Organic or Interposer</td>
</tr>
<tr>
<td>Accelerators (including accelerators with bi-directional coherency)</td>
<td>Security, data base processing, HPC..</td>
<td>Organic</td>
</tr>
<tr>
<td>IO Devices</td>
<td>PIM; storage , NIC</td>
<td>Organic</td>
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</tbody>
</table>

Ideal to have minimum standard interfaces that can scale and provide *multiple solutions* creation from same central die.

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Standardization Effort Directions - PHY

> Serial
  >> XSR – 56G, 112G

> Parallel
  >> Expand use of HBM real-estate and design - HBM → HBI
  >> What is HBI?
    - Minimally enhanced HBM compatible Interface for chip-2-chip; HBM → HBI
      ▪ Interface definition from the perspective of signaling, clocking, voltage ranges, driver characteristics
      ▪ Move to lower voltage in next gen (HBM3 is 0.4v)
      ▪ Additional architected speeds
      Parallel interface is suitable for optimally carrying over both interposer and organic substrate
  >> Realization of HBI - HBI is realized in two ways
    - HBI-int (HBI over interposer) –
      ▪ Bump map – consistent with HBM bump-map
      ▪ Target freq spec
      ▪ ........
    - HBI-O (inter-operation of HBI-O with BoW for organic package)
      ▪ Bump map
      ▪ Terminate optionally
      ▪ Number of layers assumed for routing
      ▪ Target freq spec
      ▪ ........
Standardization Effort Directions - DataLink and Protocol

- Protocols – FIFO/PCIe/AXI/CCIX/CXL
- Datalink over Serdes
- Datalink over Parallel
- XSR(112, 56, ..)
- HBI-O ↔ BoW
- HBI-int

Pipe Interface

Organic

Interposer

Medium

Framing from protocol layer to data link layer

Direct attach or Pipe Interface
Summary

> Creating a broad adoption chiplet interface standard requires careful evaluation to avoid fragmentation

> Ideal to have minimum standard interfaces that can scale and provide *multiple solutions* creation from same central die

> Serdes interface – XSR/USR for medium to high performance

> Parallel- Low to medium performance based on C4 – establish **HBI-O** and its inter-operation with BoW
  >> Channel definition and IO analysis
  – Target frequencies
  – Max traces within two package layers for routing
  – Trace length
  >> Example C4 bump map for
  >> Power

> Parallel – high performance – can be over fine-pitch - HBI-int (HBI over interposer) as ODSA standard?

> Convergence on Datalink layer for serial and parallel
Chip-to-Chip Landscape