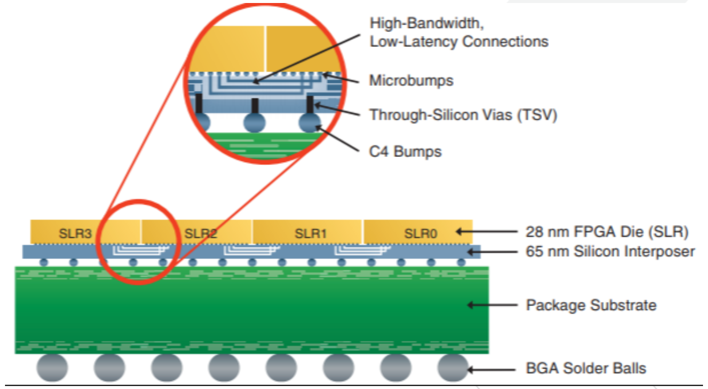
Xilinx Chip-to-chip Interface

Millind Mittal

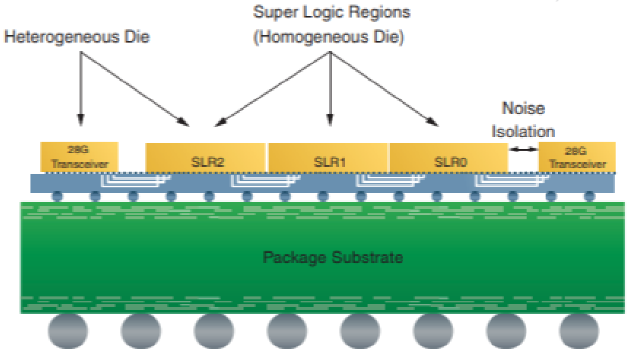
XILINX.

Xilinx Chip to Chip Interconnect History

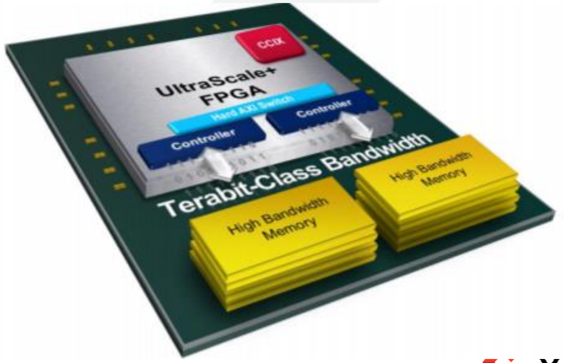
- Multiple FPGA Dies Integration (Virtex-7 2000T)
  - Four homogeneous 28nm FPGA Dies over Interposer
  - 10000s of signals system-synchronous interconnect
  - Announced: 2011



- **Multiple FPGA & SerDes Chiplets (Virtex-7 H870T)**
  - Up to three FPGA and two 28G SerDes Chiplets
  - 10000s of signals system-synchronous interconnect
  - Announced: 2012



- **Multiple FPGA & HBM Dies (Virtex US+ VU3xP)**
  - Up to three FPGA and two HBM2 Chiplets
  - 10000s of signals system-synchronous interconnect
  - 2x HBM2 DDR interconnect (~3500 interface signals)
  - Announced: 2017



Chip-to-chip Interconnect echo-system Motivation

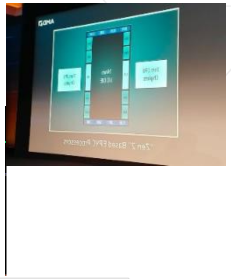
> Integration

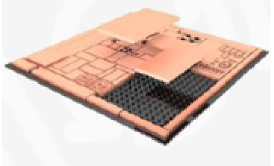
- Dis-similar process technologies with high BW interface need
- Cost effective new class of solutions with higher BW between modules from different vendors
- Lower latency, lower power
- Smaller Form factor
- E.g., CPU ←→FPGA/GPU/ASIC and HBM;
  FPGA ←→ HBM, Processor SoC, ASICs, Optical modules

> Disaggregation of Monolithic Die into Chiplets

- Different functions separated into modular chiplets for **re-use**
- Initially may be done in the context of one company design decision – still highly desirable to be based on interoperable eco-system driven standard
- 3rd Party chipset eco-system develops over time.
- E.g., FPGA ←→CPU & Domain-specific functions chiplets

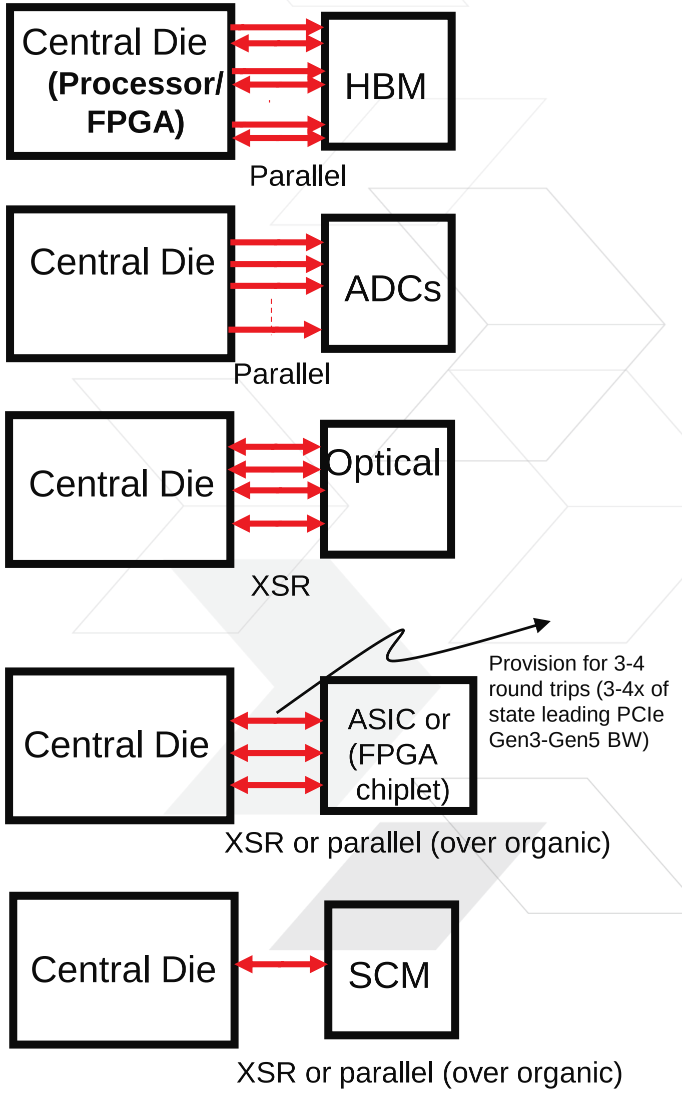
Creating a broad adoption chip-let interface standard requires careful evaluation to avoid fragmentation





Use Cases

	Eg. chip-lets	BW	Substrate
Memory dies	HBM	High (4Tb+/sec)	Interposer
Streaming interface	ADCs, optical modules	Medium to high BW (2-4Tb/sec)	Organic or Interposer
Accelerators (including accelerators with bi-directional coherency)	Security, data base processing, HPC..	Medium (0.5Gb/sec-2Tb/sec)	Organic
IO Devices	PIM; storage , NIC	Low to medium	Organic



Provision for 3-4 round trips (3-4x of state leading PCIe Gen3-Gen5 BW)

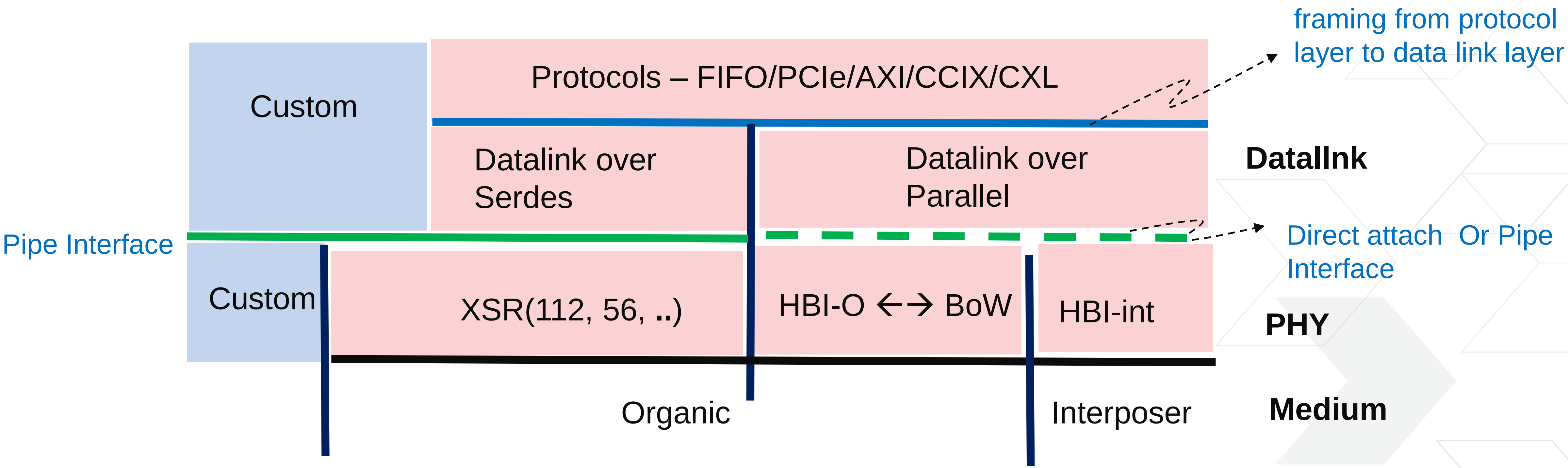
Ideal to have minimum standard interfaces that can scale and provide *multiple solutions* creation from same central die

Standardization Effort Directions- PHY

- Serial
  - XSR – 56G, 112G
- Parallel
  - **Expand use of HBM real-estate and design - HBM → HBI**
  - **What is HBI ?**
    - Minimally enhanced HBM compatible Interface for chip-2-chip ; **HBM → HBI**
      - Interface definition from the perspective of signaling, clocking, voltage ranges, driver characteristics
      - Move to lower voltage in next gen (HBM3 is 0.4v)
      - Additional architected speeds

      Parallel interface is suitable for optimally carrying over both inter-poser and organic substrate
  - **Realization of HBI - HBI is realized in two ways**
    - **HBI-int** (HBI over inter-poser) –
      - Bump map – consistent with HBM bump-map
      - Target freq spec
      - ……
    - **HBI-O** (inter-operation of HBI-O with BoW for organic package)
      - Bump map
      - Terminate optionally
      - Number of layers assumed for routing
      - Target freq spec
      - ……..

Standardization Effort Directions- DataLink and Protocol



Summary

- Creating a broad adoption chiplet interface standard requires careful evaluation to avoid fragmentation
- Ideal to have minimum standard interfaces that can scale and provide *multiple solutions* creation from same central die
- Serdes interface – XSR/USR for medium to high performance
- Parallel- Low to medium performance based on C4 – establish **HBI-O** and its inter-operation with BoW
  - Channel definition and IO analysis
    - Target frequencies
    - Max traces within two package layers for routing
    - Trace length
  - Example C4 bump map for
  - Power
- Parallel – high performance – can be over fine-pitch - HBI-int (HBI over interposer) as ODSA standard?
- Convergence on Datalink layer for serial and parallel

Chip-to-Chip Landscape

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