OPEN POSSIBILITIES.

OCP Server Delta Lake
OSF RAS Features
OCP Server Delta Lake OSF RAS Features

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OSF RAS Overview

• RAS - Reliability, Availability, Serviceability
  ○ Reliability - the ability of a system to protect data integrity and self correct
  ○ Availability - the resiliency of a computer system to stay operational
  ○ Serviceability - speedy recovery, repair and maintenance

• RAS consists of both hardware and software components
  ○ Dispersed across multiple areas of HW and SW
    ■ CPU, PCIE, DMI, memory
    ■ Firmware, ACPI tables, ACPI ASL, OS kernel, OS drivers

• RAS helps identify failures early
• RAS provides a structured mechanism of reporting errors to higher level SW
SW & HW Building Blocks

- CPU/MCA Banks
- PCIE
- Endpoints
- UPI/DMI
- coreboot
- ACPI Drivers/Tables
- OS/Kernel/Drivers
- Memory Controllers
- BMC

DIMMs

OPEN SYSTEM FIRMWARE
OSF RAS Feature Support

Memory
- Correctable, uncorrectable, patrol scrub, parity error
- No support for features that reduce memory capacity or system performance

CPU - IERR, MCERR
- No UPI support or multi-socket support (yet)

AER/PCIE/, DMI

ACPI/APEI - EINJ, HEST, & GHES (APEI)

Kconfig options
- Manage Firmware First or OS-1st error handling and reporting
- Error thresholds, error propagation, & corrupt data containment
- Error reporting to BMC and OS via UEFI CPER (common platform error record)

Many debug config options
OSF RAS Validation Status

- Test status: > 92% passing
- Passed Tests
  - All memory controllers and channels
    - Memory correctable
    - Memory uncorrectable non-fatal
    - Memory uncorrectable fatal
    - Patrol Scrub & parity errors
OSF Validation Status (con’t)

- Passed Tests
  - PCIE
    - Correctable, uncorrectable
    - All IIO stacks and endpoints
    - LER (link error recovery)
    - DMI
  - BMC
    - Logging of errors to BMC via SEL

- GAPS/Failures
  - BERT (Boot error record table), FSP error handling
  - IERR/MCERR - error injection is not functional
  - PCIE error issue during bootup with LER (deferred)
  - UPI support
OSF RAS Code Status

- Code base located mostly in src/soc/intel/xeon_sp folder
  
  https://github.com/coreboot/coreboot

- Support for Deltalake Mainboard
- Intel Xeon Processor CPX-6: 3rd Gen Intel Xeon Scalable
- Non-NDA code is already part of public repo
Call to Action

• Contribute to coreboot and LinuxBoot open source projects
• Please contact Wiwynn for purchasing Delta Lake
• Please contact 9elements Cyber Security for Delta Lake OSF feature development and professional support

OCP OSF Delta Lake:
https://github.com/opencomputeproject/OpenSystemFirmware/tree/master/Wiwynn/deltalake

Where to buy: https://www.wiwynn.com/contact-wiwynn/

9elements Cyber Security: https://9esec.io/contact

coreboot: https://coreboot.org/

LinuxBoot: https://www.linuxboot.org/

Thank you!
## RAS Code Layout

RAS Folder, ~14 C files, 4 header files, many hooks into other components

<table>
<thead>
<tr>
<th>MCA setup and init</th>
<th>SMM specific init</th>
<th>MCE handler</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uncore handler</td>
<td>Core handler</td>
<td>IIO/pcie handler</td>
</tr>
<tr>
<td>Access routines</td>
<td>Kconfig/Makefiles</td>
<td>IEH (integrated error hub)</td>
</tr>
<tr>
<td>Hest, GHES (acpi tables)</td>
<td>Elog (enhanced log)</td>
<td>EINJ</td>
</tr>
<tr>
<td>DMI</td>
<td>AER init</td>
<td>AER SMM</td>
</tr>
<tr>
<td>ACPI SCI</td>
<td>BMC error logging</td>
<td>UEFI/CPER</td>
</tr>
</tbody>
</table>
Memory CE/UCE Flow

Memory Controller

error

MCE

notify

Firmware

via ACPI

OS

Sys Log

I/O

BMC SEL