Modular Hardware System-Common Redundant Power Supply (M-CRPS) Base Specification

Part of the
Datacenter – Modular Hardware Systems (DC-MHS) Rev 1.0 Family

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Revision history

Date	Version	Description
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II.   Scope

The present specification defines all the requirements for an M-CRPS internal redundant power supply used in Open Compute Project that could be used in different environments like home/office, datacenter, and high-performance computing, hence harmonizing the server power supply requirements used in the industry with the purpose of creating a standard specification that the customers and vendors of Enterprise and Hyperscale can use for their products.

Any supplier seeking OCP recognition for a hardware product based on this specification must be 100% compliant with any and all features or requirements described in this specification.

1   Overview

The Modular Hardware System Common Redundant Power Supply (M-CRPS) Base Specification addresses multiple form factors that includes 185mm by 73.5mm (Length x width), 185mm by 60mm, and 265mm by 73.5mm all of them in 1U height and having different input connector types and voltage ranges like 240VAC/240VDC, 277VAC/380VDC, +54VDC for rack input power using a bus bar connector, and a -48VDC input for the Telecom industry. All the variations of the M-CRPS share the same electrical output interface.

Given the necessity of having some differentiation in the industry, the M-CRPS Base Specification can accommodate the preferences of different OEMs by choosing details like:

- LED blinking pattern
- latch finger grip color and design.
- Label artwork
- FRU content
- Packaging options

Along with the aforementioned customizations the M-CRPS introduces a new concept of Configuration File described in *Section 12.8*, with this feature the OEM can change the default configuration of most of the thresholds in the power supply and some of its signal timings as well as a new serial interface called Data & Sideband Serialization Interface (DSSI) described in *Section 12.8.3.11* with the purpose of be utilized as an I/O expander providing flexibility for the side-band signals of the M-CRPS, thus avoiding the need of changing the output connector in the future.

2   Mechanical Overview

The physical sizes of the power supply enclosures are defined below. The power supply shall contain a fan for self-cooling. The power supply has a card edge output that interfaces with a high-power card edge

connector in the system. The AC/DC plugs directly into the external face of the power supply. Refer to the following subsections for details.

2.1   Form Factor Outline

There are three main form factors addressed by this specification, they differ in width both sharing the same length and height: 185x73.5x40mm (LxWxH) and 185x60x40mm (LxWxH), and a third one having the following dimensions 265x73.5x40mm (LxWxH). *Figure 2-1* shows the 3D models of the three main form factors.
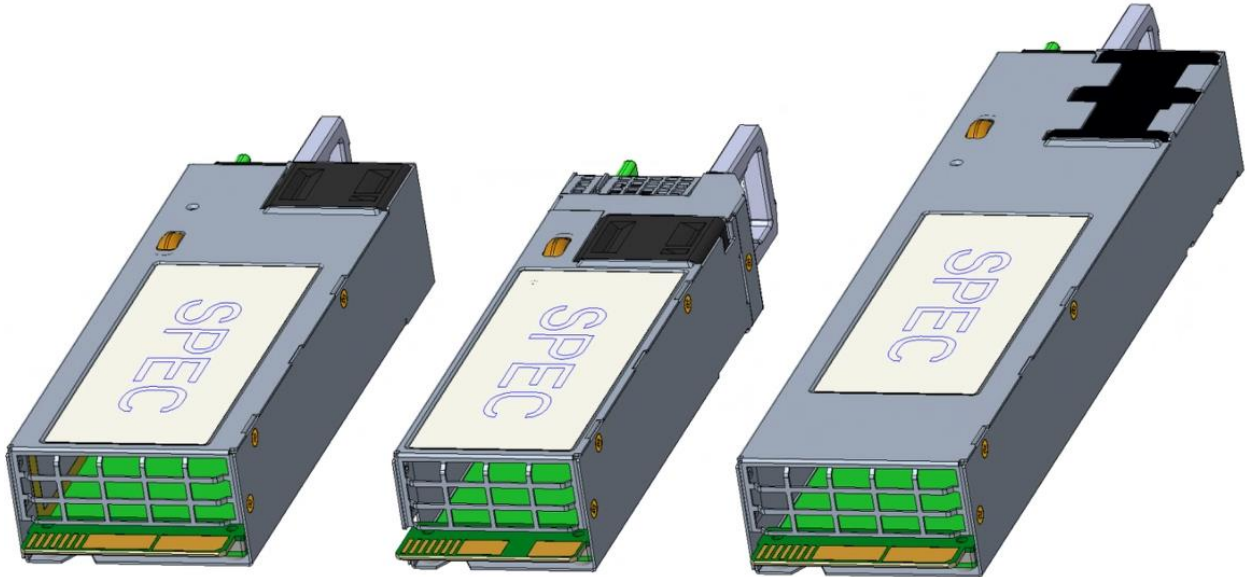
Figure 2-1 Form factors side by side (Front view), from left to right: 185mm by 73.5mm, 185mm by 60mm and 265mm by 73.5mm.

2.1.1   185mm by 73.5mm Form Factor

Figure 2-2 shows the outline for the 185mm by 73.5mm M-CRPS form factor, the power supply can support single or dual rotor fan depending on the application; single rotor fan is shown in the figure.
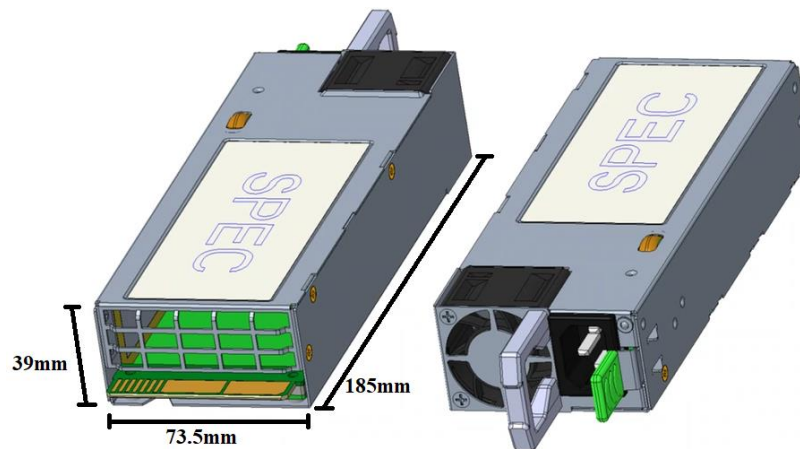
Figure 2-2 185mm by 73.5mm in width form factor outline

Note: Height of the power supply is 40mm in the fan area and 39mm on the rest of the case, for more details see *Supplemental Material A*

2.1.1.1   240VAC/240VDC Input

Figure 2-3 shows a front/rear isometric view of the 185mm by 73.5mm form factor using the C14 inlet connector. Same representation applies for the 265mm by 73.5mm form factor.
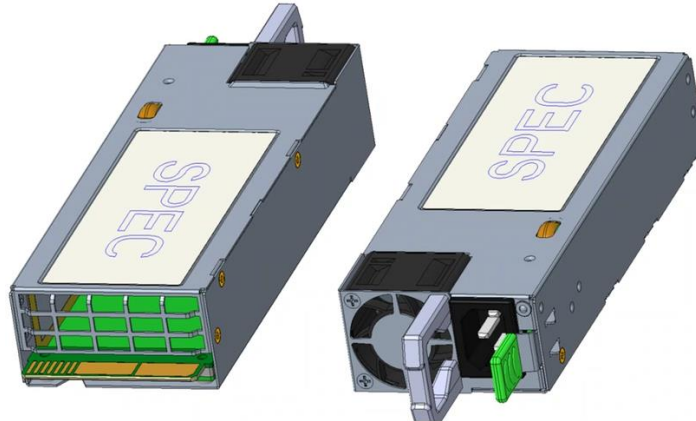
Figure 2-3 185mm by 73.5mm form factor with IEC320-C14 inlet connector as example

2.1.1.2   277VAC/380VDC Input

Figure 2-4 shows a front/rear isometric view of the 185mm by 73.5mm form factor using the TBD inlet connector. Same representation applies for the 265mm by 73.5mm form factor.

Figure 2-4 185mm by 73.5mm form factor with 277VAC/380VDC inlet connector

2.1.1.3   +54VDC Input (Rack Power Input)

Figure 2-5 shows a front/rear isometric view of the 185mm by 73.5mm form factor using the TBD bus bar clip connector. Same representation applies for the 265mm by 73.5mm form factor.

Figure 2-5 185mm by 73.5mm form factor with bus bar connector input

2.1.1.4   -48VDC Input (Telecom)

Figure 2-6 shows a front/rear isometric view of the 185mm by 73.5mm form factor using the TBD -48VDC Telecom inlet connector. Same representation applies for the 265mm by 73.5mm form factor.

-48VDC Input M-CRPS
isometric image

Figure 2-6 185mm by 73.5mm form factor with -48VDC input connector

2.1.2   185mm by 60mm Form Factor

Figure 2-7 shows the outline for the 185mm by 60mm M-CRPS form factor, the power supply shall support single rotor fan.

39mm

185mm
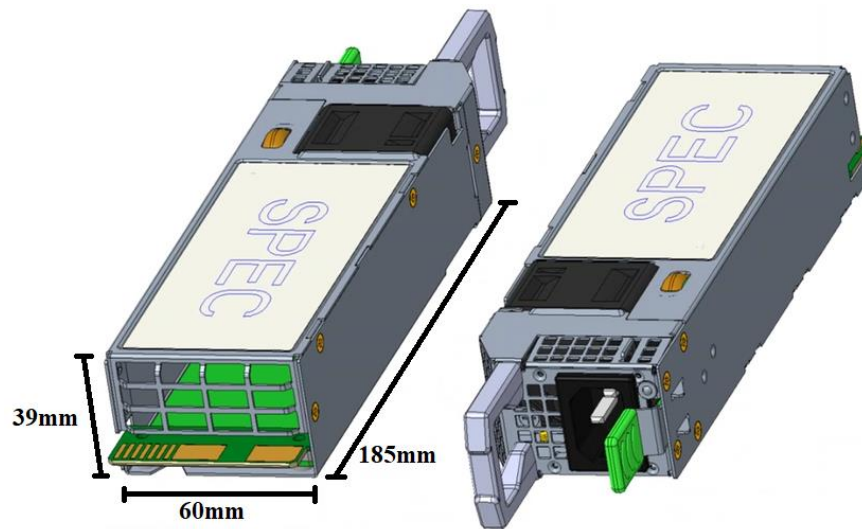
60mm

Figure 2-7 60mm in Width form factor outline

> **Note:** Height of the power supply is 40mm in the fan area and 39mm on the rest of the case, for more details see *Supplemental Material B*

2.1.2.1   240VAC/240VDC Input

Figure 2-8 shows a front/rear isometric view of the 185mm by 60mm form factor using the C14 inlet connector.
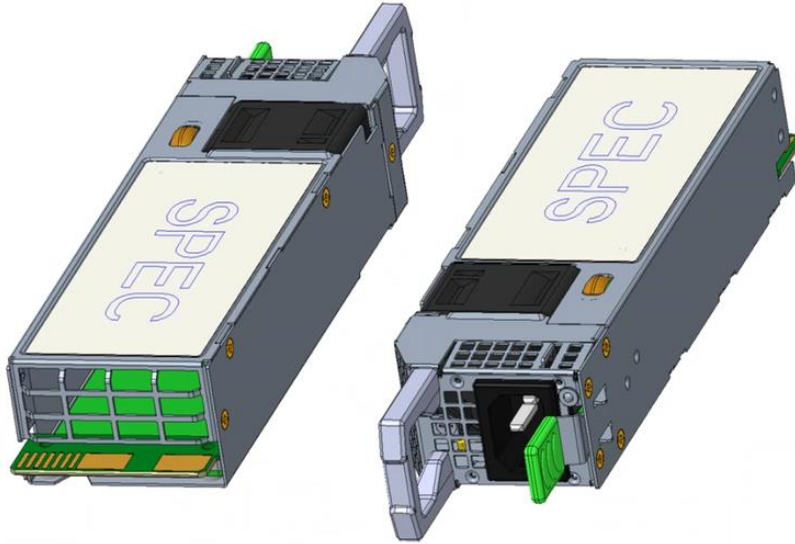
Figure 2-8 185mm by 60mm form factor with IEC320-C14 inlet connector as example

2.1.2.2   277VAC/380VDC Input

Figure 2-9 shows a front/rear isometric view of the 185mm by 60mm form factor using the TBD inlet connector.

277VAC/380VDC Input M-CRPS isometric image

Figure 2-9 185mm by 60mm form factor with 277VAC/380VDC inlet connector

2.1.2.3   +54VDC Input (Rack Power Input)

Figure 2-10 shows a front/rear isometric view of the 185mm by 60mm form factor using the TBD bus bar clip connector.

+54VDC Input M-CRPS isometric image

Figure 2-10 185mm by 60mm form factor with bus bar connector input

2.1.2.4   -48VDC Input (Telecom)

Figure 2-11 shows a front/rear isometric view of the 185mm by 60mm form factor using the TBD -48VDC Telecom inlet connector.

Figure 2-11 60mm form factor with -48VDC input connector

2.2 Handle and Retention Latch

The power supply shall have a fixed water-clear polycarbonate illuminated handle to assist insertion and extraction, *Figure 2-13* shows the 3D representation of the handle. The operator shall be able to insert and extract the power supply without the assistance of tools. The power supply shall have a latch which retains the power supply into the system and prevents the power supply from being inserted or extracted from the system when the AC/DC power cord is inserted into the power supply. The handle shall protect the operator from any burn hazard. The finger grip color and shape can be customized.
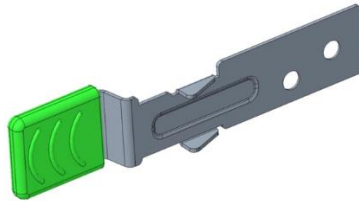
Figure 2-12 Retention latch example

Note: For details about the dimensions of the latch and finger grip options see *Supplemental Material G, Supplemental Material H,* and *Supplemental Material I.*
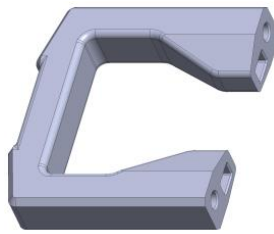
Figure 2-13 M-CRPS illuminated handle

Note: For details about the dimensions please see *Supplemental Material F.*

2.3 LED Marking and Identification

The power supply shall use a bicolor LED, Green & Amber. Below table shows the LED states for each power supply operating state and the LED's wavelength characteristics.

Table 2-1 LED Characteristics

	Nominal λd Wavelength	Units
Green	515	nm
Amber	590	nm

Notes:

2. Amber LED should be biased with a forward current (If) - 18mA ± 2 mA.
3. Green LED should be biased with a forward current (If) - 8mA ± 2 mA.
4. An example bicolor LED that meets these requirements is TBD.

The handle shall be illuminated by LEDs mounted on a flex PCB in the rear that terminates to the control board in the front of the power supply as shown in *Figure 2-14* below.
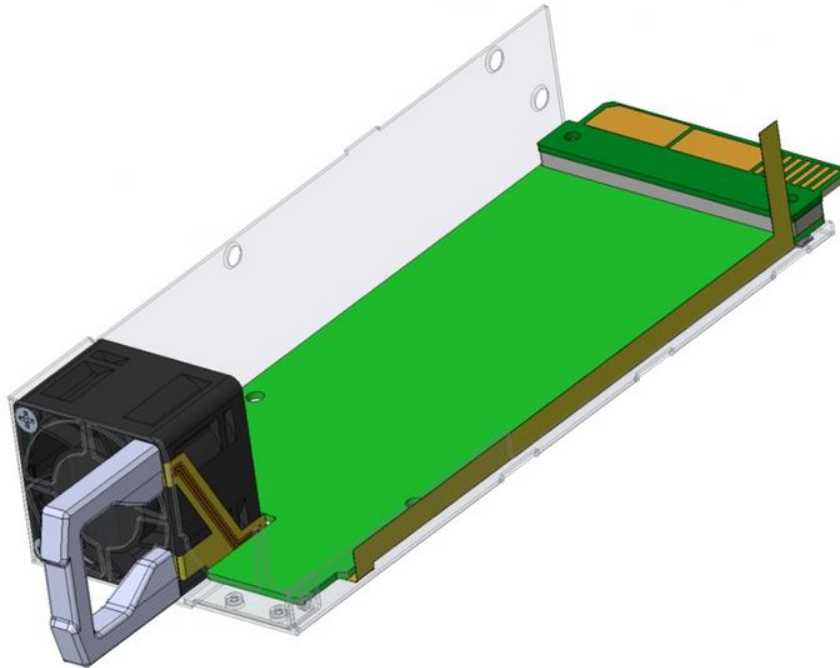
Figure 2-14 Flex PCB with LEDs installed in a 185mm by 73.5mm form factor as example

Two sets of two LEDs (four LEDs total) shall be located at the end of the flex PCB as shown in *Figure 2-15* below; two (green and amber) at the top bifurcation and two (green and amber) at the bottom bifurcation.
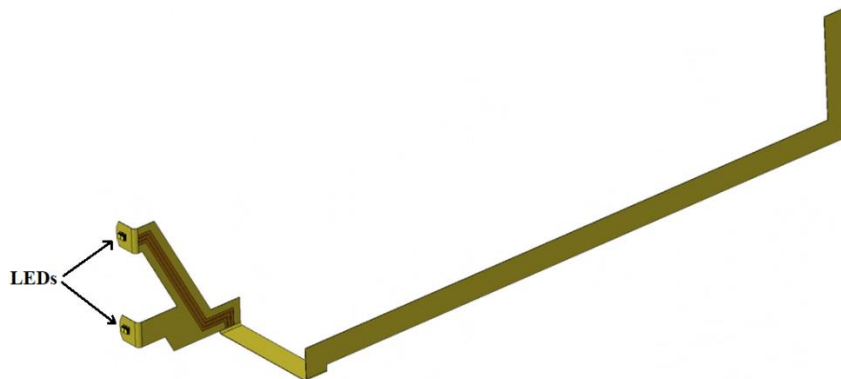
Figure 2-15 Flex PCB 3D representation showing the location of the LEDs

> **Note:** The same flex PCB could be leveraged for the fan power and signals connection to have a cleaner solution.

The LEDs shall be controlled by Firmware to easily change blink rates and colors for the different states using update to the PSU secondary side Firmware's configuration file as defined in *Section 12.8.3.1 LED Behavior Configuration Block*. This allow the M-CRPS to be reprogrammed to match different customer's LED state requirements.

2.4   Inlet Connector

The power supply can have different inlet connectors depending on the input voltages, current rating and type of connection that could be directly interfacing with a bus bar in a rack or through a power cord.

2.4.1   240VAC/240VDC Input

To comply with international regulations IEC320-C14 inlet connector shall be used when a maximum of 10 Amperes is required by the power supply. IEC320-C16 can be used to support higher exhaust temperatures in the power supply at 10 Amperes. A picture of the IEC320-C14 inlet connector is shown in the figure below.

Figure 2-16 IEC320 C14 Inlet connector example

To comply with international regulations IEC320-C20 inlet connector shall be used when a maximum of 16 Amperes is required by the power. Additionally, IEC320-C22 can be used to support higher exhaust temperatures in the power supply at 16 Amperes.

Figure 2-17 IEC320-C20 Inlet connector example

2.4.2   277VAC/380VDC Input

For 277VAC/380VDC input the inlet connector is TBD.

Figure 2-18 277VAC/380VDC inlet connector

2.4.3   +54VDC Input (Rack Power Input)

A bus bar type connector shall be used when using a direct bus bar connection for the input of the power supply to interface with +54VDC rack power delivery, the connector shall be properly sized for the required input current of the power supply. An example of this type of connector is shown in the following figure.

Figure 2-19 Bus bar connector example

2.4.4   -48VDC Input (Telecom)
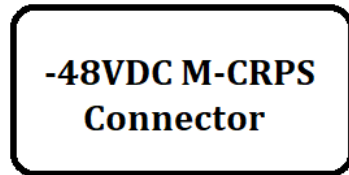
Figure 2-20 -48VDC inlet connector example (Telecom)

2.5   Label Outline and Artwork

All the supported power supply form factors shall have a space of 115x52mm for the label, an example of the label artwork is shown in the figure below. Refer to specific OEM artwork and drawing for more details about the required information like company name, addresses, etc.
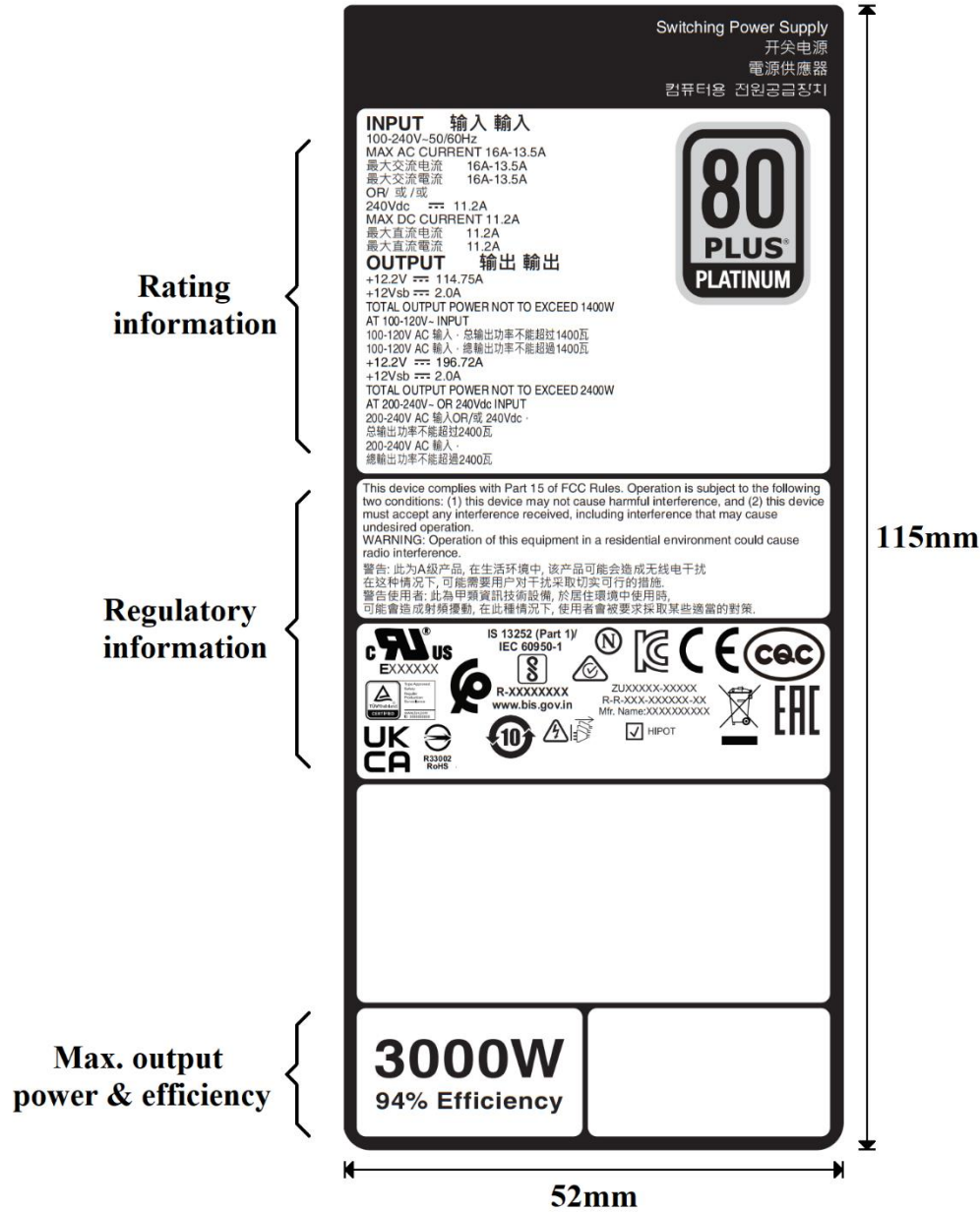
Figure 2-21 PSU Label artwork example

2.6   Output Connector Interface

The output connector interface for the form 185mm by 73.5 and the 185mm by 60mm factors include the same amount of signal and power connections, the difference in the 185mm by 60mm form factor is the reduced contact area of the Ground and Power connections. *Figure 2-22* shows 3D representations of the two different card edge interfaces, mechanical details are shown in *Supplemental Material D* for the 185mm by 73.5mm form factor and *Supplemental Material E* for the 185mm by 60mm form factor.
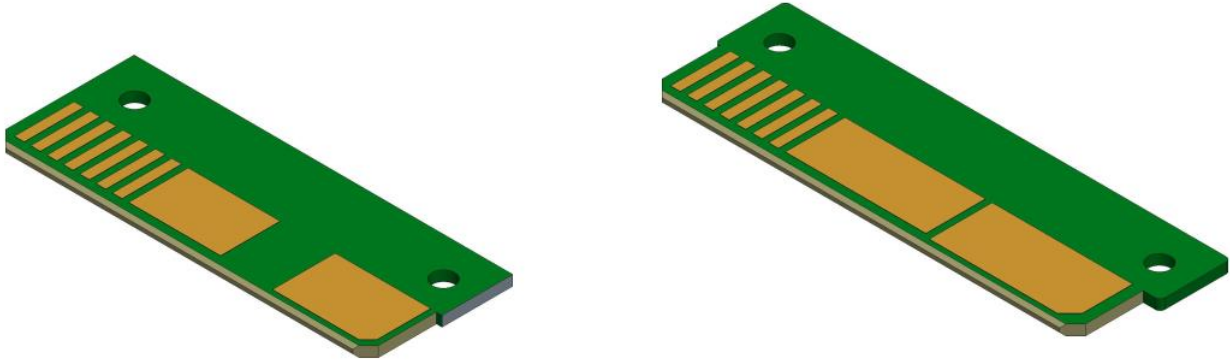
Figure 2-22 185mm by 60mm card edge (left), 185mm by 73.5mm card edge (right)

2.6.1   185mm by 73.5mm Form Factor

Table 2-2 185mm/265mm by 73.5mm M-CRPS dimensions and receptacle connector

Dimensions	M-CRPS-185-73.5: 40mm x 73.5mm x 185mm (H x W x L)
Output connector	Please refer to connector vendors or Document TBD for more information.

Power supply front view

B25 (S14)   A25 (S7)

B1 (P7)   A1 (P1)
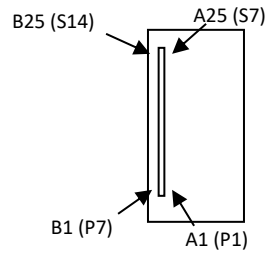
Figure 2-23 185mm/265mm by 73.5mm Power supply's output pin numbering

Note: Pin numbering is shown based on listed connectors in *Table 2-2*.

The power supply card edge pinout for the 73.5mm in width PSU form factor is defined in the below table.

Table 2-3 73.5mm in with PSU pinout definition

Name	High pwr conn[2]	Regular conn[1]	Regular conn[1]	High pwr conn[2]	Name
GND		A1	B1		GND
GND	P1	A2	B2	P7	GND
GND		A3	B3		GND
GND		A4	B4		GND
GND	P2	A5	B5	P8	GND
GND		A6	B6		GND
GND		A7	B7		GND
GND	P3	A8	B8	P9	GND
GND		A9	B9		GND
+12V	P4	A10	B10	P10	+12V

+12V		A11	B11		+12V
+12V		A12	B12		+12V
+12V		A13	B13		+12V
+12V	P5	A14	B14	P11	+12V
+12V		A15	B15		+12V
+12V		A16	B16		+12V
+12V	P6	A17	B17	P12	+12V
+12V		A18	B18		+12V
PMBus SDA	S1	A19	B19	S8	A0 (SMBus address)[5]
PMBus SCL	S2	A20	B20	S9	A1 (SMBus address)[4]
PSON#	S3	A21	B21	S10	+12VSB
SMBAlert#	S4	A22	B22	S11	Cold Redundancy Bus
Return Sense / PS_KILL	S5	A23	B23	S12	12V load share bus
+12V Remote sense	S6	A24	B24	S13	Imon[3]
PWOK	S7	A25	B25	S14	VINOK

Notes:
1. Regular 50-pin card edge connector *Table 2-2*.
2. High power connector listed in *Table 2-2.*
3. *Imon* output signal current information based on 12V main output's loading condition, please see details in *Section 9.5 Imon Output Signal (Output)*.
4. A1 pin shall support bi-directional serialization mechanism described in *Section 12.7 Data & Sideband Serialization Interface (DSSI)*.
5. A0 pin shall be connected to an ADC input in the secondary side MCU to support up to 6 SMBus addresses, levels are described in *Section 9.6.1 A0 Input Addressing*.

2.6.2 185mm by 60mm Form Factor

Table 2-4 185mm by 60mm M-CRPS dimensions and receptacle connector

Dimensions	M-CRPS-185-60: 40mm x 60mm x 185mm (H x W x L)
Output connector	Please refer to connector vendors or Document TBD for more information.

Power supply front view
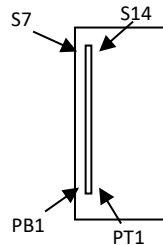
Figure 2-24 185mm by 60mm Power supply's output pin numbering

Note: Pin numbering is shown based on listed connectors in *Table 2-4*.

The power supply card edge pinout for the 60mm in width PSU form factor is defined in the below table.

Table 2-5 60mm in with PSU pinout definition

Name	Conn. pin	Conn. pin	Name
GND			GND
GND	PT1	PB1	GND
GND			GND
GND			GND
GND	PT2	PB2	GND
GND			GND
Empty (no connection)			Empty (no connection)
Empty (no connection)	PT3	PB3	Empty (no connection)
Empty (no connection)			Empty (no connection)
+12V			+12V
+12V	PT4	PB4	+12V
+12V			+12V
+12V			+12V
+12V	PT5	PB5	+12V
+12V			+12V
PMBus SDA	S8	S1	A0 (SMBus address)[3]
PMBus SCL	S9	S2	A1 (SMBus address)[2]
PSON#	S10	S3	+12VSB
SMBAlert#	S11	S4	Cold Redundancy Bus
Return Sense / PS_KILL	S12	S5	12V load share bus
+12V Remote sense	S13	S6	Imon[1]
PWOK	S14	S7	VINOK

Notes:
1. *Imon* output signal current information based on 12V main output's loading condition, please see details in *Section 9.5 Imon Output Signal (Output)*.
2. A1 pin shall support bi-directional serialization mechanism described in *Section 12.7 Data & Sideband Serialization Interface (DSSI)*.
3. A0 pin shall be connected to an ADC input in the secondary side MCU to support up to 6 SMBus addresses, levels are described in *Section 9.6.1 A0 Input Addressing*.

3   Thermal Requirements

The following subsections describe the power supply thermal test conditions. The power supply is intended to be installed in a system in which the power supply will support limited operation up to an inlet temperature of 70⁰C during loss of redundancy conditions, however the typical maximum operating ambient power supply's inlet temperature is 55⁰C.

3.1 Temperature and Altitude Conditions

Table 3-1 Power supply thermal test conditions

PSU configuration	Load on a power supply	AC/DC input	Temp / Altitude combination	Texit Max
1+0	100% Max load	Min nominal to Max nominal	50^oC / $2286m^6$ 55^oC / $2286m^6$	70^oC 75^oC
1+1	60% max load	Min nominal to Max nominal	55^oC / $2286m^6$ 60^oC / $2286m^6$	70^oC 75^oC
1+0	100% max load	Min nominal to Max nominal	70^oC / $2286m^6$	90^oC^1
2+0	Max load	Min nominal to Max nominal	50^oC / $2286m^6$ 55^oC / $2286m^6$	70^oC 75^oC
2+2	70% max load	Min nominal to Max nominal	55^oC / $2286m^6$ 60^oC / $2286m^6$	70^oC 75^oC
2+0	100% max load	Min nominal to Max nominal	70^oC / $2286m^6$	90^oC^1
3+0	Max load	Min nominal to Max nominal	50^oC / $2286m^6$ 55^oC / $2286m^6$	70^oC 75^oC
3+3	70% max load	Min nominal to Max nominal	55^oC / $2286m^6$ 60^oC / $2286m^6$	70^oC 75^oC
3+0	100% max load	Min nominal to Max nominal	70^oC / $2286m^6$	90^oC^1

Notes:

1. This condition shall be supported only once in the life of the power supply for 24 hours straight, and the temperature limit for the components will be based on their maximum Tj -10^oC. To support this condition the PSU will need to have a mylar coating in all the metal parts in the rear part of the chassis. Over Temperature Warning and Over Temperature Protection shall be disabled in the configuration file to support this condition.
2. All the conditions shall be supported assuming 0 in H2O of back pressure.
3. For PCBs with SMD power components, the maximum operating temperature shall be kept below Tg -10^oC, for example an FR4 material with a Tg = 130^oC shall be kept below 120^oC.
4. 20C air temperature rise is allowed for 100% load from the inlet to the exhaust of the power supply, and 15C air temperature rise is allowed for 70% load.
5. SMBAlert# shall not assert under any of the operating conditions stated in the above table unless configured in the configuration file.
6. A maximum of 3000m might be required for some models of power supplies, this requirement shall be stated in the design specification of a given model.

The power supply shall operate within all specified limits over the full environmental range. All airflow shall pass through the power supply and not over the exterior surfaces of the power supply.

In situations when the system cannot maintain the required maximum power supply inlet temperature, it is acceptable and expected that the power supply assert SMBAlert# based in the configured threshold due

to inlet temperature and throttle the processors and memory to maintain power supply cooling and attempt to prevent power supply shutdown due to over temperature. System level throttling under these conditions is acceptable.

The max load on the power supply may vary based on input voltage. The max load stated in *Section 7.1 Output Power/Currents* shall be used when testing at lower input voltages.

Power supply shall meet the thermal requirements under the load and environmental condition identified in each table. Even though the table addresses only the exhaust air temperature, all other components in the power supply shall also meet their temperature specifications and lifetime requirements.

The power supply must meet UL enclosure requirements for temperature rise limits. All sides of the power supply with exception to the air exhaust side must be classified as "Handle, knobs, grips, etc. held for short periods of time only".

3.2   Airflow Impedance

The power supply shall be capable of supplying the airflow that is sufficient for self-cooling when installed in different system airflow impedances. The power supply shall be characterized using the following figures in this section for airflow impedance and fan PWM respectively. Airflow as function of inlet temperature is characterized for the one or multiple internal critical components (bulk capacitor, primary core transformer) inside PSU which are thermocouple instrumented such that temperature is tracked as function of a sweep of airflow, such plot is generated from highest power load to the minimum operational percentage. As shown in *Figure 3-1 Airflow requirement for thermal compliance for inlet temperature for different PSU loads*, the server designer has the means to determine the effective airflow must move to maintain safe internal temperatures.
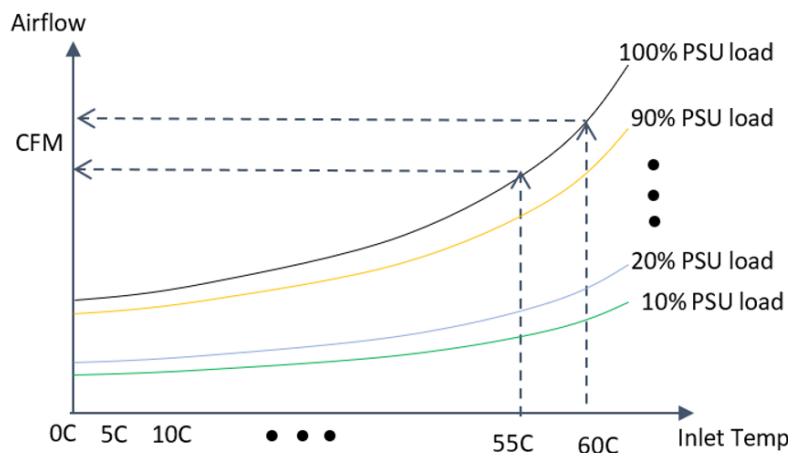
Figure 3-1 Airflow requirement for thermal compliance for inlet temperature for different PSU loads

Power supply vendor shall complete the table below with the corresponding data collected from the test conducted to generate the previous *Figure 3-1 Airflow requirement for thermal compliance for inlet temperature for different PSU loads.*

Table 3-2 Airflow requirement for thermal compliance for inlet temperature at different PSU load conditions

PSU Load	10%		20%		30%		40%		50%		60%		70%		80%		90%		100%	
PSU Tla	CFM	PWM	CFM	PWM	CFM	PWM	CFM	PWM	CFM	PWM	CFM	PWM	CFM	PWM	CFM	PWM	CFM	PWM	CFM	PWM
60 ºC																				
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5 ºC																				
0 ºC																				

The airflow that PSU moves is known through a simple free air wind tunnel characterization, but that is incomplete PSU characterization as such airflow is affected by each server design and condition in which own server system fans move air and generate back pressure toward power supply, either positive and therefore helping to move higher CFM through PSU or in some instances a negative back pressure fighting against the effort of the own PSU fan reducing its overall airflow. Complete characterization of a power supply shall consist of 3 tests, impedance of PSU without fan in place, fan performance curve and the effective M-CRPS performance curve as shown in *Figure 3-2 Power supply airflow impedance, fan curve and equivalent performance curve (Example from a real* test). Tests shall be performed at sea level conditions (test facilities at elevated environment shall perform altitude correction projections).
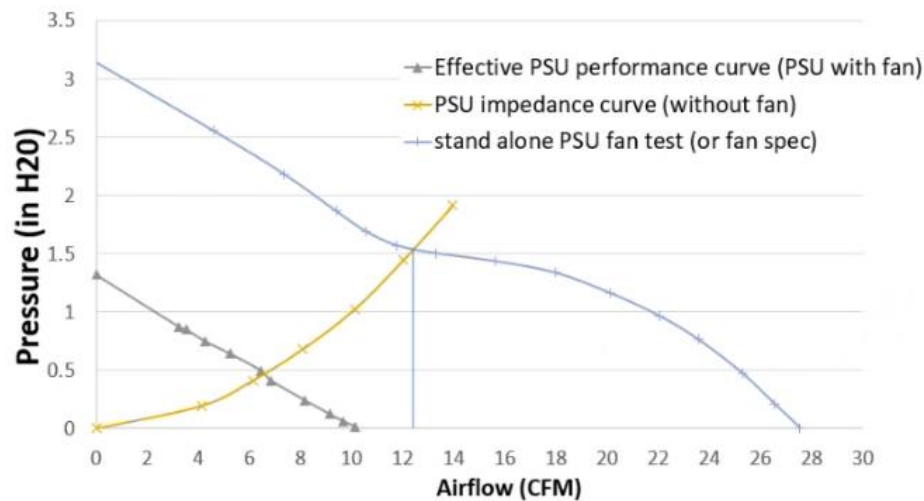
Figure 3-2 Power supply airflow impedance, fan curve and equivalent performance curve (Example from a real test)

Power supply vendor shall complete the table below with the corresponding data collected from the test conducted to generate the previous *Figure 3-2 Power supply airflow impedance, fan curve and equivalent performance curve* (Example from a real test)*.*

Table 3-3 Power supply airflow impedance, fan curve and equivalent performance curve

Airflow (CFM)	PSU without fan Pressure (in H_2O)	Stand-alone fan Pressure (in H_2O)	PSU with fan Pressure (in H_2O)
0			
2			
4			
6			
8			
10			
12			
14			
16			
18			
20			

Notes:
1. Maximum CFMs in the previous table shall be based on the maximum airflow for the stand-alone fan specification.

In addition, the power supply's fan shall be characterized to create the *Figure 3-3 Power supply fan PWM characterization (example only)* below and complete table.
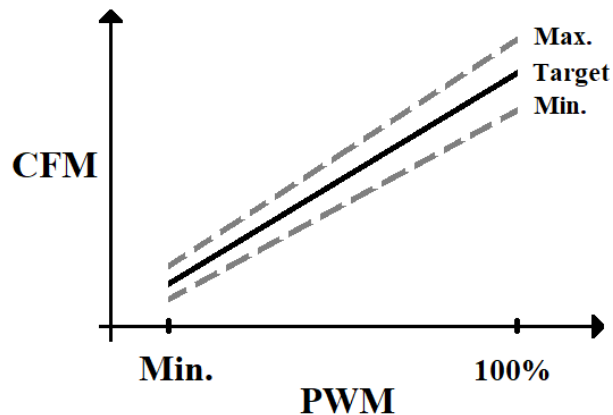
Figure 3-3 Power supply fan PWM characterization (example only)

Table 3-4 Power supply fan PWM characterization

PWM Duty cycle (%)[1]	Airflow (CFM)
10%	
20%	
30%	
40%	
50%	
60%	
70%	
80%	
90%	
100%	

Notes:
1. Minimum PWM duty cycle shall be taken from the specific fan being used in the power supply (either 10% or 20% PWM duty cycle).

3.3   Minimal Fan Speed

In some system applications, there is a possibility that the airflow through the PSU will reverse direction and lead to components exceeding their thermal limits. To prevent this reverse airflow condition, the PSU must support the PMBus command to boost the PSU fan speed. System will communicate the minimal fan speed to the PSU via the FAN_COMMAND_1 (3Bh) PMBus command. This sets the PSU minimum fan speed to guarantee positive airflow direction through the PSU.

The power supply shall be able to accept and execute the FAN_COMMAND_1 (3Bh) while in standby or when the input voltage is not present, for this mode of operation the PSU shall bias its internal fan from the main output when it is available or from the standby rail when the power supply is in standby mode. Writing 0000h to the FAN_COMMAND_1 (3Bh) shall stop the fan operation in standby operation as well as ON state. The connection between fan VCC and +12Vmain output of the power supply shall include necessary isolation and protection circuit as shown in the figure below.
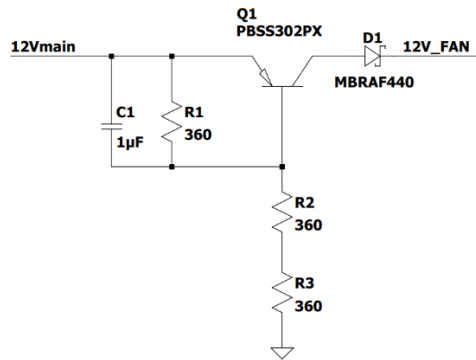
Figure 3-4 Fan power isolation circuit example

3.4   Fan Speed Control

The power supply shall incorporate a fan for cooling the power supply. The airflow direction shall be from the card edge connector side to the AC/DC inlet side of the power supply for a regular airflow power supply and from the AC/DC inlet side to the card edge connector side for reversed airflow power supplies.

The Fan speed control shall have close loop algorithm based on both the critical component temperature and the ambient temperature (Inlet temperature). Thus, ensuring the PSU fan will always ramp to maximum speed under any condition to protect the power supply from overheating. These conditions include high ambient temperatures, loading, voltage input, and airflow impedance.

Under any steady state operating condition (steady state power output level and steady state inlet air temperature), fan oscillation shall be controlled such that associated sound power level variation falls within a band of 2.0 dBA (roughly 10% mean speed). This condition may be treated as steady state fan speed condition.

The fan is allowed to run in Standby mode as necessary to cool the PSU when the ambient temperature exceeds 35C. In Standby mode, the power supply shall allow to override the fan speed through the PMBus command.

The PSU shall detect a warning or fault on the PSU fan and report over the PMBus and shall be able to be configurable for a difference between the Fan Speed Control (FSC) setpoint and the actual fan speed reading in RPM and the warning/fault timing. A fan fault is defined as fan RPM being less than a configurable difference in RPM between FSC setpoint and the actual fan speed during normal operation or during standby operation with ambient temperature exceeding 35°C. If the difference of the FSC setpoint and the measured fan speed is bigger than a configurable value in RPM within 5 seconds, the "Fan X Warning" should be asserted. If the difference of the FSC setpoint and the measured fan speed is bigger than a configurable value in RPM within 15 seconds, the Fan X fault should be asserted immediately. The PSU main rail (+12V) shall also shutdown when in Normal operation. This fan fault shutdown mechanism shall be activated within 15 seconds after the power supply outputs are first turned-on. This will allow sufficient time for the fan to come up to speed and the fan detect circuitry to stabilize. If the Fan fault or obstruction is removed when PSU is still in STANDBY mode, then the fan/ should be able to recover or latch OFF depending on the selected configuration. Optionally the PSU can be configured to try to restart the fan to see if fault is cleared, and if the fault is cleared, STANDBY becomes operational (subject to input being within operational range and there is no other fault in the PSU which could cause STANDBY to shutdown).
When there is a fan fault, no safety issue should occur due to the lack of airflow.

The fan curve or fan speed control will be defined in terms of a fan RPM idle and fan RPM maximum. The loading conditions for those RPM values will be defined as idle fan loading and maximum fan loading which are percentages of the rated load (worst case loading in terms of output power) of the power supply at the defined idle fan control temperature and maximum fan control temperature in degrees C.

After the new load and/or cooling condition steady state is established, transition to the steady state fan speed shall take place within 60 seconds.

The power supply airflow shall fall to the range of minimum of TBD CFMs and maximum of TBD CFMs for 20% and 100% PWM to maintain even airflow between two or more power supplies during parallel operation.

3.4.1 Clamped Fan Speed Control Algorithm

The power supply shall use a PID controller as fan speed control algorithm using the structure shown in *Figure 2-1.* The parameters for the PID controller are shown in *Table 3-5 PID controller parameters* below.

Table 3-5 PID controller parameters

Name	Description
Input Name	Label global clamp sensor
Input Sensor Input	Add sensor(s) list
FFGainCoefficient	Feedforward coefficient setting parameter
FFOffCoefficient	Feedforward coefficient setting parameter
PCoefficient	Proportional coefficient
ICoefficient	Integral coefficient

ILimitMax	Integral maximum value limit
IlimitMin	Integral minimum value limit
OutlimitMax	Maximum sensor limit
OutlimitMin	Minimum sensor limit
NegativeHysteresis	
PositiveHysteresis	
SlewNeg	Negative rate of change
SlewPos	Positive rate of change
Setpoint	Temperature control target
Zones	Add the zone(s) the sensor will be driving fan speed

Notes:

1. LSB and MSB need to be added for the second integral gain coefficient and LSB: MSB need to be added for the derivative.
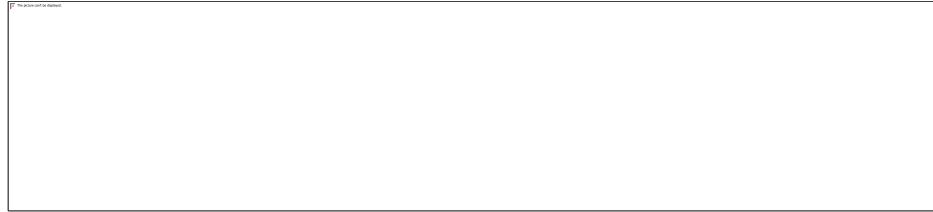
Figure 3-5 Simplified diagram for the Fan Speed Control Clamped Algorithm
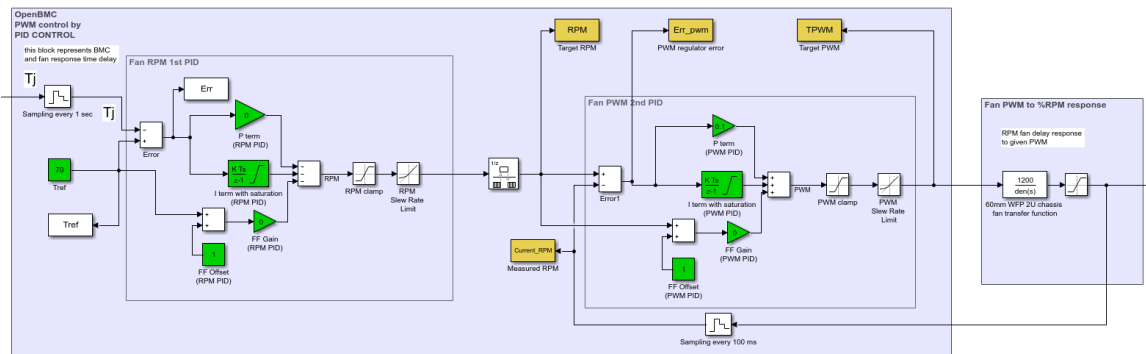
Figure 3-6 Detailed diagram for the implementation of the Clamped Fan Speed Control Algorithm

Notes:

1. The clamped algorithms cannot drive the fan speed outside the bounds of the lower and upper clipping curves defined for any sensor.
2. All power supplies shall have a minimum of 4 sensors, which includes the inlet air and exhaust air sensors.
3. For power supplies with output power rating beyond 2000W a total 6 sensors is preferred.

3.5 Thermal Sensors

The PSU shall have thermal sensors to measure inlet temperature, exhaust temperature, and two hot spot component temperatures. These shall be used for asserting over temperature warning condition (OTW), over temperature protection/shutdown (OTP), reporting temperatures via PMBus, and for controlling the fan speed.

Thermal sensors accuracy shall be within +/-1°C.

Inlet ambient temperature sensors OTW and OTP levels are defined in *Section 8.1.8 Over Temperature Warning (OCW) & Section 8.1.9 Over Temperature Protection (OTP).*

Both the hotspot thermal sensor(s) and the ambient inlet thermal sensor shall have both OTW level and OTP level associated with them. The OTW level must be set at least 4°C lower than the OTP level to guarantee a warning condition is reported to the system before a shutdown condition.

- OTW: Over temperature warning level associated with all thermal sensors. This asserts the SMBAlert# signal and does not shutdown the PSU. This also asserts the associated PMBus STATUS warning bits. This supports the CLST (Closed Loop System Throttling) feature. Internal fan speed control algorithm shall ramp up the fan speed to the maximum prior to the SMBAlert insertion.
- OTP: Over temperature protection level associated with all thermal sensors. This shutsdown the PSU to protect any components from exceeding their maximum temperature. This also asserts the associate PMBus STATUS bits.

3.6 Power Supply Fan

The fan shall use either a Hall IC (in addition to hall sensor) OR should have an internal circuit & / or FW for noise immunity. Additionally, the fan shall be certified by any accredited lab for IEC61000-4-3 (radiated Magnetic Immunity) & IEC61000-4-8 (Power Frequency Magnetic Field Immunity).

4 Acoustics and Vibration Requirements

4.1 Acoustic Requirements

Each PSU offering shall meet a set of acoustical limits and reporting requirements to be compliant with this specification. Information about the acoustical noise of power supplies is useful to manufacturers of data center equipment for the purposes of product design and to compare power supplies developed under this standard.

Several methods need to be developed and leveraged to report or compare against a pre-defined limit:
- Measurement method
  ECMA-74 is leveraged to provide a uniform and certifiable standard for measurement of sound power and sound pressure data used in this specification. This standard defines unique bystander microphone locations and has additional requirements for the measurement of fan speed.
- Limit development
  Limits applied to acoustical metrics are agreed upon by the participating members of the M-CRPS working group within OCP. Data center IT equipment has a wide breadth of application spaces and environments; this specification seeks to define a subset of physical deployment environments to set limits on sound power and sound quality of a given PSU.
- Presentation of declared acoustical data
  Although methods for reporting sound power and sound pressure data are well described by ECMA-74 and ECMA-109, this standard defines a unique set of reporting requirements for various operating conditions and acoustic metrics.

4.1.1   General, Laboratory, and Sampling Requirements

Acoustical measurements shall be performed in a NVLAP, or equivalent, certified laboratory qualified to measure and report in accordance with ECMA-74. The test environment should provide an essentially free field over a reflecting plane. Per EMCA 74 clause 7.3.1.1, criteria for suitable test environments are defined in ISO 3744 and ISO 3745.

Samples to be evaluated for acoustical compliance with this specification shall be randomly selected from a larger batch manufactured for qualification. At least three power supply samples for each qualified fan make and model qualified in the design shall be tested to comply with this specification.   For example, if two fan models are to be qualified for use, 6 total power supplies shall be sampled from a qualification batch, three for each of the fan models.

4.1.2   Test Environment

The test environment and meteorological conditions shall meet the requirements of ECMA-74 clause 7.

4.1.3   Instrumentation

Microphones shall meet the instrumentation requirements of ECMA-74 clause 7 for sound power measurements and ECMA-74 Clause 8 for sound pressure and sound quality measurements.

A sound power array meeting the qualifications of ISO 3744 or ISO 3745 shall be used for measuring sound power. Two additional microphones shall be used to measure sound pressure and for the purposes of evaluating sound quality. The location of these microphones is documented in *Section 4.1.5 Microphone Positions.*

In addition to microphones for measuring acoustical data, fan speed should also be measured and recorded simultaneously.   For simplicity across acoustical and vibration testing, recording the fan tachometer signal directly is recommended to record fan speed. An optical tachometer may be used for acoustical testing; however, optical tape may negatively impact fan vibration measurements, and thus should be removed for vibration tests. NOTE: fan speed measurement is still required for vibration testing. The optical tachometer shall not be positioned to interfere with acoustic transmission between the fan and the bystander microphone.

For some constant fan speed tests, described in *Section 4.1.5 Microphone Positions*, a resistive load is required to be applied to an energized PSU to evaluate electronic noise. The load shall not be a DC electronic load or any load that itself produces noise.

4.1.4   Installation and Operation of the Power Supply

PSU should be installed in the test environment in accordance with sub-assembly requirements per ECMA-74 clause 5.1.7. The PSU shall be supported 0.25 m ± 0.03 m above the reflecting plane by a vibration isolating stand or fixture, or by appropriate vibration-isolating elements. The method of supporting the sub-assembly shall not interfere with the propagation of airborne sound from the sub-assembly or generate any additional sound radiation. Vibration isolation elements should be placed on the bottom of the PSU at each of the four corners of the device; rubber isolators approximately 20mm in diameter and 12mm in height are recommended.

For tests which specify operation of the fan, the fan shall be manually controlled through the PSU firmware or directly with wires to a power supply and function generator. In these cases, the fan should not be controlled with a closed loop fan control algorithm.

4.1.5   Microphone Positions

For sound power measurement, the measurement surface and microphone positions shall follow ECMA-74 clause 7.6.

For sound pressure measurement, two microphones, defined as front and rear operator microphones shall be installed. The operator positions shall be at a horizontal distance of 0.5 m ± 0.03 m from the front and rear sides of the reference box, as defined in ECMA-74 clause 7.6.1, at a vertical height of 0.25 m ± 0.03 m. For the purposes of this acoustical measurement, the front and rear of the PSU are defined in *Figure 4-1 Front and rear surface definition for PSU bystander microphone position*. PSU setup with operator microphone positions are shown in *Figure 4-2 PSU installation and operator microphone position locations [side view]* in accordance with ECMA-74 Clause 5.1.7.Operator microphones located downstream of the fan shall have a windscreen placed on the microphone to prevent wind noise.

Microphone orientation shall follow requirements in ECMA-74 clause 8.6.4.
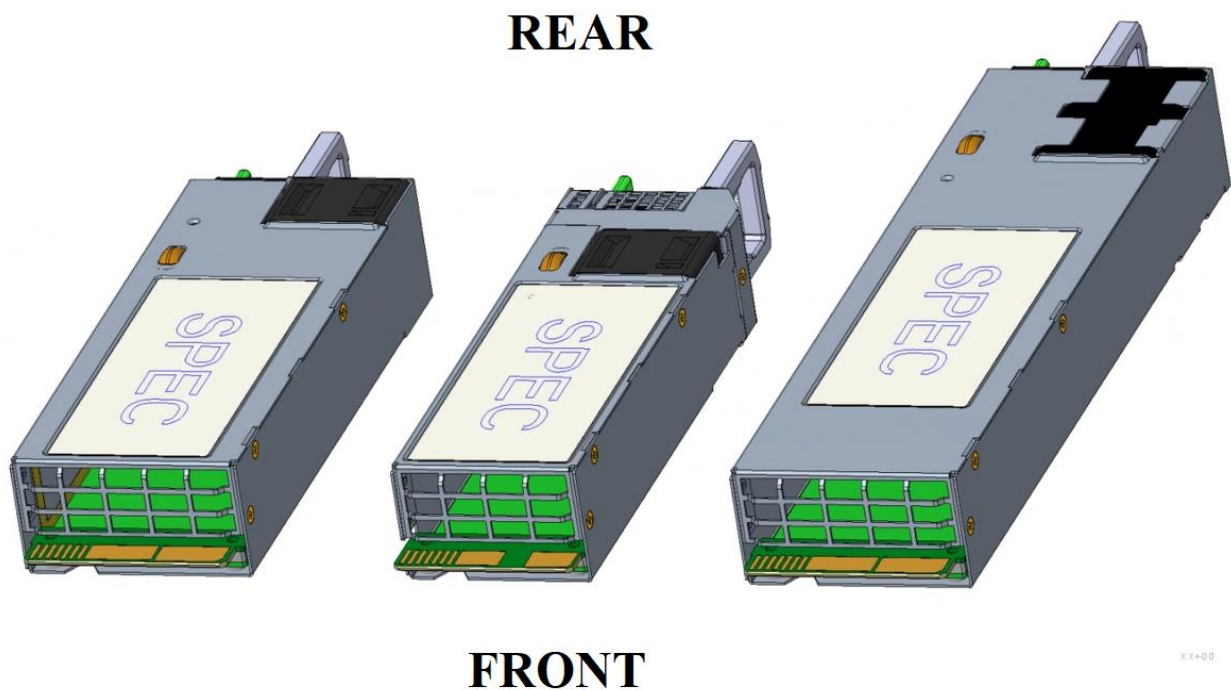
Figure 4-1 Front and rear surface definition for PSU bystander microphone position.
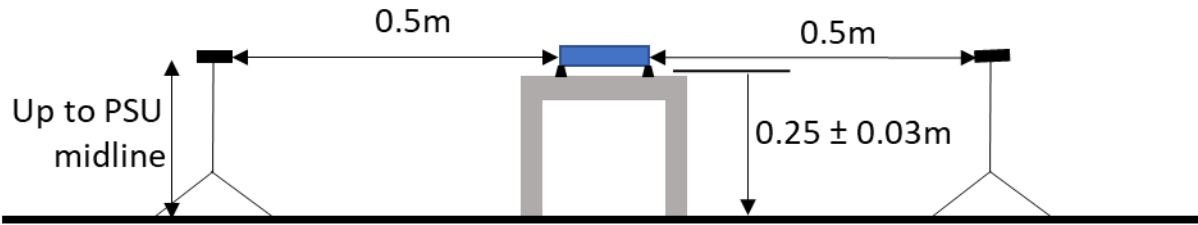
Figure 4-2 PSU installation and operator microphone position locations [side view] in accordance with ECMA-74 Clause 5.1.7.

4.1.6   Measurement of Acoustical Data

The following data shall be recorded simultaneously for each operating mode defined in *Section 4.1.7 Operating Modes:*

- •   Raw waveform (pressure time history) and associated calibration information
- •   Rotation speed of the fan.

These signals are then used to calculate the acoustic metrics.

The duration of the recording is outlined by operating mode in *Section 4.1.7 Operating Modes*.

4.1.7   Operating Modes

Acoustical requirements are provided for five primary operating modes:

1. Continuous Fan Speed Sweep
2. Discrete Fan Speed Sweep
3. Constant Fan Speed
4. Transient Event
5. Retaining Latch

Fan sweep requirements provide overall limitations on the fan performance and give integrator designers data to use for engineering products. Constant speed fan operation modes reflect the efficiency of the design by reporting and limiting response at simulated operating points at a given PSU inlet temperature, load as a percentage of maximum PSU outlet wattage, inlet pressure, and altitude. Limits on transient fan control response are designed to prevent annoying oscillation during steady state operation, overshoot when the PSU changes load or inlet temperature states, and perceptions of poor product quality during PSU startup and shutdown. Lastly, limits are set on the mechanical latch noise to prevent annoyance or perceptions of poor product quality during physical install or removal of the PSU.

The 5 operating modes are now outlined in more detail:

4.1.7.1   Continuous Fan Speed Sweep

Fan speed shall be continuously ramped from 10% of the maximum fan speed to 100% of the maximum fan speed over a period of at least 120 seconds. Recordings should contain at least 5 seconds at the minimum and maximum fan speeds to ensure that all fan speeds are contained in the analysis sweep.

4.1.7.2   Discrete Fan Speed Sweep

The fan speed shall be operated at 10 discrete fan speeds from 10% of the maximum fan speed to 100% of the maximum fan speed. The fan speed shall be incremented by 10% of the maximum fan speed. Recordings at each discrete fan speed sweep should have an equal measurement duration of at least 10 seconds.

4.1.7.3   Constant Fan Speed

For the duration of the recording, the fan will be manually controlled at a fixed fan speed. The fan should be operating at the prescribed fan speed for at least 30 seconds prior to beginning a recording to ensure no transient fan speed fluctuations are captured. Constant fan speed recordings shall be at least 10 seconds in duration.

This standard specifies a set of operating modes that nominally correlate to potential end-user states of operation. These operating modes are defined by inlet air temperature to the PSU, an operating load defined as a percentage of the maximum PSU design load, inlet air pressure differential, and altitude. For acoustical testing, these load conditions shall be simulated by manually setting the fan speed to the measured performance of the PSU under the default fan speed control algorithm in a thermal test chamber as performed to satisfy the requirements of *Section 3 Thermal Requirements* in this document.

For several acoustical metrics defined in this section, a maximum fan speed is used to calculate a percentage of potential fan speed. For acoustical and vibration testing, maximum fan speed is the maximum fan speed required to cool the PSU at 60°C inlet and 100% of maximum design power as measured for *Section 3 Thermal Requirements*.

For some test constant fan speed testing, a load is required to be applied during testing to measure potential electronic noise. For load testing, a resistive load shall be used and installed such that the components applying the load do not interfere with the transmission of noise between the PSU fan inlet or outlet and the bystander microphone positions. The resistive load shall not be a DC electronic load or any load that is itself a source of noise. Equipment used to apply a load should be removed for all testing that does not require a resistive load.

Nominal operating states are defined below.

Table 4-1 Definition of operating modes for constant fan speed testing for Home & Office PSU's.

Constant Fan Speed Operating Modes					
Nominal Emulated Operating State	Standby	Idle	Operating Redundant	Operating Non-Redundant	Maximum, Non-Redundant
Applied/Simulated % of max Load on single Power Supply	10%	25%	30%	60%	100%
Apply Resistive Load?	Yes	Yes	No	No	No
Simulated Power Supply Inlet Temperature	25° C	25° C	35° C	35° C	35° C

Altitude, m	900	900	900	900	900

Table 4-2 Definition of operating modes for constant fan speed testing for General Purpose & Storage PSU's and High-Performance Computing PSU's.

Constant Fan Speed Operating Modes					
Nominal Emulated Operating State	Standby	Idle	Operating Redundant	Operating Non-Redundant	Maximum, Non-Redundant
Applied/Simulated % of max Load on single Power Supply	10%	25%	30%	60%	100%
Apply Resistive Load?	Yes	Yes	No	No	No
Simulated Power Supply Inlet Temperature	25° C	50° C	55° C	55° C	60° C
Altitude, m	900	900	900	900	900

4.1.7.4   Transient Event

For transient mode evaluation, a fully operational PSU shall be used. The fan shall be controlled by the default fan control algorithm.

The operator applying power should minimize acoustical impact on the measurement by remaining as still as possible and standing out of the direct acoustical path between the device and the measurement microphones.

Two primary operating transient operating modes shall be evaluated:
   a)   Apply power by inserting the external power plug into the device.
   b)   Remove power by unplugging the external power plug from the device.

Transient event recordings shall be at least 10 seconds. At least 1 second shall be recorded prior to the application or removal of the power plug.

4.1.7.5   Retaining Latch

For retaining latch evaluation, a fully operational PSU shall be used. For this operating a mode the PSU shall have no inlet plug installed.

To perform a latch event, the operator shall place a hand on the PSU to prevent it from moving and with the thumb of the opposite hand, push the latch open so that it would be fully disengaged when installed in a system; for most products the latch element should be touching the PSU housing in this mode. To initiate the latch event, the operator should suddenly release the latch to capture the closure sound of the retaining latch.

At least three latch events shall be performed in each recording. At least 10 seconds shall pass between latch events. At least 10 seconds shall be recorded prior to the first latch event. Each recording shall be at least 40 seconds.

4.1.8   Calculation of Acoustical Values by Operating Mode

4.1.8.1   Continuous Fan Speed Sweep

For continuous fan speed sweeps, analysis should focus on the ramped fan speed region of the recording and thus recordings should be edited to include less than 500ms of starting and ending fan speeds.

For continuous fan speed sweep recordings, the following acoustical values shall be calculated:
- ISO 532-1 Loudness vs. % Maximum Fan Speed. In this calculation the recording shall be divided into RPM bins no smaller than 50 RPM's and no larger than 150 RPM's. In each of these RPM bins, an average ISO 532-1 loudness shall be calculated. The RPM bins should then be scaled to the maximum thermal fan speed defined in Section 4.1. For ISO 532-1, assume a free sound field for the purposes of this calculation. A single curve should be calculated for each fan sample tested.
- Maximum Specific Prominence Ratio vs. % of Maximum Fan Speed. In this calculation the recording shall be divided into RPM bins no smaller than 50 RPM's and no larger than 150 RPM's. In each of these RPM bins, prominence ratio shall be calculated with an average FFT in accordance with ECMA 418-1 Clause 12. Next, the maximum measured prominence ratio across all frequencies per RPM bin shall be calculated. The RPM bins should then be scaled to the maximum thermal fan speed defined in Section 4.1. A single curve should be reported for each fan sample tested.
- Sound Pressure Level vs. % of Maximum Fan Speed. In this calculation the recording shall be divided into RPM bins no smaller than 50 RPM's and no larger than 150 RPM's. In each of these RPM bins, unweighted sound pressure level and A-weighted sound pressure level shall be calculated. Fast time weighting shall be used for the time integral duration. The RPM bins shall then be scaled to the maximum thermal fan speed defined in Section 4.1. One plot for each operator position and fan vendor shall be generated. Both A-weighted and unweighted sound pressure level shall be included on the plot. All samples tested with the same vendor shall be on the plot.

4.1.8.2   Discrete Fan Speed Sweep

For discrete fan speed sweep recordings, the following acoustical values shall be calculated:
- Mean A-weighted Sound Power Level vs. % Maximum Fan Speed. For each discrete fan speed sweep recording, A-weighted sound power level shall be calculated in accordance with ECMA-74 clause 7. For multiple samples of the same fan model the linear mean of n, samples shall be calculated for reporting. One curve of mean A-weighted Sound Power Level vs. % of maximum fan speed shall be calculated for each fan model.

4.1.8.3   Constant Fan Speed

For constant fan speed recordings, the following acoustical values shall be calculated:
- Mean A-weighted Sound Power Level. For each recording, A-weighted Sound Power Level shall be calculated in accordance with ECMA-74 clause 7. For each operating mode, the mean A-

weighted Sound Power Level shall be calculated for each fan model. One mean A-weighted Sound Power Level shall be calculated for each operating mode and fan model.

- Maximum Specific Prominence Ratio. For each recording, specific prominence ratio shall be calculated at frequency resolution smaller than 7Hz using the prominence ratio methods of ECMA 418-1. The maximum measured specific prominence ratio across all frequencies shall be calculated for each recording. For each operating mode and fan model, one maximum shall be calculated as the maximum of the individual maximum values measured.

4.1.8.4 Transient Modes

For transient mode recordings, the following acoustical values shall be calculated:

- Maximum of ISO 532-1 Loudness vs. Time. For each recording, loudness should be calculated in accordance with ISO 532-1 vs. time. Next take the maximum value from the recording to calculate the maximum loudness for each recording. Finally, the maximum for all transient tests should be obtained.
- Maximum specific prominence ratio. For each recording, specific prominence ratio shall be calculated at frequency resolution smaller than 7Hz using the prominence ratio methods of ECMA 418-1. Next, the maximum value across all frequencies and time shall be calculated. Finally, the maximum value across all samples tested shall be calculated.

4.1.9 Acoustical Requirements

Acoustical requirements include specific limits on sound power, sound pressure, and sound quality metrics. Acoustical requirements also include some report-only values for the purposes of designing systems with these PSUs as components. PSU limits may differ based on the intended PSU application space:

- Home & Office use PSU's are designed for use in lightly configured rack and tower servers that may be physically located in home or office environments around bystanders. PSU's that support low-line AC voltage input and that are designed for maximum output of approximately 1400W (including low-line AC derated power) will likely be required to meet this level of acoustical output. A PSU vibration limit is also applicable to rotational storage media, see *Section 4.2 Vibration Requirements.*
- General data center & storage PSU's are designed for general purpose server applications and specifically for servers that utilize rotational media for storage. Rotational storage media has a demonstrated sensitivity to excessive noise and vibration levels, the maximum acoustical output of these PSU's is limited to prevent excessive impact to storage performance. A PSU vibration limit is also applicable to rotational storage media, see *Section 4.2 Vibration Requirements*.
- High performance computing PSU's are designed for high power sever computing applications in unattended data center environments and other areas where power density is prioritized over sound quality. PSU's designed to meet this acoustical output category may degrade the performance of rotational storage devices in some server and storage applications.
- .

 Limits are defined according to operating mode for each PSU classification.

In addition to quantifiable acoustical metric limits, two additional sound quality requirements must be evaluated by the PSU vendor:

- The default fan control algorithm should not induce fan oscillation during steady state load and inlet temperature conditions. Operator position noise levels should not fluctuate more than ±2 dBA over a 10-minute period. A statement indicating compliance to this specification is required.
- The default fan control algorithm should not induce overshoot over 3dB during fan speed transients of PSU load change. A statement indicating compliance to this specification is required.
- The PSU should not produce any buzzes, squeaks, or rattles during operation. A statement indicating no buzzes, squeaks, or rattles shall be included in the report for compliance to this specification.

Table 4-3 Home & Office PSU Acoustical Requirements

Home & Office PSU Acoustical Requirements				
Continuous Fan Speed Sweep Requirements				
Metric	**Limit**			
SPL vs. % of Max RPM	Report			
Loudness vs. % of Max RPM	Report			
Maximum Prominence Ratio vs. % of Max RPM	For fan speeds between 10% and Operating Redundant ≤ 15dB For fan speeds more than Operating Redundant ≤ 20dB			
Discrete Fan Speed Sweep Requirements				
Mean A-weighted Sound Power Level vs. % of Max Fan Speed	Report			
Constant Fan Speed Requirements				
Nominal Emulated Operating State	Standby	Idle	Operating Redundant	Operating Non-Redundant	Maximum Non-Redundant
Simulated % of max Load on single Power Supply	10%	25%	30%	60%	100%
Apply Resistive Load?	Yes	Yes	No	No	No
Simulated Power Supply inlet Temperature	25° C	25° C	35° C	35° C	35° C
Simulated Altitude, m	900	900	900	900	900
Fan Speed (% of Max Fan Speed)	Report	Report	Report	Report	Report
LwA,m, Bels, limit	3.9	4.4	4.7	6.2	7.1
Maximum Prominence Ratio limit					
Transient Mode Requirements				
Maximum of Loudness vs. Time	1.0 sone			
Maximum Prominence Ratio	9dB			

Retaining Latch Noise Requirements	
Maximum of Loudness vs. Time	1.0 sone
Maximum Prominence Ratio	9dB, no prominent tones
General Thermal Control Requirements	
Operating Thermal Response	No Oscillation: < 2 dB over 10-min. Report compliance. No Overshoot: <3dB. Report compliance.
All Operating Modes	No buzzes, squeaks, or rattles. Report compliance.

Table 4-4 General Data Center & Storage PSU Acoustical Requirements

General Data Center & Storage PSU Acoustical Requirements				
Continuous Fan Speed Sweep Requirements				
Metric	**Limit**			
SPL vs. % of Max RPM	Report			
Loudness vs. % of Max RPM	Report			
Maximum Prominence Ratio vs. % of Max RPM	For fan speed between 10% and Operating Redundant, ≤ 20dB For fan speed more than Operating Redundant, ≤ 25			
Discrete Fan Speed Sweep Requirements				
Mean A-weighted Sound Power Level vs. % of Max Fan Speed	Report			
Constant Fan Speed Requirements				
Nominal Emulated Operating State	Standby	Idle	Operating Redundant	Operating Non-Redundant	Maximum Non-Redundant
Simulated % of max Load on single Power Supply	10%	25%	30%	60%	100%
Apply Resistive Load?	Yes	Yes	No	No	No
Simulated Power Supply inlet Temperature	25° C	50° C	55° C	55° C	60° C
Simulated Altitude, m	900	900	900	900	900
Fan Speed (% of Max Fan Speed)	Report	Report	Report	Report	Report
LwA,m, Bels, limit	4.6	4.9	5.2	6.7	7.1
Maximum Prominence Ratio limit					
Transient Mode Requirements				
Maximum of Loudness vs. Time	1.0 sone			
Maximum Prominence Ratio	9dB			
Retaining Latch Noise Requirements				
Maximum of Loudness vs. Time	1.0 sone			

Maximum Prominence Ratio	9dB, no prominent tones
General Thermal Control Requirements	
Operating Thermal Response	No Oscillation: < 2 dB over 10-min. Report compliance. No Overshoot: <3dB. Report compliance.
All Operating Modes	No buzzes, squeaks, or rattles. Report compliance.

Table 4-5 High Performance Computing PSU Acoustical Requirements

High Performance Computing PSU Acoustical Requirements				
Continuous Fan Speed Sweep Requirements				
Metric	**Limit**			
SPL vs. % of Max RPM	Report			
Loudness vs. % of Max RPM	Report			
Maximum Prominence Ratio vs. % of Max RPM	≤ 25dB			
Discrete Fan Speed Sweep Requirements				
Mean A-weighted Sound Power Level vs. % of Max Fan Speed	Report			
Constant Fan Speed Requirements				
Nominal Emulated Operating State	Standby	Idle	Operating Redundant	Operating Non-Redundant	Maximum Non-Redundant
Simulated % of max Load on single Power Supply	10%	25%	30%	60%	100%
Apply Resistive Load?	Yes	Yes	No	No	No
Simulated Power Supply inlet Temperature	25° C	50° C	55° C	55° C	60° C
Simulated Altitude, m	900	900	900	900	900
Fan Speed (% of Max Fan Speed)	Report	Report	Report	Report	Report
LwA,m, Bels, limit	4.6	6.9	7.1	8.6	Report
Maximum Prominence Ratio limit					
Transient Mode Requirements				
Maximum of Loudness vs. Time	1.0 sone			
Maximum Prominence Ratio	9dB			
Retaining Latch Noise Requirements				
Maximum of Loudness vs. Time	1.0 sone			

Maximum Prominence Ratio	9dB, no prominent tones
General Thermal Control Requirements	
Operating Thermal Response	No Oscillation: < 2 dB over 10-min. Report compliance. No Overshoot: <3dB. Report compliance.
All Operating Modes	No buzzes, squeaks, or rattles. Report compliance.

4.1.10 Reporting Requirements

Vendors should provide detailed identifying information about the following items:

- PSU Make/Model/Serials tested
- Fan make, model, and PPID
- Laboratory information

For continuous fan sweep mode, the following items shall be reported:

- Plot of ISO 532-1 Loudness vs. % of Maximum Fan Speed for each operator position and fan vendor.
    1. One front operator position plot per fan vendor
    2. One rear operator position plot per fan vendor
- Plot of Maximum Specific Prominence Ratio vs. % of Maximum Fan Speed for each operator position and fan vendor.
    1. One front operator position plot per fan vendor
    2. One rear operator position plot per fan vendor
- Plot of unweighted sound pressure level and A-weighted sound pressure level vs. % of Maximum Fan Speed for each operator position and fan vendor.
    1. One front operator position plot per fan vendor, include A-weighted and unweighted SPL
    2. One rear operator position plot per fan vendor, include A-weighted and unweighted SPL

For discrete fan sweep mode, the following items shall be reported:

- Plot of averaged sound power, $L_{wA,m}$ vs. % of maximum fan speed for each fan vendor. Report only.

For Constant Speed Fan testing, the following items shall be reported:

- Mean A-weighted Sound Power Level for each fan vendor and operating mode
- Maximum prominence ratio for each fan vendor and operating mode.

For Transient Mode testing, the following items shall be reported:

- Maximum loudness for all samples
- Maximum prominence ratio for all samples

For Retaining Latch Noise, the following items shall be reported:

- Maximum loudness for all samples
- Maximum prominence ratio and frequency for all samples

4.2 Vibration Requirements

Each PSU offering shall meet a set of vibration limits and reporting requirements to be compliant with this specification.

4.2.1 General, Laboratory, and Requirements

Vibration limits are designed to avoid performance degradation in electro-mechanical storage components in end-use PSU applications. This standard is written with the intent that acoustical and

vibration measurements can be performed concurrently; however, vibration measurements may be conducted outside of an acoustical facility if background vibration noise can be controlled, and environmental conditions can be satisfied.

Vibration sampling requirements shall be the same as acoustical sampling requirements detailed in *Section 4.1.1 General, Laboratory, and Sampling Requirements.*

4.2.2   Test Environment

The test environment shall be a quiet room with a sufficiently low vibration noise floor to measure the performance of the PSU. The environmental requirements of section 4 are strongly recommended.

For environments that do not meet the requirements of *Section 4.1 Acoustic Requirements*, measurement of the background vibration levels should be performed to verify no elements of noise are within 15dB of the measured PSU vibration level at 50% of PSU fan speed in all individual channels.

4.2.3   Instrumentation

Four accelerometers shall be required for vibration testing. Accelerometer shall have a mass equal to or less than 1 gram and be capable of measuring vibration to an accuracy of ±5% over the frequency range from 10 Hz to 5000 Hz.

A method for measuring fan speed is required for vibration testing. Although optical tachometers may be used, direct measurement of the fan tachometer signal is strongly recommended. Optical tape applied to the fan may impact the vibration results.

4.2.4   Installation and Operation of the Power Supply

The PSU shall be installed on a support structure as described in *Section 4.1 Acoustic Requirements*, or at the center of a standard test table as described in ECMA-74 Annex A.1.

Vibration isolation elements should be placed on the bottom of the PSU at each of the four corners of the device; rubber isolators approximately 20mm in diameter and 12mm in height are recommended.

4.2.5   Accelerometer Positions

For the purposes of vibration testing, the front and rear of the PSU shall be defined as in Section 4. The bottom of the PSU shall be designated as the exterior surface of the enclosure closest to and coplanar to the primary PCB of the PSU.

Four accelerometers shall be installed in the bottom side of the power supply when measuring vibration as shown in the figures below.
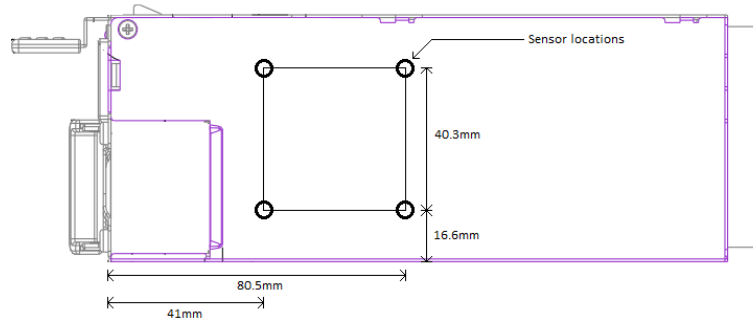
Figure 4-3 Accelerometer's locations in the bottom of the 185mm by 73.5mm power supply

Figure 4-4 Accelerometer's locations in the bottom of the 185mm by 60mm power supply

Figure 4-5 Accelerometer's locations in the bottom of the 265mm by 73.5mm power supply

4.2.6   Measurement of Acoustical Data

The following data shall be recorded simultaneously for all PSU vibration testing:

- Acceleration time history
- Fan speed time history

The duration of the recording is outlined by operating mode in *Section 4.2.7 Operating Modes.*

4.2.7   Operating Modes

4.2.7.1   Continuous Fan Speed Sweep

Fan speed shall be continuously ramped from 10% of the maximum fan speed to 100% of the maximum fan speed over a period of at least 120 seconds. Recordings should contain at least 5 seconds at the minimum and maximum fan speeds to ensure that all fan speeds are contained in the analysis sweep.

4.2.8 Calculation of Vibration Values to Report

4.2.8.1 Continuous Fan Speed Sweep

For continuous fan speed sweeps, analysis should focus on the ramped fan speed region of the recording and thus recordings should be edited to include less than 500ms of starting and ending fan speeds prior to calculation of vibration values.

For continuous fan speed sweep recordings, the following vibration values shall be calculated:

- Mean Peak-hold Spectrum. For each accelerometer channel, a spectrum vs. time shall be calculated using an FFT with the following properties:
  - Window size set to the first factor of two where the frequency resolution is equal to or less than 6Hz.
  - Hanning window
  - ≥75% overlap of FFT windows
  - RMS amplitude scaling

  Next the maximum value measured in each frequency bin shall define the peak-hold spectrum for a single accelerometer channel. Finally, the mean of peak-hold spectrums for four accelerometer channels shall be calculated as the mean peak-hold spectrum. One spectrum shall be calculated for each fan sample.

- Mean Acceleration Level vs. % Maximum Fan Speed. In this calculation the recording shall be divided into RPM bins no smaller than 50 RPM's and no larger than 150 RPM's. In each of these RPM bins, acceleration level for each accelerometer channel shall be calculated using rectangular (real-time) time weighting. The mean of all four accelerometer channels shall be calculated for each frequency bin to obtain the mean acceleration level. The RPM bins shall then be scaled to the maximum thermal fan speed defined in *Section 4.1.1 General, Laboratory, and Sampling Requirements*.

4.2.9 Vibration Requirements

4.2.9.1 Continuous Fan Speed Sweep

Peak-Hold spectrum response of the continuous fan speed sweep shall be less than a frequency-dependent limit curve defined by vertices listed in *Table 4-6 Mean peak vibration spectrum limit line vertices*. A plot of the limit line composed of these vertices is shown in *Figure 4-6 Plot of mean peak vibration spectrum limit.*

Table 4-6 Mean peak vibration spectrum limit line vertices

Mean Peak Vibration Spectrum Limit	
Frequency (Hz)	Vibration Level (g)
0	0
800	0.7
1250	0.7
1900	0.4

2500	0.4
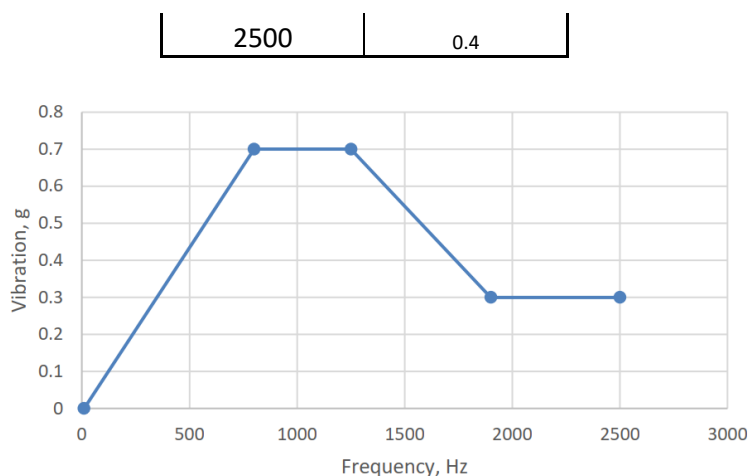
Figure 4-6 Plot of mean peak vibration spectrum limit.

4.2.9.2   Fan Balance Requirements

In addition to PSU requirements, each fan shall meet ISO1940 Balance Grade G5.2 or better. This fan balance grade will help ensure that the PSU meets continuous fan sweep vibration and acoustical requirements.

4.2.10 Reporting Requirements

Fan and PSU identification reporting requirements shall be the same as *Section 4.1.10 Reporting Requirements.*

For continuous fan sweep mode, the following items shall be reported:

- Plot of Mean Peak-Hold Spectrum with overlay of Mean Peak Vibration Limit indicating compliance with the spec. Report one plot for each fan vendor model tested.
- Plot of Mean Acceleration Level vs. % of Maximum Fan Speed. One plot per fan model that includes each mean acceleration level curve.

5   Electrical Input Requirements

5.1   High Voltage AC/DC Input Requirements

5.1.1   Power Factor and iTHD

The power supply must meet the power factor and current iTHD requirements are stated below. These requirements are within the Energy Star® Program Requirements for Computer Servers.

Table 5-1 Power factor requirements

Output power	10% load	20% load	50% load	100% load
Power factor	> 0.92	> 0.96	> 0.98	> 0.99

Table 5-2 iTHD requirements

Output power	< 5%	5%≤In≤10%	10%<Iin≤20%	20%<Iin≤50%	50%<Iin≤100%
Current iTHD (240VAC)	20%	8.5%	< 7.5%	< 5%	< 3.5%

Notes:

1. Tested at 230Vac, 50Hz.
2. Tested according to Generalized Internal Power Supply Efficiency Testing Protocol. This is posted at http://www.plugloadsolutions.com/80pluspowersupplies.aspx

5.1.2   Inlet Connector

The AC input connector shall be an IEC 320 C-22, IEC 320 C-20 connector may be used upon request from the costumer for environment conditions where the exhaust temperature of the power supply will not exceed 70C. This inlet is rated for 16A/250VAC. Additionally an IEC 320 C-14 can be used for input currents up to 10A/250VAC. IEC320-C16 can be used to support higher exhaust temperatures in the power supply at 10 Amperes.

277VAC/380VDC inlet connector is to be defined.

5.1.3   Input Voltage Specification

The power supply must operate within all specified limits over the following input voltage ranges. Harmonic distortion of up to 10% of the rated line voltage must not cause the power supply to go out of specified limits.

Table 5-3 AC Input voltage ranges

PARAMETER	MIN	RATED	V_{MAX}	Startup VAC[2]	Power Off VAC
Voltage (240 V_{RMS})	180 V_{RMS}	200-240 V_{RMS}	264 V_{RMS}	174V_{RMS} – 180V_{RMS}	169V_{RMS}– 175V_{RMS}
Voltage (Wide range)	90 V_{RMS}	120/240 V_{RMS}	264 V_{RMS}	84V_{RMS} – 89V_{RMS}	79V_{RMS} – 85V_{RMS}
Voltage (277 V_{RMS})	180 V_{rms}[1]	200-277 V_{RMS}	305 V_{RMS}	243V_{RMS} – 249V_{RMS}	238V_{RMS} – 244V_{RMS}
Frequency	47 Hz	50/60	63 Hz		

Notes:
1. 277VAC input power supply's efficiency shall be tested at 230Vac, 50Hz.

Application of an input voltage below the power off threshold shall not cause damage to the power supply, including a blown fuse.

5.1.3.1   Crest Factor

The PSU shall be capable of starting and operating at Minimum Turn-On Voltage and Maximum Operating Voltage with Crest Factors (C.F.) between 1.1 and 1.5 (both inclusive) of the Input Waveform. In either case the PSU continues to operate but PSU performance may not meet the specification requirements such as but not limited to – iTHD, Power Factor, efficiency, output voltage regulation and ripple, dynamic load response. Crest factor (C.F.) is defined as the ratio of Peak Voltage to RMS Voltage of the Input Sinewave. CF Test should be done using both waveforms – Clipped Sinewave and AC Sinewave with Peak at the top. The input voltage shall be provided by a programmable source capable of providing a clipped AC waveform and an AC Sinewave with peak at the top shown in the figure below.
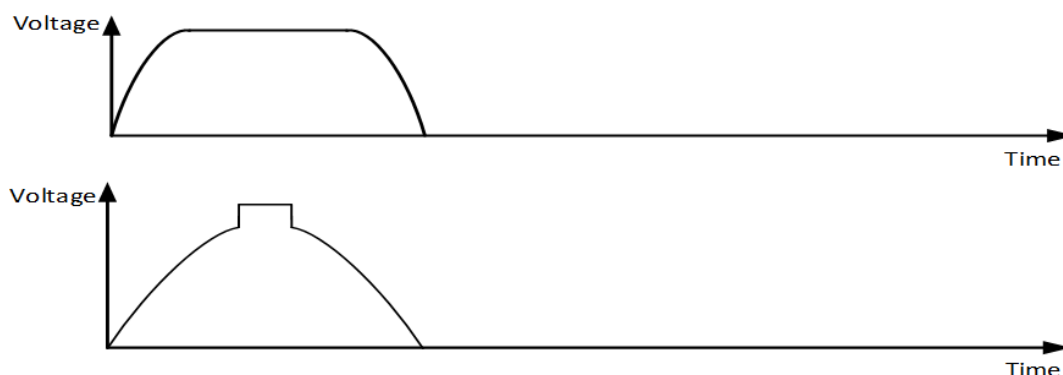
Figure 5-1 Crest factor examples

5.1.3.2 240VDC/380VDC

The power supply must be able to operate normally with 240VDC input.

- Operating range: 192VDC to 310VDC
- PMBus commands must function normally
- Power timing requirements met during power cycling
- Output power requirements support for same equivalent RMS AC input voltage
- LED functioning correctly
- In Always Standby mode in a 1+1 PSU configuration the active PSU will have >95% load, the Standby PSU will have <5% load
- In 1+1 PSU configuration and one PSU Active and the other in Always Standby mode; if the Active PSU fails the Standby PSU must support the load to maintain output voltage > 11.20V. Tested with 2,200uF 12V capacitance.
- For slow input voltage ramp.
- turn ON input voltage: 180VDC / 192VDC (MIN/MAX)
- turn OFF input voltage: 175VDC / 187VDC (MIN/MAX)

Table 5-4 DC input voltage ranges

PARAMETER	MIN	RATED	V_{MAX}	Startup VDC	Power Off VDC
Voltage (240 V_{DC})	192 V_{DC}	200-240 V_{DC}	310 V_{DC}	180V_{DC} – 192V_{DC}	175V_{DC} – 187V_{DC}
Voltage (380 V_{DC})	260 V_{DC}	336 V_{DC}	400 V_{DC}	254V_{DC} – 260V_{DC}	249V_{DC} – 255V_{DC}
Hysteresis				5 V	5 V

5.1.4 Line Isolation Requirements

The power supply shall meet all safety agency requirements for dielectric strength. Additionally, power supply vendor must provide the customer with written confirmation of dielectric withstand test which includes voltage level, duration of test and identification detailing how each power supply is marked to indicate dielectric withstand test had been completed successfully. Transformers' isolation between primary and secondary windings must comply with the 3000Vac (4242Vdc) dielectric strength criteria. If the working voltage between primary and secondary dictates a higher dielectric strength test voltage the highest test voltage should be used. In addition, the insulation system must comply with reinforced insulation per safety standard IEC 950. Separation between the primary and secondary circuits, and primary to ground circuits, must comply with the IEC 950 spacing requirements.

Note: This test shall be done only during development.

5.1.5   Line Dropout/Holdup

5.1.5.1   Main output

An AC/DC line dropout is defined to be when the AC/DC input drops to $0V_{AC/DC}$ at any phase of the AC/DC line for any length of time. During an AC/DC dropout the power supply must meet dynamic voltage regulation requirements. An AC/DC line dropout of any duration shall not cause tripping of control signals or protection circuits other than the SMBAlert# signal. If the AC/DC dropout lasts longer than the holdup time the power supply should recover and meet all turn on requirements. The power supply shall meet the AC/DC dropout requirement overrated AC/DC voltages and frequencies. A dropout of the AC/DC line for any duration shall not cause damage to the power supply.

Table 5-5 AC/DC holdup / dropout

Loading during AC/DC dropout / holdup	Holdup time / Dropout duration[1]
0% to 100% of rated load	10msec

Notes:
4. This must be proven by calculation using the worst capacitance tolerance, variance with temperature and bus voltage. It shall be tested with a bulk capacitor having the minimum capacitance tolerance, at worst case loading and at worst case AC voltage conditions.

5.1.5.2   Auxiliary (Stand-by) Output

The 12VSB output voltage should stay in regulation under its full load (static or dynamic) during an AC dropout of 70ms min (=12VSB holdup time) at 70% of max load and 150ms minimum at 1 Ampere of load whether the power supply is in ON or OFF state (PSON asserted or de-asserted).

5.1.6   Line Fuse

The power supply shall have one line fused in the single line fuse on the line (Hot) wire of the AC input. The line fusing shall be acceptable for all safety agency requirements. The input fuse shall be a High breaking capacity fast blow type. AC/DC inrush current shall not cause the AC/DC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC/DC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

5.1.7   Inrush Current

AC line inrush current shall not exceed 35A peak ignoring the initial 500us of the EMI filter charge, for up to one-half of the AC cycle, after which the power supply is allowed to have a secondary inrush event for up to TBD Amperes and lasting for up to 2500ms, the input current should be no more than the specified maximum input current. The peak inrush current shall be less than the ratings of its critical components (including input fuse, bulk rectifiers, and surge limiting device).

The power supply must meet the inrush requirements for any rated AC voltage, during turn on at any phase of AC voltage, during a single cycle AC dropout condition as well as upon recovery after AC dropout of any duration, and over the specified temperature range (Top).

5.1.7.1   Cold Start Inrush Current With PSON# asserted

The PSU Input Current during a Cold Start event (with PSON# in asserted state) should follow the timing diagram below.
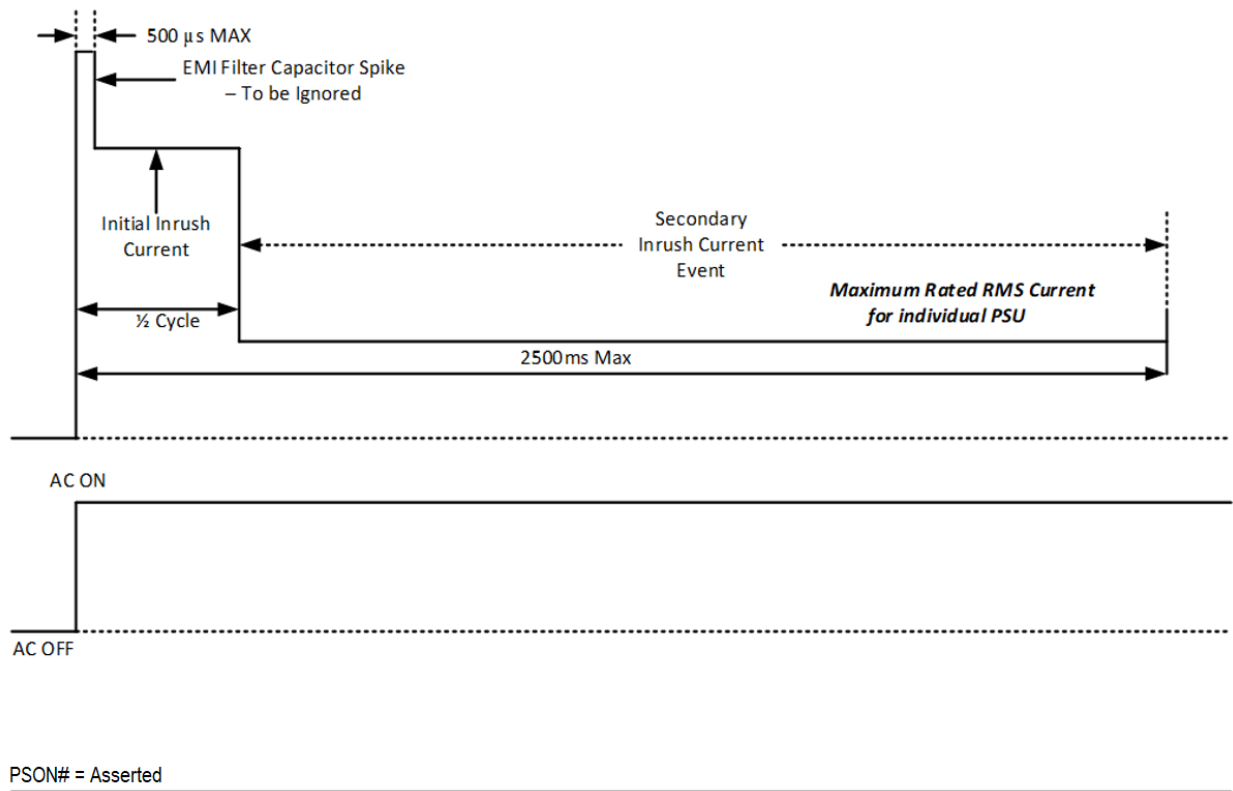
Figure 5-2 Inrush condition at cold start with PSON# asserted

At any point during this event input current should meet I vs t profile shown below (excluding the charging current of EMI Caps if the duration of the peak is ≤ 500μs)
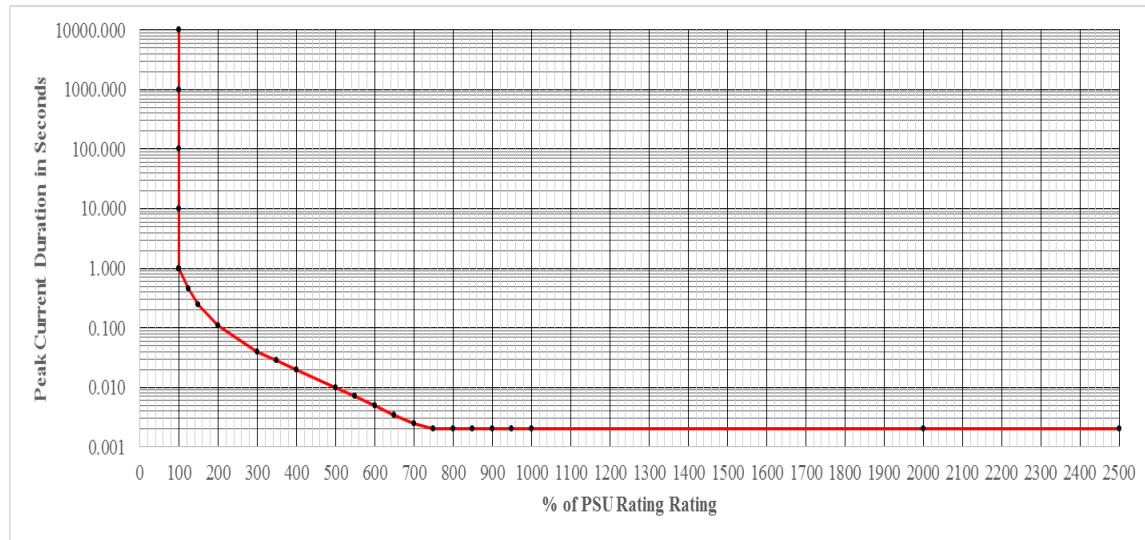
Figure 5-3 I vs T profile of the PSU input current

5.1.7.2   Cold Start Inrush Current With PSON# de-asserted

The PSU Input Current during a Cold Start event (with PSON# in De-Asserted state) should follow the timing diagram below.
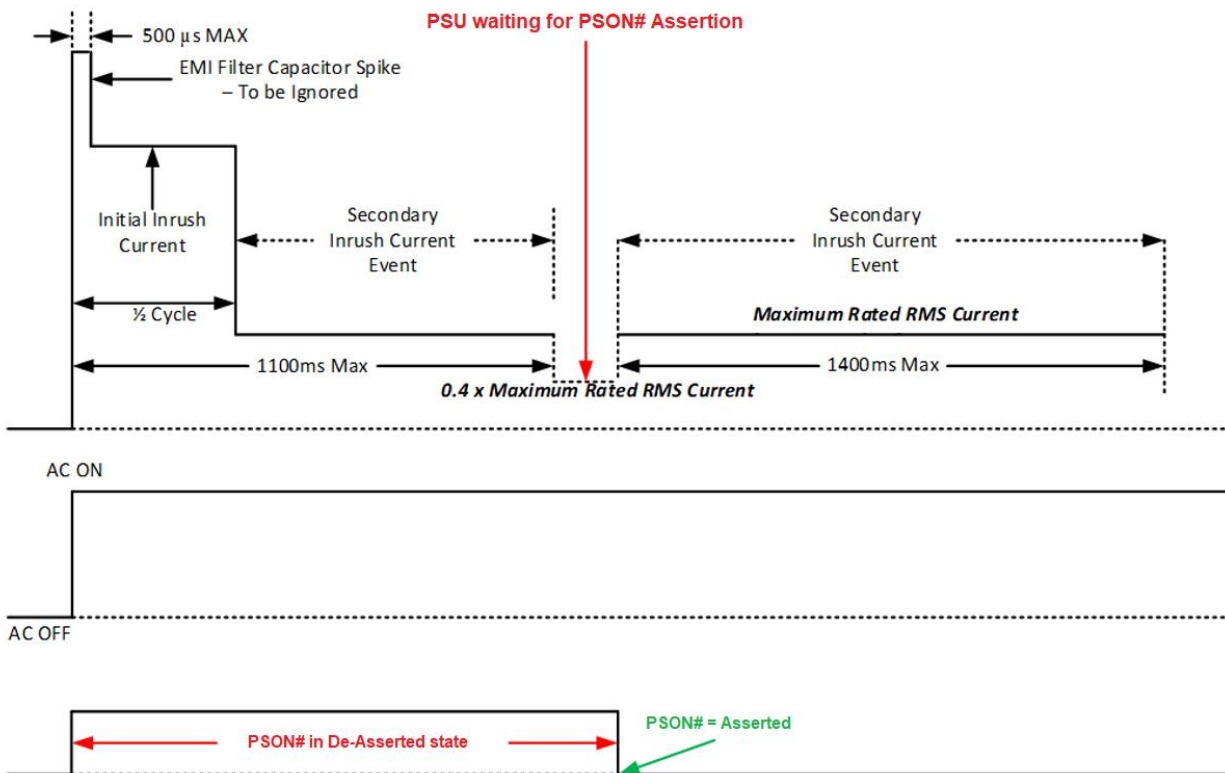
Figure 5-4 Cold start inrush current with PSON# de-asserted

5.1.7.3   Re-rush Current

In addition to the Inrush Requirements, the Re-Rush current profile on the PSU should satisfy the following requirements when the Input Voltage is applied after an Input Brown out / Black Out event. The re-application of the Input Voltage can happen at the Peak of the Input Waveform at Maximum Specified Operating Voltage. The values defined below are true over the Operating Input Voltage, Frequency, Load Capacity and Temperature Range of the PSU. The re-rush condition shall meet the timing and duration of the figure below.
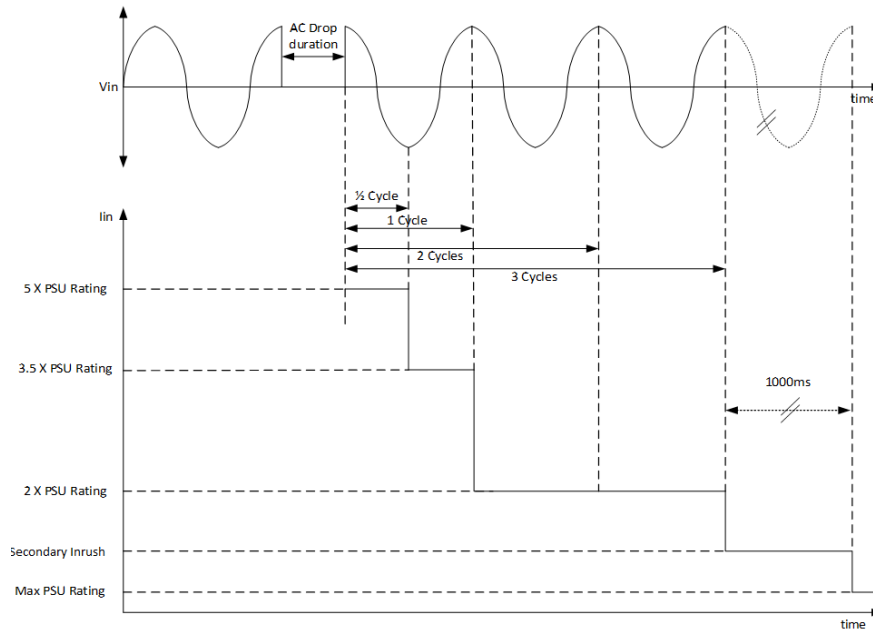
Figure 5-5 Re-rush current and timing

The RMS Value of the Re-Rush Current will not exceed 5 x Maximum PSU Rating over ½ Cycle of Input Frequency, 3.5 x Maximum PSU Rating over 1 Cycle of Input Frequency. In addition, the Input Current of the PSU should settle to a value less than or equal to 2 x Maximum PSU Rating of the PSU within 2 Cycles of the Input Frequency after the AC Input is applied.

The secondary Inrush Current Event if present should be over within 1000ms after the initial 3 cycles of re-application of Input. The RMS value of this Secondary Inrush Current should not exceed 2 x Maximum Rated Input Current of the PSU as measured during any 100ms interval within the 1000ms period. Maximum of 2 such intervals are permitted during this 1000ms period. After 1000ms the Input Current of the PSU should be less than or equal to the Maximum Rated Current Rating of the PSU.

At any point during this event, input current should fit under the profile shown in *Figure 5-3 I vs T profile of the PSU input current*.

5.1.8   Line Transient Specification

AC line transient conditions shall be defined as "sag" and "surge" conditions. "Sag" conditions are also commonly referred to as "brownout", these conditions will be defined as the AC line voltage dropping

below nominal voltage conditions. "Surge" will be defined to refer to conditions when the AC line voltage rises above nominal voltage. The power supply shall meet the requirements under the following AC line sag and surge conditions.
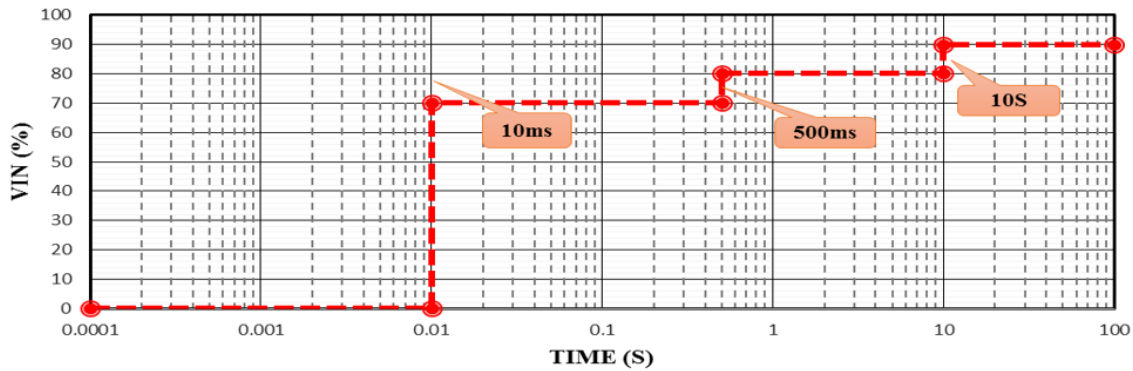
Figure 5-6 AC input brown-out behavior

Note: This test shall be done only during development.

Table 5-6 AC Line Surge Transient Performance

AC Line Surge				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60Hz	No loss of function or performance
0.5ms to ½ AC cycle	35%	Mid-point of nominal AC Voltages	50/60Hz	No loss of function or performance

Note: During these tests, the load should be set to 50% of maximum load.

Additional requirements are described in TBD file.

5.1.9   Susceptibility Requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter which meets the criteria defined in the SSI document EPS Power Supply Specification.

Table 5-7 Performance criteria

Level	Description
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

5.1.10 Electrostatic Discharge Susceptibility

The power supply shall comply with the limits defined in EN 55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-2: Edition 1.2: 2001-04 test standard and performance criteria B defined in Annex B of CISPR 24.

5.1.11 Fast Transient/Burst

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-4: Second edition: 2004-07 test standard and performance criteria B defined in Annex B of CISPR 24.

5.1.12 Radiated Immunity

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-3: Edition 2.1: 2002-09 test standard and performance criteria A defined in Annex B of CISPR 24.

5.1.13 Surge Immunity

The power supply shall be tested with the system for immunity to AC Unidirectional wave as shown in the table below per EN 55024: 1998/A1: 2001/A2: 2003, EN 61000-4-5: Edition 1.1:2001-04.

The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.

Table 5-8 Surge immunity requirements

Condition	Surge immunity
Line to ground	3kV
Line to line	2kV
Line to ground (tested for design margin)	3.5kV
Line to line (tested for design margin)	2.5kV

Notes: Margin test shall be conducted only during development

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-5: Edition 1.1:2001-04 test standard and performance criteria B defined in Annex B of CISPR 24.

5.1.14 Voltage Interruptions

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-11: Second Edition: 2004-03 test standard and performance criteria C defined in Annex B of CISPR 24.

5.1.15 Power Recovery

The power supply shall recover automatically after an AC/DC power failure. AC/DC power failure is defined to be any loss of AC power that exceeds the dropout criteria stated in section *5.1.5 Line Dropout/Holdup*.

Although the power supply may power off under conditions described in this section, it must be capable of restarting, either automatically or under program control after the disturbance. In addition, the power supply should not be in a latched state such that any of the operator buttons/switches do not operate correctly after the disturbance. At no time should the AC/DC power cord have to be removed to clear an error condition.

Auto restart conditions are tested from –40% to –100% Input under voltage conditions for time intervals ranging from 25ms to 2 seconds.

These tests are performed at both the lowest and highest nominal operating voltages of the power supply. Time intervals: 25ms, 40ms, 60ms, 90ms, 130ms, 200ms, 280ms, 400ms, 600ms, 900ms, 1.3s, and 2.0s

Under voltage deviation from nominal AC voltage: -40%, -50%, -60%, -70%, -80%, -90%, -100% In a temporary AC input power outage situation (dropout/brownout/blackout), the power supply will be able to automatically restart under any load, once the PSON# signal is asserted LOW. This is true even under a condition such as the PSON# signal de-asserts (HIGH) and then asserts (LOW) during the temporary power outage period. This toggling of the PSON# signal can happen at any interval and may repeat during the temporary power outage period.

5.2 Low Voltage +54VDC Input Requirements (Rack Power Input)

5.2.1 Inlet Connector

The power supply shall have a 100A power blade type connector model TBD.

5.2.2 Input Voltage Specification

The power supply must be able to operate normally with 240VDC input.
- Operating range: 40 VDC to 60 VDC
- PMBus commands must function normally
- Power timing requirements met during power cycling
- LED functioning correctly
- In Always Standby mode in a 1+1 PSU configuration the active PSU will have >95% load, the Standby PSU will have <5% load
- In 1+1 PSU configuration and one PSU Active and the other in Always Standby mode; if the Active PSU fails the Standby PSU must support the load to maintain output voltage > 11.20V. Tested with 2,200uF 12V capacitance.
- turn ON input voltage: TBD / TBD (MIN/MAX)
- turn OFF input voltage: TBD / TBD (MIN/MAX)

Table 5-9 +54VDC input voltage specification

PARAMETER	MIN	Typical	V_{MAX}	Startup VAC[2]	Power Off VAC[2]
Steady state voltage	40 V_{DC}	54 V_{DC}	60 V_{DC}	TBD	TBD
Transient state voltage	40 V_{DC}	54 V_{DC}	60 V_{DC}	NA	NA

5.2.3 Fuse

Input fusing shall be provided at the input of the PSU.

5.2.4   Inrush Current

The power supply input inrush current shall be less than TBD at input insertion and shall not cause arcing. Hot swap/inrush controller MOSFET shall be used to avoid arcing at insertion. Capacitors in front of Hot Swap Controller shall be avoided. Sense +/- (short pins in the input connector) shall be used to turn ON/OFF the Hot Swap Controller (Inrush switch MOSFETs) to avoid arcing during the insertion and extraction operations.

5.2.5   Transients Requirements

Voltage transitions could take place when the power source transitions from/to the backup power. The input power circuitry must be fully functional during the input voltage transitions, i.e., the input capacitor should be sized properly, and the hot swap controller protection levels should be set correctly to avoid protection tripping during voltage transitions. The maximum voltage slew rate during the transitions is listed below:

Table 5-10 Maximum voltage slew rate during input transient events.

PARAMETER	Slew rate (V/ms)
Ramp up rate	30
Ramp down rate	10

5.2.6   Susceptibility Requirements

To be defined.

5.2.7   Input Dropout/Holdup

5.2.7.1   Main output

A DC input dropout is defined to be when the DC input drops to $0V_{DC}$ for any length of time. During an DC dropout the power supply must meet dynamic voltage regulation requirements. A DC input dropout of any duration shall not cause tripping of control signals or protection circuits other than the SMBAlert# signal. If the DC dropout lasts longer than the specified holdup time in *Table 5-11 +54VDC input power supply holdup / dropout* below the power supply should recover and meet all turn ON requirements. The power supply shall meet the DC dropout requirement overrated DC voltages. A dropout of the DC input for any duration shall not cause damage to the power supply.

Table 5-11 +54VDC input power supply holdup / dropout

Loading during AC/DC dropout / holdup	Minimum Holdup time / Dropout duration[1]
0% to 100% of rated load	1msec

Notes:
1. This must be proven by calculation using the worst capacitance tolerance, variance with temperature and bus voltage. It shall be tested with a bulk capacitor having the minimum capacitance tolerance, at worst case loading and at worst case DC voltage conditions.

5.2.7.2   Auxiliary (Stand-by) Output

Not applicant for this type of power supplies.

5.2.8   Input Ripple Voltage

To be defined.

5.2.9   Isolation Requirements

Isolation between input and output is not required in this type of power supply.

5.3   Low Voltage -48VDC Input Requirements (Telecom)

This type of power supply is intended to be in a Telecom environment, due to this compliance with NEBS specifications are be required, please see *Section 14.5 Telecommunications DC Mains Powered Power Supplies*.

5.3.1   Inlet Connector

To be defined.

5.3.2   Input Voltage Specification – Note: Include Ripple

Table 5-12 -48VDC power supply Input voltage range

PARAMETER	MIN	RATED	V_{MAX}	Startup VDC	Power Off VDC
Voltage (-48 V_{DC})	-48 V_{DC}	-48 V_{DC} – -60 V_{DC}	-72 V_{DC}	-38 V_{DC} – 40 V_{DC}	-37 V_{DC} – -39 V_{DC}
Hysteresis				1V	1V

5.3.3   Minimum Input Inductance

The power supply shall have a minimum input inductance (*Lin*) specified in TABLE below when operating with a voltage range defined in *Table 5-12 -48VDC power supply Input voltage range.*

Table 5-13 Minimum input inductance for -48VDC input power supplies

PARAMETER	MIN
Input inductance (*Lin*)	11mH/kW

> **Note:** The recommended approach to determine the input inductance (*Lin*) of the power supply is show below in *Supplemental Material LDC input impedance measurement procedure.*

Recommended approach to determine the input inductance (*Lin*) of the PSU is show below.

5.3.4   Input Impedance

5.3.5   Fuse

The power supply must have internal primary over current protection. A fuse type acceptable for all safety agencies' requirements and utilizing high-breaking-capacity must be placed in the input circuit. The fuse is not to be considered replaceable for the purposes of determining power supply reliability and life as specified in *Section 13 Reliability.* The fuse shall not open in any transient condition but only in an internal failure of the power supply.

5.3.6   Reversed Polarity Protection

Reversed polarity protection is required for a -48VDC input Telecom power supply.

5.3.7   Input dv/dt

The PSU while operating on a DC input shall be able to sustain a dv/dt defined in *Table 5-14 Input dv/dt during* Turn-On and Turn-Off and during input line transients including input voltage sags and surges. The value of dv/dt should be guaranteed by design (by including data on dv/dt and di/dt of all components exposed to input dv/dt).

Table 5-14 Input dv/dt

Parameter	Max
Input dv/dt	10 V/us

5.3.8   Input Ripple Voltage

While operating on a DC input, the maximum ripple voltage on the input bus (generated from the source & infrastructure) shall be 1% peak-peak of the operating voltage as measured at the PSU terminals. The frequency of the input ripple voltage is 94 Hz - 126Hz. The PSU should consider this ripple as normal operating range, if the ripple is outside this range the performance may be de-graded. If the PSU continues to operate outside the range, it should operate safely.

5.3.9   Input Reflected Ripple Current

While operating on DC Input, the pk-pk ripple current as seen on the PSU input from 10% load to 100% load shall be less than 10% of the maximum DC Input Current specified in the Design Specification for individual PSU, at loads below 10%, the value is 30% of the maximum DC Input Current specified in the Design Specification for individual PSU with input ripple voltage defined above.

The Input Current ripple will be measured with scope bandwidth limited to 1 MHz.

5.3.10   Surge Immunity

Compliance with NEBS specification is required. see *Section 14.5 Telecommunications DC Mains Powered Power Supplies* for more details.

5.3.11   Inrush Current

For power supplies used in telecommunication applications (operating on -48VDC nominal), the Initial Inrush, secondary Inrush and Re-Rush current the ratio of the instantaneous inrush current It to maximum steady state current *Im* at interface "A", when the switch is closed within the normal service voltage range, shall not exceed the limits shown in *Figure 5-7 I vs T Profile for -48VDC Input power supply at nominal voltage and maximum load.*

The parameters are defined as follows:

- *It*: inrush current (magnitude of instantaneous value).

- **Im:** maximum steady state input current for a fully equipped equipment under test connected to interface "A", at nominal voltage.

The power generator for Inrush current test shall be in accordance with CENELEC EN 61000-4-29. Performance criteria:

- Below 0.1 ms, the inrush current is not defined.
- Below 0.9 ms the **It/Im** ratio shall be lower than 48.
- Above 1 ms: the curve corresponds to the maximum tripping limit of majority of existing protective devices.

Maximum inrush current characteristics for Telecommunications and Datacom (ICT) equipment at nominal voltage and maximum load:
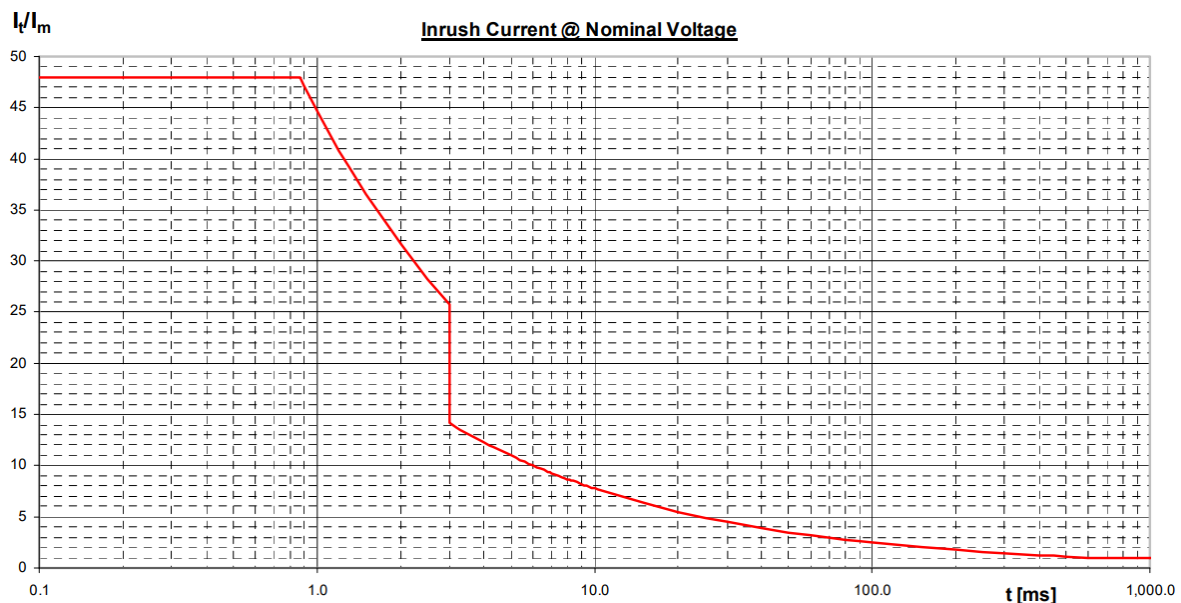
Figure 5-7 I vs T Profile for -48VDC Input power supply at nominal voltage and maximum load

Note: Refer to ETSI EN 300 132-2 V2.5.1 (2016-10) for measurement set-up.

6 Efficiency

6.1.1 High Voltage AC/DC Input Power Supplies

The power supply shall be tested for efficiency to meet efficiency levels of www.80plus.com for 230V Internal power supplies. There is a link to the testing protocol here; Generalized Test Protocol for Calculating the Energy Efficiency of Internal Ac-Dc and Dc-Dc Power Supplies revision 6.7. Output shall be load according to the proportional loading method defined by 80 Plus in Generalized Internal Power Supply Efficiency Testing Protocol Rev 6.7. In these testing requirements the power supply is tested at 230VAC/60Hz input and does not include the losses of the PSU fan.

6.1.1.1 240VAC/240VDC and Wide Input Range

Table 6-1 Efficiency requirements for 240VAC/240VDC and wide input range power supplies

Loading	100% of maximum	50% of maximum	20% of maximum	10% of maximum
Titanium efficiency for PSUs equal or beyond 2500W	94%	96%	94%	90%
Titanium efficiency for PSUs below 2500W	91%	96%	94%	90%
Platinum efficiency	91%	94%	90%	85%

6.1.1.2 277VAC/380VDC Input

Table 6-2 Efficiency requirements for 277VAC/380VDC power supplies

Loading	100% of maximum	50% of maximum	20% of maximum	10% of maximum
Titanium efficiency for PSUs equal or beyond 2500W[1]	94%	96%	94%	90%
Titanium efficiency for PSUs below 2500W	91%	96%	94%	90%
Platinum efficiency	91%	94%	90%	85%

Notes:
1. Titanium efficiency certificate is required for 380VDC input power supplies.

6.1.2 Low Voltage DC Input Power Supplies

The subsections provide the required minimum efficiency levels at various loading conditions power supplies for low input voltage. These are provided at different load levels; 100%, 50%, 20%, and 10%.

6.1.2.1 +54VDC Input

Table 6-3 Efficiency requirements for +54VDC input power supplies

100% of maximum	50% of maximum	20% of maximum	10% of maximum
95%	96%	94%	90%

Notes:
2. Tested at +51VDC and +54VDC.
3. Efficiency test shall be conducted excluding the losses of the PSU fan

6.1.2.2 -48VDC Input (Telecom)

Table 6-4 Efficiency requirements for -48VDC (Telecom) input power supplies

100% of maximum	50% of maximum	20% of maximum	10% of maximum
91%	94%	90%	85%

Notes:
1. Tested at -48VDC.
2. Efficiency test shall be conducted excluding the losses of the PSU fan

7 Output Requirements

7.1 Output Power/Currents

The following tables define the minimum power and current ratings. The power supply must meet both static and dynamic voltage regulation requirements for all conditions.

Table 7-1 Load requirements

Output	Input voltage (VAC)	Min. (A)	PL1 Max. Continuous[4] (A)	PL2 CLST Peak 20sec duration [2] (%)	PL3 Peak 10msec duration [3] (%)	PL4 Peak 100μsec duration (%)
12V main	200-240	0.0	PSU rating	115%	155%	165%
12V main (wide input range)	90-264	0.0	PSU rating	115%	155%	165%
12VSB [1]	100-240	0.0	3.0	113%	NA	NA

Notes:
1. 12VSB must provide 6.0A with two power supplies in parallel. The Fan may work when Standby current >1.5A and the ambient temperature is higher than 35C.
2. CLST Peak load duration is based on thermal sensor and assertion of the SMBAlert# signal. Minimum peak power duration shall be 20 seconds without asserting the SMBAlert# signal at maximum operating temperature.
3. PL3 peak duty cycle shall be 25%; 4msec at PL3 / 12msec at CLST Peak. Applying a PL3 peak load must not trip the SMBAlert# signal. The maximum length of time the PL3 peak must be supported is based on the SMBAlert# signal asserting. The PSU must support this peak load for 5msec after SMBAlert# asserts.
4. When applying a repetitive or non-repetitive transient load profile, the effective Iavg load must never exceed the maximum current rating as stated on PL1.
5. Refer to *Section 8.1.2 Averaging Mechanism* for more details about the averaging algorithm, accuracy, and timing.
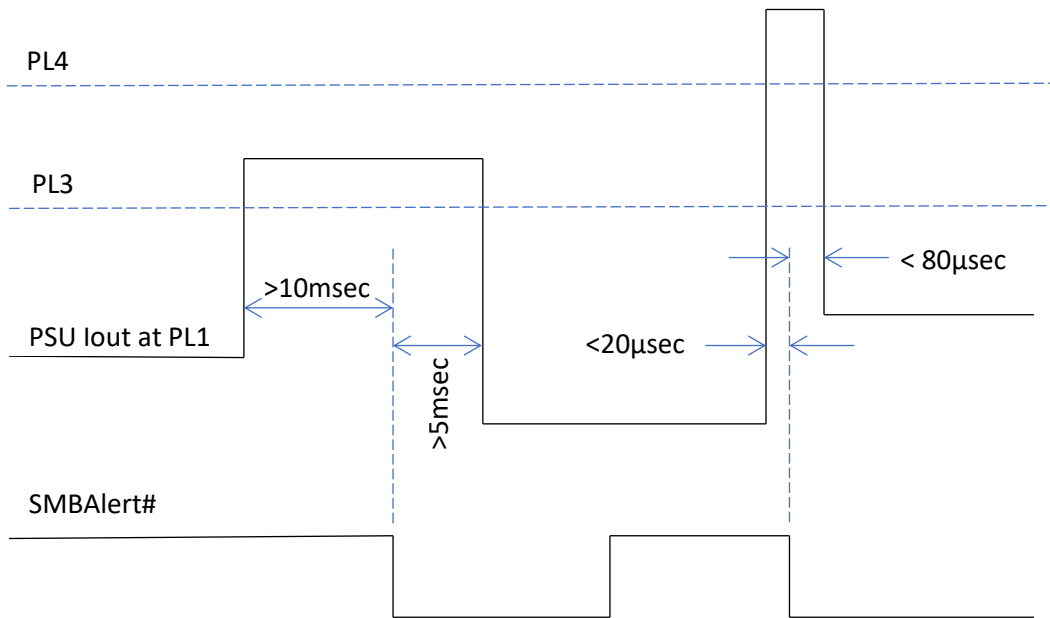
Figure 7-1 PSU Peak power timing example

7.2   Peak Load Protection

For peak loads above the PL3 peak load level the PSU may assert the SMBAlert# signal to shorten the duration of the peak load to < 100μsec. For peak loads up to PL3 peak load level the PSU must not assert SMBAert# if the peak load duration is <10msec. If the peak load last longer than 10msec the PSU may assert SMBAlert# to throttle the load within 15msec. Below are PSU requirements for peak load conditions.

Table 7-2 Peak load protection testing conditions

Peak Load	Peak current	System capacitance	SMBAlert# timing	Peak load duration	Voltage undershoot
PL4	Rated + 169 A	6 x 1,500μF	< 20μsec	100μsec	-2%

7.3   Auxiliary (Stand-by) Output

The 12VSB output shall be present when an AC input greater than the power supply turn on voltage is applied. There should be load sharing in the standby rail.

7.4   Voltage Regulation

The power supply output voltages must stay within the following voltage limits when operating at steady state, for dynamic conditions see section *7.5 Dynamic Loading*. These limits include the peak-peak ripple/noise. These shall be measured at the output connectors.

Table 7-3 Voltage regulation limits

Parameter	Min.	Nom.	Max.	Units
+12V[1]	+12.11	+12.20	+12.29	V_{RMS}
+12V SB	+11.40	+12.00	+12.60	V_{RMS}

Notes:

1. Output voltage set point when the PSU is standalone shall be 12.2V +-30mV at 50% loading condition and vary from 12.25V +-30mV at 5% loading condition to 12.15V +-30mV at 95% loading condition measured at the mating connector. The droop bandwidth shall be equivalent to the +12Vmain voltage regulation loop.

7.5 Dynamic Loading

The output voltages shall remain within limits specified for the step loading and capacitive loading specified in the table below. The load transient repetition rate shall be tested between 50Hz and 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the Peak load conditions.

Table 7-4 Transient load requirements

Output	Δ Step Load Size	Load Slew Rate	Test capacitive Load[3]	Regulation limits
+12V	100% of max load[1]	2.5 A/µsec	3,300µF	12V -8% / +8%
+12V	70% of max load	2.5A/µsec	3,300µF	12V -5% / +5%
+12V	60% of max load[2]	2.5 A/µsec	1,000 µF	12V - 7% / +7%
+12V	60% of max load[2]	2.5 A/µsec	1x 2,200 µF	12V - 6% / +6%
+12V	60% of max load[2]	2.5 A/µsec	3x 2,200 µF	12V - 5% / +5%
+12VSB	1.0A	0.5 A/µsec	1,000 µF	12V -8% / +8%

Notes:

1. For 100% step dynamic condition it shall be tested from 5% to 105% loading.
2. For step loading condition +12V minimum loading is 5A and can be anywhere between 5A to max load.
3. The capacitor type used for this test shall be Aluminum Electrolytic.

Additionally, the power supply shall support the transient conditions stated in below table.

Table 7-5 Additional transient load requirements

Profile	Starting Load		End Load		Step Size %	Frequency Hz	Duty Cycle %	Load Slew Rate A/us
	%	Mode	%	Mode				
A	70	CC	170	CC	100	100	20	2.5
B	85	CR	170	CC	85	40	8	2.5
C	90	CC	140	CC	50	40	20	2.5
D	63	CR	151	CC	88	28	40	2.5
E	2	CC	52	CC	50	50	50	2.5
F	5	CC	105	CC	100	50	50	2.5
G	0	CC	50	CC	50	50	50	2.5

Notes:

1. CC = Constant Current, CR = Constant Resistance.

7.6   Capacitive Loading

The power supply shall be stable and meet all requirements with the following capacitive loading ranges.

Table 7-6 Capacitive loading conditions

Output	MIN	MAX	Units
+12VSB	270	4,700	µF
+12V	2,000	70,000	µF

Notes:
1. The minimum capacitive load on 12V output is required to hold regulation during Cold Redundancy mode PSU failures and PSU hot swapping.

7.7   Grounding

The output ground of the pins of the power supply provides the output power return path. The output connector ground pins shall be connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 1.0 mΩ. This path may be used to carry DC current.

7.8   Closed Loop Stability

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges specified in Section 4.6. A minimum of 45 degrees phase margin and -10dB-gain margin over temperature is required using 0mF and 5mF of capacitance, in addition the test shall be performed with 70mF for exploratory purposes. The power supply manufacturer shall provide proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at 0%, 10%, 25%, 50% and 100% loading conditions the maximum and minimum loads as applicable. A gain of 20dB is required at 100Hz and 120Hz for each one of the capacitances and loading conditions.

Table 7-7 Phase and gain margin requirements

Capacitance[1]	Load	Phase margin	Gain margin
0µF/5000µF	0%, 10%, 25%, 50% and 100%	45º	-10dB
70,000µF	0%, 10%, 25%, 50% and 100%	Characterization	Characterization

Notes:
1. The capacitor type used for this test shall be Aluminum Electrolytic.

7.9   Residual Voltage Immunity in Standby Mode

The power supply should be immune to any residual voltage placed on its outputs (Typically a leakage voltage through the system from standby output) up to 500mV. There shall be no additional heat generated, nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on.

The residual voltage at the power supply outputs for no load condition shall not exceed 100mV when AC voltage is applied and the PSON# signal is de-asserted.

7.10 Soft Starting

The Power Supply shall contain control circuit which provides monotonic soft start for its outputs without overstress of the AC line or any power supply components at any specified AC line or load conditions.

7.11 Zero Load Stability

When the power subsystem operates in a no-load condition, it does not need to meet the output regulation specification, but it must operate without any tripping of over-voltage or other fault circuitry. When the power subsystem is subsequently loaded, it must begin to regulate and source current without fault.

7.12 Hot Swap

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply shall use a latching mechanism to prevent insertion and extraction of the power supply when the AC power cord is inserted into the power supply.

> **Note:** +54VDC input power supplies do not have hot swap capability due to the usage model.

7.13 Forced Load Sharing

The +12V output will have active load sharing using average plus droop control methods. The output shall share within <2% at full load. The failure of a power supply should not affect the load sharing or output voltages of the other supplies still operating. The supplies must be able to load share in parallel and operate in a hot swap / redundant 1+1, 2+1, 3+1 and 2+2 configurations. The 12VSB output is required to actively share current between power supplies (droop control). The 12VSB output of the power supplies are connected in the system so that a failure or hot swap of a redundant power supply does not cause these outputs to go out of regulation in the system.

The Ishare bus signal shall have a voltage setting of 5V at full load to accommodate a dynamic range of up to 10V for a 2x rated current measurement.

7.13.1 Current Share (Ishare)

The requirements for the Ishare signal are listed below.

- Vishare Output Accuracy: +/-0.5% of full scale plus +/-0.5% of reading.

- Vishare Output Bandwidth: 1 kHz +/-5%.
- Current Sharing method: Voltage Droop + Active Average.
- Current Sharing Accuracy: +/-2% individual PSU relative to total average (sample averaged over 20ms moving window for 500ms after change in load). The accuracy shall be based on the highest rating of the PSU (irrespective of at what input voltage range the PSU is operating).
- Output Voltage Adjusting Range/Clamping due to Current Sharing loop: +/-200 mV with +/-5% tolerance.
- Output Voltage Adjusting Resolution due to Current Sharing loop: <1mV, to cover low impedance Power Distribution Boards.

Table 7-8 Additional Requirements on current share behavior

Parameter	Value	Remarks
Gain at 1Hz	> 25dB	All parameters validated by Test at each stage during development using inter PSU board as 800µΩ (±10%). In addition, all parameters to be verified by calculation / simulation based in inter PSU impedance
Cross Over Frequency	100Hz (±5Hz)	
Gain Margin	-12dB	
Phase Margin	90 Degrees	
Output Clamp	+200mV (±10mV) / -200mV (±10mV)	
Vishare Ripple Note 1	50mV pk-pk	
Transient test for Load Step (Applicable load steps up to 100% for the defined profiles)	Settling Time (settling within +/-2% of final value) ≤ 10ms	
Response - Vishare_error (1V step) to 12Vmain	Settling Time (settling within +/-2% of final value) ≤ TBD	

Notes:

1. Vishare ripple to be measured with BW limited to 10 kHz measured with single PSU. This specification limit is not applicable when more than one PSU is sharing load.

The following figure depicts the implementation of the average current share mechanism.
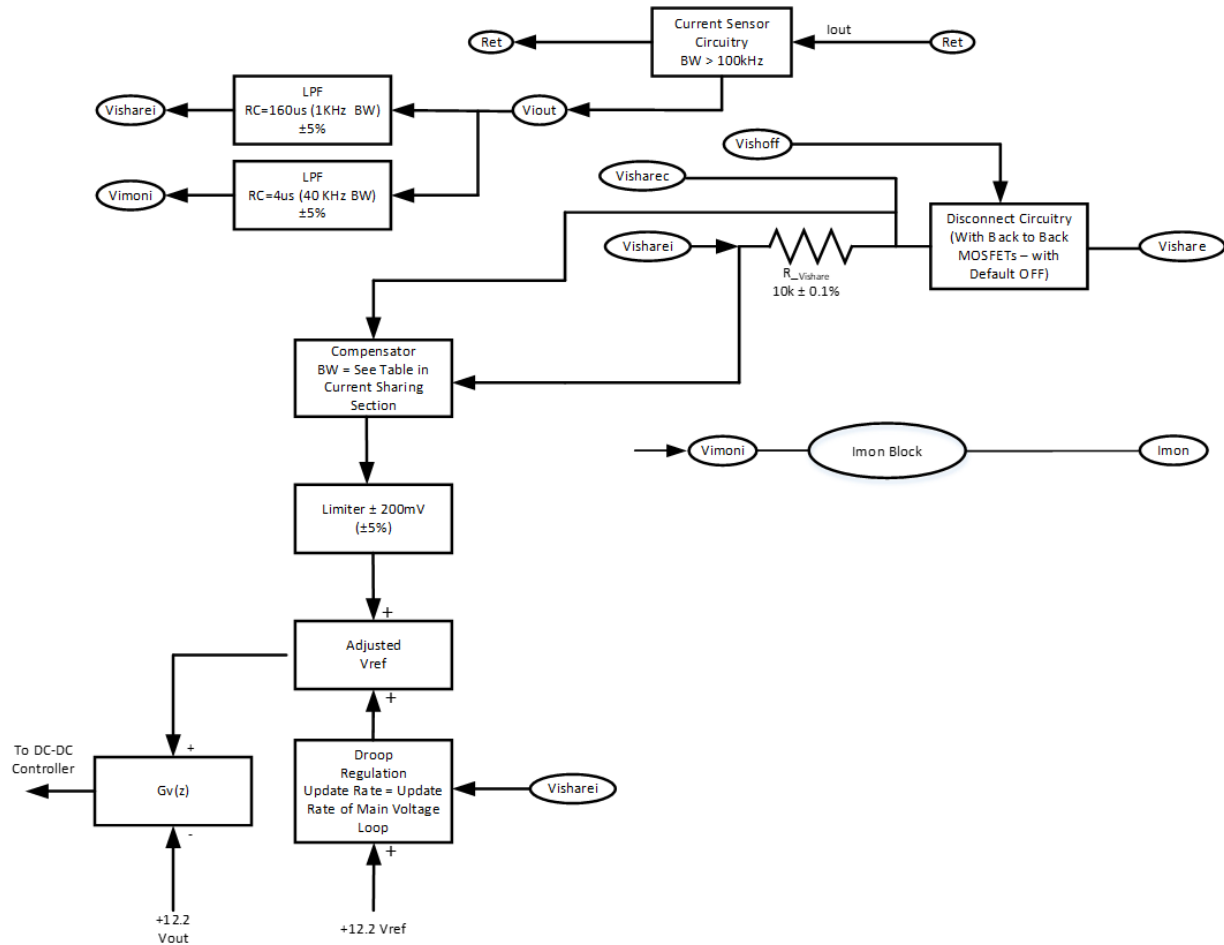
Figure 7-2 Digital control implementation of average current mode control

Iout to Vimoni

Scale: 10V @ 200% Rated Capacity

DC Accuracy: ±1% of full scale plus ±1% of reading

Time Constant: 4us (40 kHz BW) ±5%

Signal Delay: <100ns

Iout to Visharei

Scale: 10V @ 200% Rated Capacity

DC Accuracy: ±0.5% of full scale plus ±0.5% of reading

Time Constant: 160us (1 kHz BW) ±5%

Signal Delay: = 30us ±5%

Implementation Considerations:

The voltage across R-Vishare should be detected by an analog differential amplifier. Feeding directly the two signals into an A/D converter and process the signal digitally requires 8-10 bits resolution for the Ishare error and would require 12-bit or more resolution for direct A/D measurements of Vishare external and internal.

Limiter should be implemented with an analog circuit, so the A/D converter will receive a delta signal of 200mV only, so an 8–10-bit converter can be used.

The converter voltage regulation loop must have the capability of adjusting the output voltage with a resolution better than 1mV for proper current sharing operation with low impedance between the PSUs. This would equate to minimum 14-bit resolution out of the 12.2V output. Depending on details of Voltage Regulation loop implementation this might require 12.2V out and 12.2V ref to be represented in the MCU calculation as 14–16-bit numbers.

Notes:
1. Time Constant is defined as the time it takes for the signal to reach 63.2% of the signal step.
2. In *Figure 7-2 Digital control implementation of average current mode control* above, at any point of this compensator, the value should not exceed +/- 200mV (anti-windup).

7.13.2 Main Output Voltage Regulation Droop

The main output voltage will have a droop characteristic. Droop is set at 100mV for 5%-95% of rated load (1.111mv / 1% load). A standalone PSU will have the output voltage factory set at 12.20V +/-12.5mV. A standalone PSU will have a voltage drop of 100mV with a load change from 5% to 95%, voltage measured on the PDB's mating power connector. Bandwidth for the droop shall be equivalent to the main rail voltage regulation loop. For load transients in an "N" PSU in parallel system, the output voltage must stay within Dynamic Regulation band.

7.13.3 Current Sharing Load Step Response

Maximum 20% current deviation from the ideal value, recovering within 4% of the ideal value within 5ms.

7.13.4 Current Share with Margining

PSU shall meet all Current Share requirements (including current sharing load step response) when Margin is enabled. For test purposes, Margin should be enabled before stating the load step. This requirement is applicable only when margin is enabled on all PSUs sharing the load. In case when margin on one or more PSUs operating in parallel is not enabled (PSUs are mis-matched in margin function), PSU/s shall not shutdown under any load profile (either steady stare or transient load) defined in the specification and will support a load which within the defined boundary of PSU Load vs Timing Behavior. In such cases PSUs can operate in Constant Current mode to keep supporting the load.

7.13.5 Current Share Activation

Average Current Sharing must be activated within 10ms from the PWOK signal being asserted   .
Current Sharing loop could be deactivated if the PSU output current is below 5% or if the current unbalance (PSU versus total load average) is below 1%

7.13.6 Ishare Disconnect Circuitry

Disconnect circuit ON resistance < 50 Ohm. The disconnect circuit should be configured with 2 Back-to-Back MOSFETs.

7.13.7 Concurrent Maintenance

This power supply will be designed to be "hot plugged/removed". No faults will be generated in the functioning units, or the system, during removal or insertion of a power supply. Output voltages must remain within regulation limits on either insertion or extraction. No damage should occur to either the operating or non-operating power supply.

A fault (UVP, OTP and short-circuit except OVP) within one power supply while running (synch FET, output cap, etc.) shall not cause output voltage of the system/common bus voltage to go outside regulation limits. If the current sharing is disabled by shorting the current share bus to ground, the power system must continue to operate within regulation limits for loads less than or equal to one power supply.

When VINOK# has been de-asserted and the power supply is shutting down due to the loss of AC/DC input, the output's OR'ing FETs must be turned OFF when the secondary main converter has turned OFF within 50us of POK de-assertion.

> **Note:** The requests above must be validated during power supply development phase to ensure concurrent maintenance.

7.13.8 Maximum Power Rating with Parallel PSUs

The supplies must be able to current share with any combination from 1 to 6 PSUs in the system. Maximum Output Power for systems with "n" PSU of "W" power each, in parallel: 1*W +0.95*(n-1)*W.

Figure 7-3 Number of power supplies in parallel vs. maximum system power rating

PSU SKUs	Number of Supplies	Maximum System Power Rating
1+0	1	100% of One PSU Rating
1+1	2	100% of One PSU Rating
2+0	2	100%+(95% x 1) x PSU Rating
2+1	3	100%+(95% x 1) x PSU Rating
2+2	4	100%+(95% x 1) x PSU Rating
3+0	3	100%+(95% x 2) x PSU Rating
3+1	4	100%+(95% x 2) x PSU Rating
3+2	5	100%+(95% x 2) x PSU Rating
3+3	6	100%+(95% x 2) x PSU Rating

7.13.9 Current Share Signal Characteristics

This current sharing section is a proposed method for achieving load sharing compatibility between different manufacturer's power supplies. This section may be updated based on information gathered during testing and other investigations to make it a reliable set of requirements. Descriptions of the voltage and current share loop stability are shown below.

Item	Description	Min	Nom	Max	Units
Ishare sink. Ishare =10V	Amount of current the load share bus of each power supply sinks.	-	-	1.5	mA
Ishare source. Ishare =10V	Amount of current the load share bus of each power supply sources.	-	-	1.5	mA
T_{ss}	Soft start of current sharing loop, count from output voltage is rising to its 90% voltage rating	-	50	100	msec

T_{Ishare}	Delay from PSU1 reaching 90% of its nominal voltage to PSU1, 2 Currents settling within Current Share Specification.	-	-	150	msec
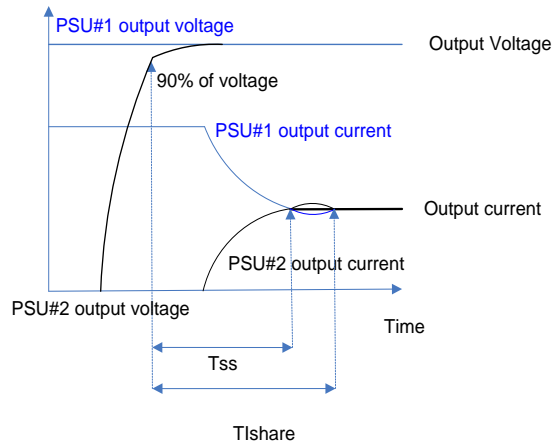
Figure 7-4 TSS and TIshare timing

7.14 Ripple/Noise

The maximum allowed ripple/noise output of the power supply is defined in *Table 7-9 Ripple and noise* below. This is measured over a bandwidth of 10Hz to 20MHz at the power supply output connectors. A 10µF in parallel with a 0.1µF ceramic capacitor is placed at the point of measurement. To help reduce switching ripple further, an additional 2,200µF low ESR electrolytic capacitor may be placed in parallel.

Table 7-9 Ripple and noise

+12V main	+12VSB
120mVp-p	120mVp-p

The test set-up shall be as shown below.
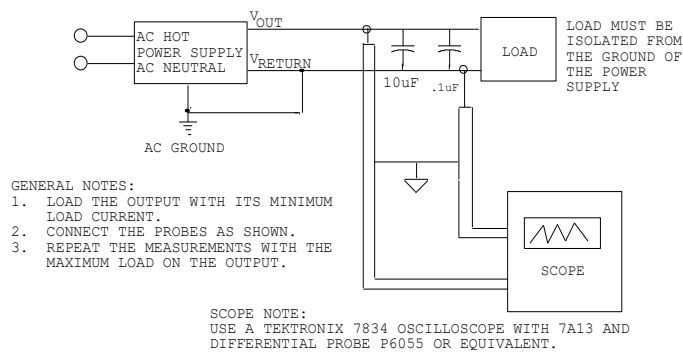
Figure 7-5 Differential noise test setup

Note: When performing this test, the probe clips and capacitors should be located close to the load.

7.15 Timing Requirements

This section describes the timing requirements for the power supply operation. All outputs must rise monotonically. Table below shows the timing requirements for the power supply being turned ON and OFF in two different ways; 1) via the AC/DC input with PSON# signal held low; 2) via the PSON# signal with the AC/DC input applied.

Table 7-10 Timing requirements

Item	Description	MIN	MAX	Units
Tvout_rise	Output voltage rise time for 12V and 12VSB from 10% to within regulation limits.	10	70	ms
Toff_latch[2]	This is the time the PSU must stay off when being powered off with loss of AC input. Both outputs must meet this OFF time; 1) whenever PWOK is de-asserted for the 12Vmain output; 2) whenever the 12VSB output drops below regulation limits.	500	1000	ms
Tsb_on_delay	Delay from AC being applied to 12VSBbeing within regulation.		1500	ms
Tac_on_delay	Delay from AC being applied to all output voltages being within regulation.		3000	ms
Tvout_holdup	Time 12Vl output voltage stays within regulation after loss of AC.	11		ms
Tpwok_holdup	Delay from loss of AC to de-assertion of PWOK	10		ms
Tpson_off_delay	Delay from PSON# de-asserted to power supply turning off		5	ms
Tpson_on_delay	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
Tpson_pwok	Delay from PSON# deactivate to PWOK being de-asserted.		5	ms
Tpwok_on	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
Tpwok_off[1]	Delay from PWOK de-asserted to output voltages dropping out of regulation limits.	1	Configurable via PMBus	ms
Tpwok_low	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		ms
Tsb_vout	Delay from 12VSBbeing in regulation to O/Ps being in regulation at AC turn on.	50	1000	ms
T12VSB_holdup	Time the 12VSBoutput voltage stays within regulation after loss of AC.	70		ms
Tvinok_on[3]	Delay from AC being applied to assertion of VINOK		Configurable	ms
Tvinok_off[3]	Time from loss of AC to de-assertion of VIONK		Configurable	ms

Notes:
1. The T_{pwok_holdup} and T_{pwok_off} times are the default values in the PSU when it's being energized, however the system now can configure the warning time stablished by T_{pwok_off} to have a different value please refer to section *7.16 PWOK Signal Timing Requirements*.
2. T_{off_latch} flow diagram is shown in *Figure 7-8 Toff_latch flow diagram.*
3. Additional logic dependencies are described *Figure 7-7 VINOK assertion logic* Below.
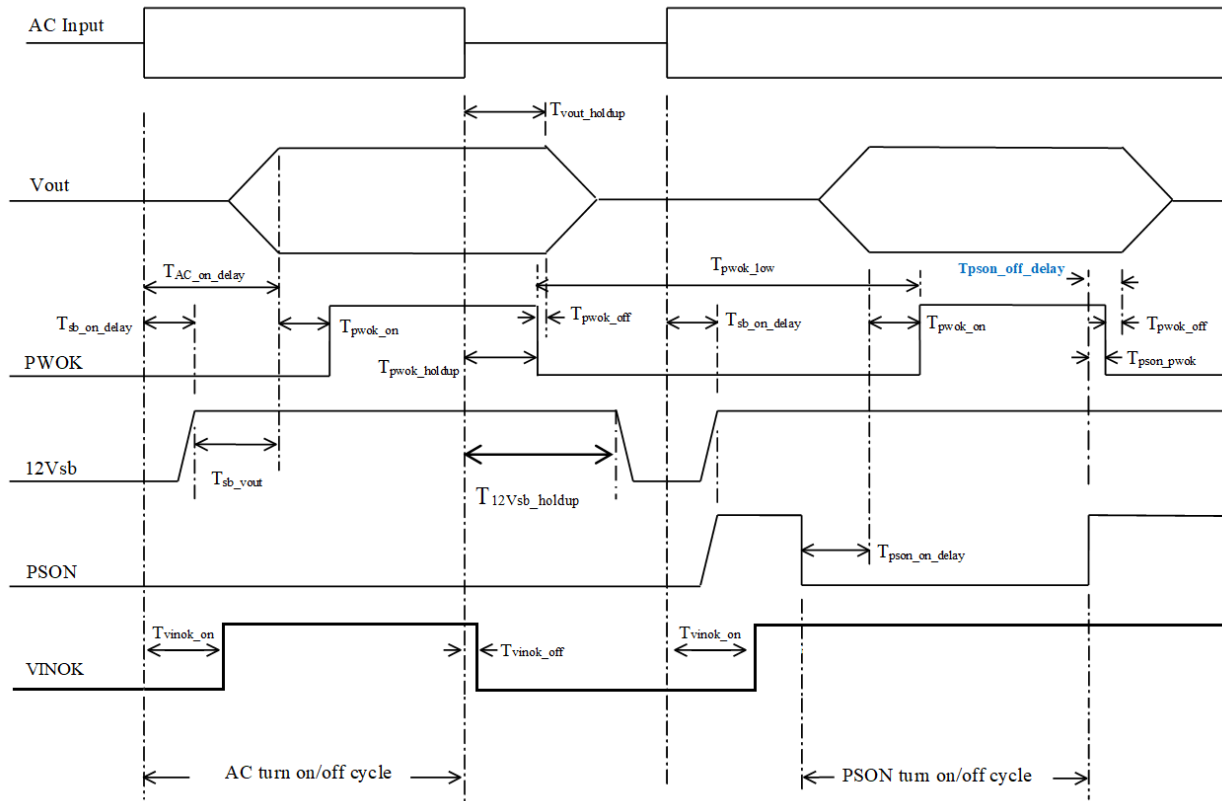
Figure 7-6 Turn ON/OFF Timing (Power Supply Signals)
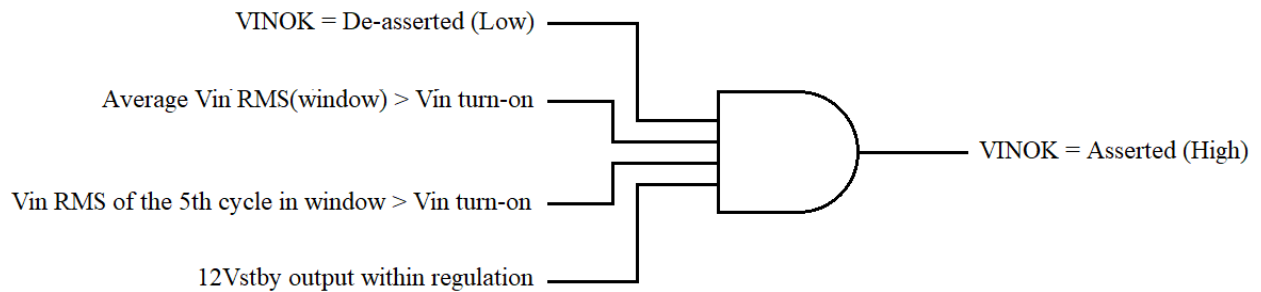
Figure 7-7 VINOK assertion logic

Note: Averaging window can go from 75ms to 120ms depending on the input frequency.
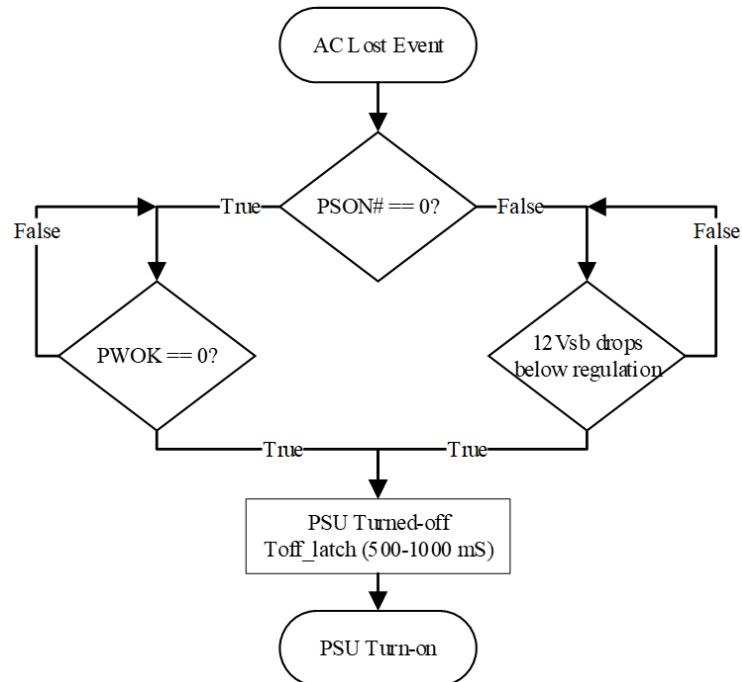
Figure 7-8 Toff_latch flow diagram

7.16 PWOK Signal Timing Requirements

The PWOK signal timing shall be as stated in Table 20. Timing requirements when the power supply is being energized (AC/DC is applied), however the warning time established by T_{pwok_off} shall be configurable via PMBus command MFR_PWOK_WARNING_TIME (F0h) using linear format it is recommended to use 1ms steps and the power supply shall guarantee at least the minimum warning time configured, it is recommended to have a jitter no more than 1.5ms. Figure 8 shows the timing diagram. T_{pwok_off} value shall return to default after an AC/DC input cycle only. The figure below shows the timing diagram. T_{pwok_off} value shall return to default after an AC/DC input cycle only.
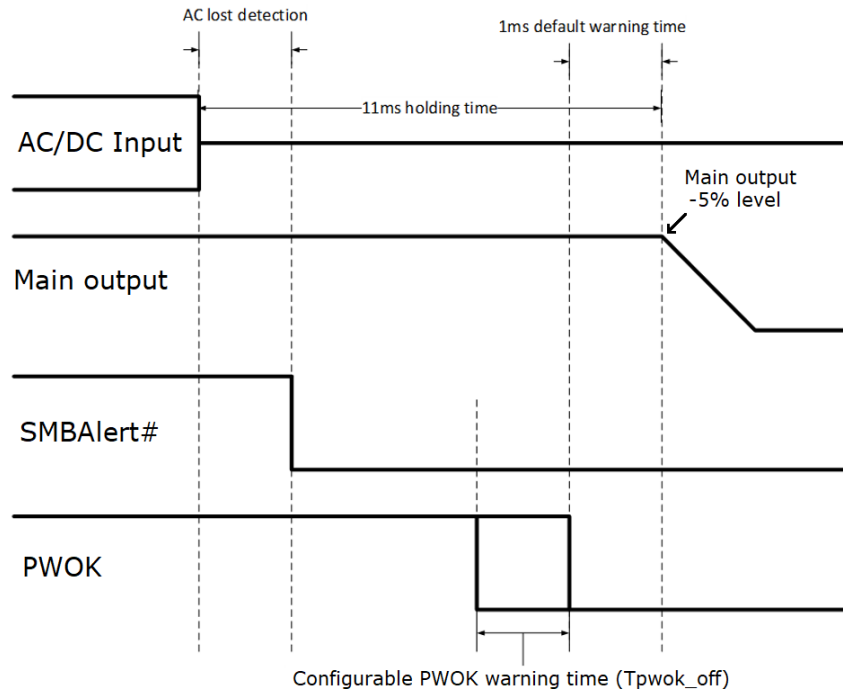
Figure 7-9 Configurable PWOK warning time timing diagram for High voltage power supplies

Note: The main output shall have a slope decay of TBD when going down for up to TBD ms.

8   Protection Circuits

Protection circuits inside the power supply shall cause only the power supply's main outputs to shut down. If the power supply latches OFF due to a protection circuit tripping, an AC/DC input power cycle OFF for 15sec and a PSON# signal cycle HIGH for 1sec shall be able to reset the power supply.

The power supply shall have over current protection (OCP), over current warning (OCW), and overpower protection (OPP) limits as defined in in the subsequent sections. These are defined to protect the PSU and to allow peak currents to power the system without the PSU shutting down.

Fast OCW and Slow OCW levels are defined to assert SMBAlert# to allow the system to throttle power to protect the PSU; but also, to allow peak current to the system without throttling the system.

When OCP trips; it shall shutdown and latch OFF the PSU. This will be cleared only by an AC/DC input power cycle. The power supply shall not be damaged from repeated power cycling in this condition.

PSON# cycling shall NOT reset the over current fault bit or cause the power supply to restart. Only a cycle of the input power shall reset the over current fault bit and allow the PSU to power on again. This is used to protect the system from overheating due to repeated fast power cycling into a faulted short condition in the system.

12VSB will be auto recovered after removing OCP limit (hiccup mode).

8.1 Main Output

8.1.1 Current sense

The PSU shall have the ability to measure output current, which is inclusive of the current delivered by the output filter capacitance within the PSU. The monitored current shall be used, at a minimum, as the input into the constant current, peak detect and overcurrent warning / protection control solution and is available as I_{mon} output from the PSU.
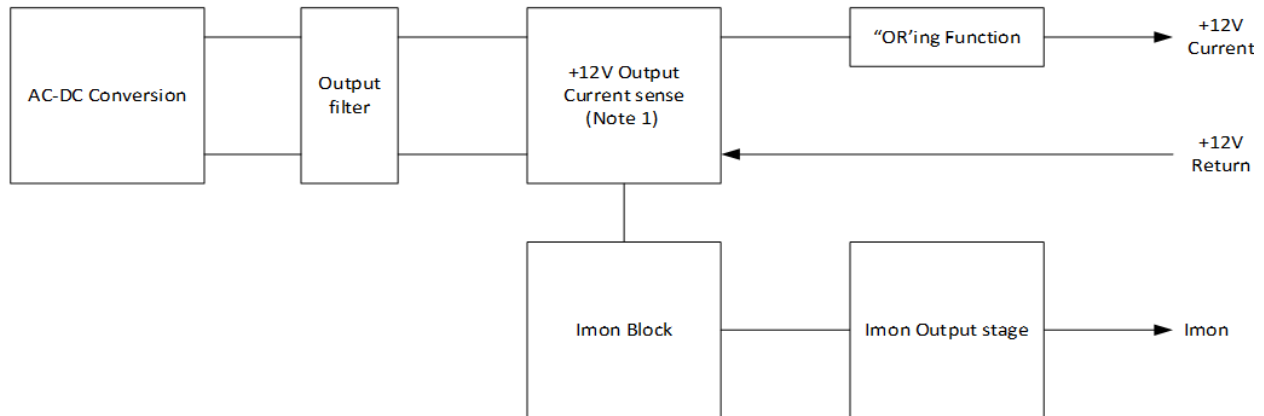
Figure 8-1 Main output current sense block diagram

Notes:
1. Signal or information that represents the +12V main output current. derivation of this signal/information shall be derived via secondary side sensing, post the output filter stage. Current sense element shall be located on the main positive rail.
2. The I_{mon} block and I_{mon} output stage blocks are detailed in *Section 9.5 Imon Output Signal (Output).*

8.1.2 Averaging Mechanism

The power supplies shall have the ability to sample output current and perform a block / window average calculation to support OCW behaviors. Select thresholds shall have the ability to be programmable inclusive of sampling rate and averaging window size. It is required that the PSU uses an average output current value when taking action on applicable OCW behaviors. Refer to *Table 8-2 OCW Thresholds.* The PSU will be required to utilize one sampling rate that will be used across the OCW levels prescribed in this specification.
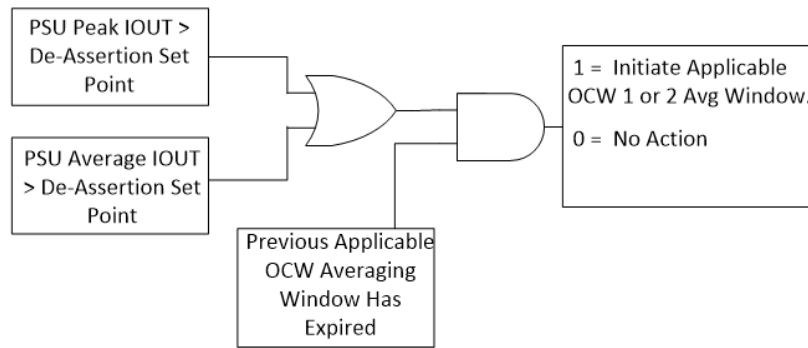
Figure 8-2 OCW1 & OCW2 average window logic
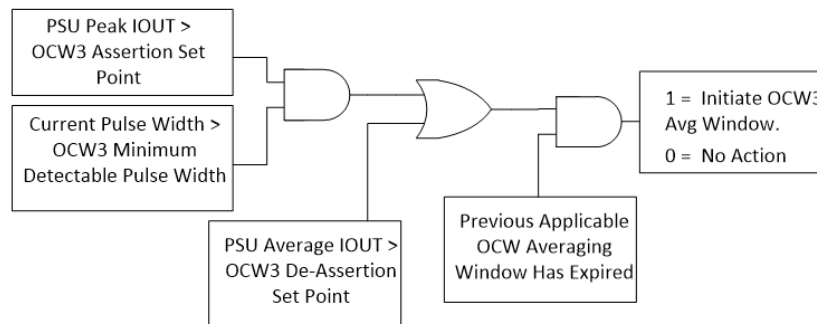
Figure 8-3 OCW3 average window logic

Notes:
3. OCW 1 & 2 Minimum detectable pulse width for averaging window assertion = 40uS ±5us.
4. *OCW 3 Minimum detectable pulse width for averaging window assertion = 20uS.*

8.1.3   Over Current Warning (OCW)

8.1.3.1   Over Current Warning Level 1 (OCW1)

This is a programmable output current warning level intended for maintaining an average PSU load. It is the slower mechanism, compared to that of the peak detects solution of OCW3. The PSU shall use an average output current, derived over a specified time window, to compare against a programmable threshold. This OCW level shall have a hysteresis (refer to *Table 8-2 OCW Thresholds*), between assertion and de-assertion thresholds. The output current averaging window shall start when the PSU (output current) > (hysteresis de-assertion threshold and the previous timer has expired). If the average current exceeds the OCW1 set point, over the specified averaging window, the PSU shall declare an OCW1 event and apply the appropriate logic to SMBAlert#. Please refer to the timing diagrams for OCW1 for further details.

8.1.3.2   Over Current Warning Level 2 (OCW2)

OCW2 is the fixed overcurrent protection threshold. The assertion & de-assertion threshold levels are fixed values. If the average current exceeds the OCW2 assertion set point, over the specified averaging window, the PSU shall declare an OCW2 event and apply the appropriate logic to SMBAlert#. It will then start a 50ms average window. If the average output current continues to remain above the de-assertion threshold, over the specified 50ms average window, the PSU shall shutdown due to overcurrent. In the

case, which OCW2 has been asserted and the average output current < de-assertion threshold over the second (50ms) averaging window, the PSU shall not shut down. The output current averaging window shall start when the (PSU output current) > (OCW2 hysteresis de-assertion threshold and the previous timer has expired).

8.1.3.3   Over Current Warning Level 3 (OCW3)

This warning level is intended to be a high-speed peak output current detection and reporting solution. It shall provide the end system with a rapid response logic signal to declare the PSU output current has exceeded a programmable threshold. The PSU shall declare an OCW3 event based on peak PSU output current, which includes the discharging of the internal PSU output capacitance. The PSU shall use a window averaging method for establishing de-assertion of applicable alert signals. The output current averaging window for de-assertion shall start when the following statement is true:

(PSU output current) > (OCW3 assertion threshold & minimum detectable current pulse width & previous OCW3 window has expired).

Table 8-1 OCW3 Timings

Specification	Description	Min	Typ	Max	Units
OCW3 Detectable Current Pulse Width	Represents the minimum output current pulse that shall be detected by the PSU for OCW3 assertion. Current pulses ≤ the minimum time specified shall not assert an OCW3 event. Output current pulses > than the maximum time specified shall assert an OCW3 event.	20			us
OCW3 Report Time	Report Time represents the time period starting after the minimum detectable PSU output current pulse to the assertion of SMBAlert#.	0		30	us
OCW3 Total Detect + Report Time	The Detection + Report time is measured from the moment the <u>actual</u> PSU output current crosses the assertion level, to the moment the SMBAlert# signal is asserted.	0		55	us
OCW 1-3 PSU Output Current Slew Rate Measurement Location	Represents the output PSU current slew rate measurement location for OCW 1/2/3. It shall be measured directly on the output of the PSU. Please refer to Figure 8-4 PSU Output Current – Slew Rate Measurement.	0.2		2.5	A/us
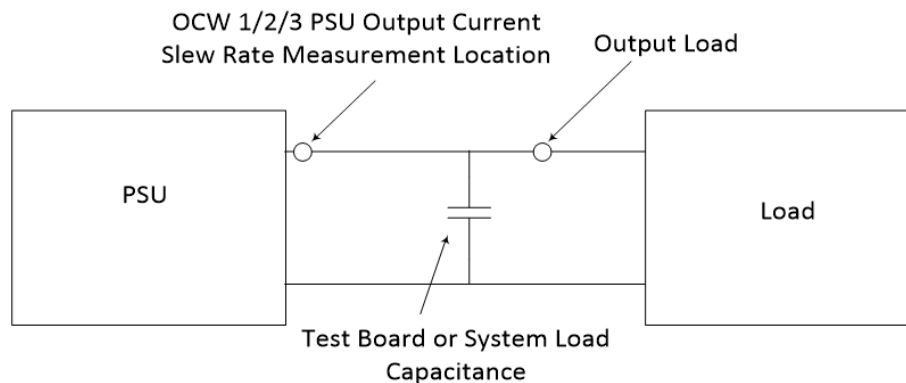
Figure 8-4 PSU Output Current – Slew Rate Measurement
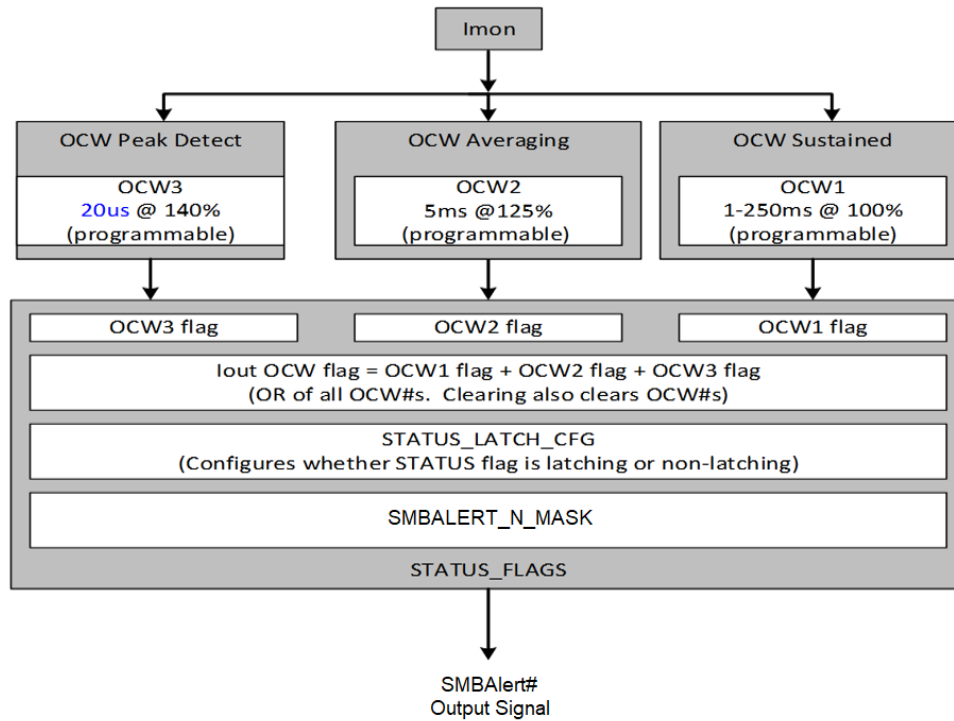
Figure 8-5 SMBAlert# flow

Table 8-2 OCW Thresholds

Item	OCW 1	OCW 2	OCW 3
Function / Purpose	OCW Sustained. Slower mechanism to ensure average output current stays below the set threshold.	OCW2 is the OCP threshold for the PSU. It will be used to reduce load and if warranted shutdown the supply if load is not reduced to below de-assertion limits.	OCW3 represents the higher speed PSU output current detection solution. It shall use a peak current detection scheme for fast detection and a window average for de-assertion.
Default Set Point Threshold	100%	125%	140%
Set Point Tolerance	-5% / +0%	-0% / +5%	-0% / +5%
Hysteresis	5%	5%	5%
Programmable Threshold Capability	Yes	Yes (only below the default setpoint)	Yes
Programmable Range	15% - 120% (Programmable Range remains unchanged with input line range).	N/A	Assertion : 25% - 140% De-assertion : Set point - 5%
Programmable Sampling Rate Capability	No	No	No
Programmable Sampling Rate Range	N/A	N/A	N/A
Sampling Rate Set Point Tolerance	+/-5%	+/-5%	For de-assertion: +/-5%

Default Sampling Rate (Min)	50kHz	50kHz	For de-assertion: 50kHz
Default Averaging Window Set Point	250mS	5mS (POWER_EVENT_N Assertion) + (50 ms to PSU shutdown)	For de-assertion: 1mS
SMBAlert# assertion time post window average termination	Max = 100uS	Max = 100uS	N/A. Assertion is triggered on a peak reading.
Programmable Averaging Window Capability	Yes	No	For de-assertion: Yes
Averaging Window Range	1mS - 250mS	N/A	For de-assertion: 1mS-5mS
Averaging Window Set Point Tolerance	(+/-50uS)	(+/-50uS)	(+0/-50uS)
T_BLNK	1mS (+/-100uS)	N/A	1mS (+/-100uS)

T_BLNK: Blanking time for programmable averaging window and OCW thresholds that apply **only** when consecutive window averages have been issued. See figure 15.13, 15.14 and 15.15. A system write to change an OCW threshold or window average, during the T_BLNK period, will result in a value change after the completion of the following window period.
Values expressed in %, in this table, are based on the full +12V main rail capacity located in section 1.2 Supply Overview in sub-section Output Current. For those PSU have different capacities for high line and low line, use the higher main rail capacity for both high line and low line if the difference of power is equal or lower than 50W. For example, an 1100W PSU Main (90.16A @ +12.2V) and 36W Aux (3A@12V) has a hysteresis of 5% of 90.16A = 4.508A for both high line and low line.

8.1.4   Over Current Warning Behavioral Timing Diagrams

8.1.4.1   Over Current Warning 1 (OCW1)
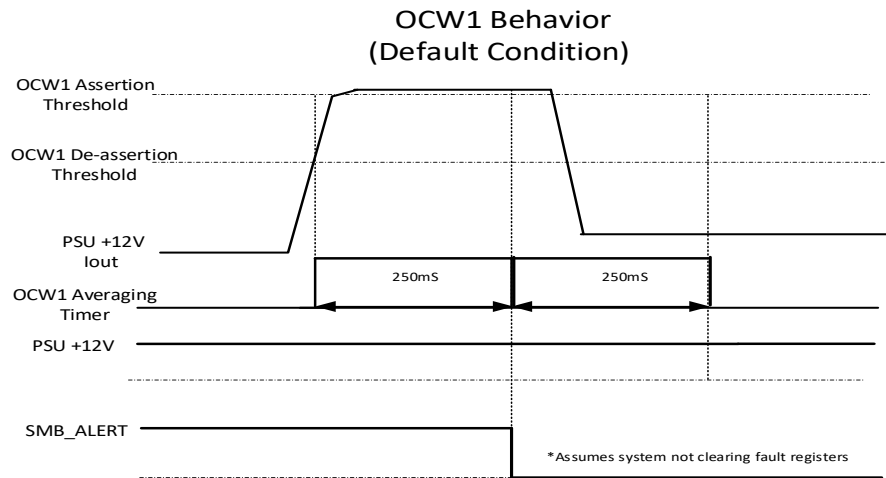
Figure 8-6 OCW1 Timing (Default Setting)

OCW1 Behavior
(Default Condition)

OCW1 Assertion Threshold

OCW1 De-assertion Threshold

PSU +12V Iout

250mS   250mS   250mS

OCW1 Averaging Timer

PSU +12V

SMB_ALERT
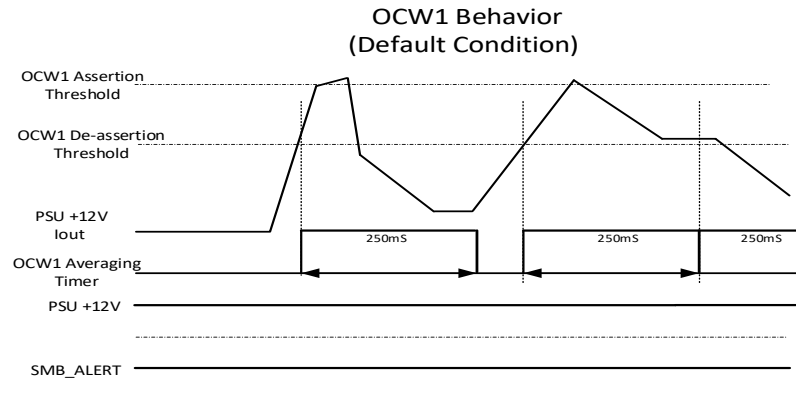
Figure 8-7 OCW1 Timing (Default Setting)

OCW1 Behavior
(Average Window = 50mS)

OCW1 Assertion Threshold

OCW1 De-assertion Threshold

PSU +12V Iout

50ms   50ms   50ms

OCW1 Averaging Timer

PSU +12V
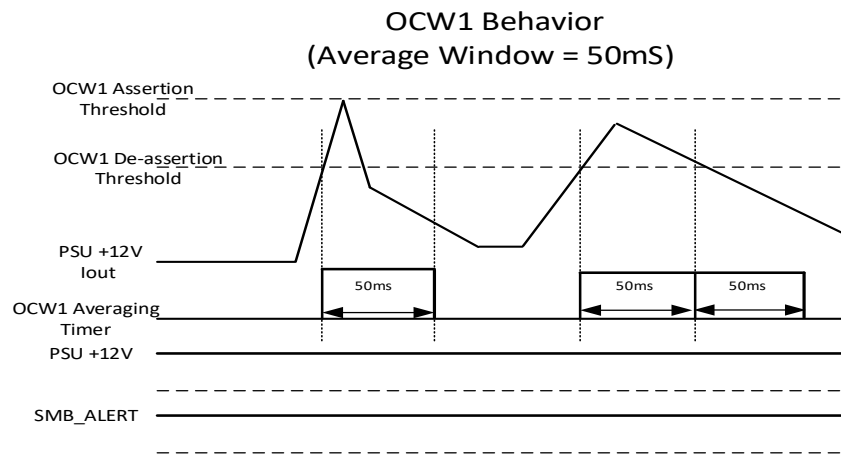
SMB_ALERT

Figure 8-8 OCW1 Timing (50ms Averaging Window)

OCW1 Behavior
(Default Condition) *Assumes All OCW Levels Not Masked

OCW1 Assertion Threshold

OCW1 De-assertion Threshold

PSU +12V Iout

250mS   250mS

OCW1 Averaging Timer

PSU +12V

Rising Edge = Clear Fault Assertion

Clear_Faults
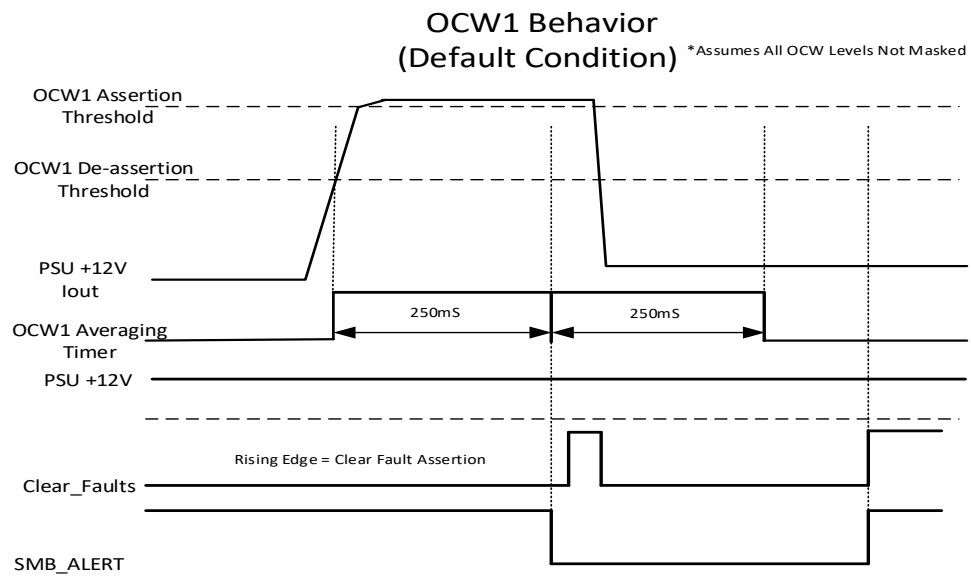
SMB_ALERT

Figure 8-9 OCW1 Timing (Default Setting)

OCW_SETTING_WRITE Occurrence In A Middle Of An Average Window (not consecutive) & During Blanking Time

Figure 8-10 OCW1 setting

OCW_SETTING_WRITE Occurrence In A Middle Of A Consecutive Average Window & During Blanking Time

Figure 8-11 OCW1 setting

**OCW_SETTING_WRITE Occurrence In A Middle Of A
Consecutive Average Window & Outside Of Blanking Time**

OCW1 Assertion Threshold

OCW1 De-assertion Threshold

T_blnk

250mS   75mS   75mS

OCW_SETTING_WRITE for OCW1 (75mS)

Low to High transition represents system OCW_SETTING_WRITE (250mS to 75mS OCW1 window change) command completion and acknowledge by PSU. Since the acknowledge of OCW_SETTING_WRITE came prior to the start of T_blnk, the next average window reflects the programmed value. (Window + 0)

Figure 8-12 OCW1 setting

8.1.4.2   Over Current Warning 2 (OCW2)

Iout OC Warning #2 Assertion = 125%

Iout OC Warning #2 De-assertion = 120%

PSU +12V IOUT

OCW2 Averaging Timer

5mS   50mS

PSU +12V

SMB_ALERT

*Assumes system not clearing fault registers
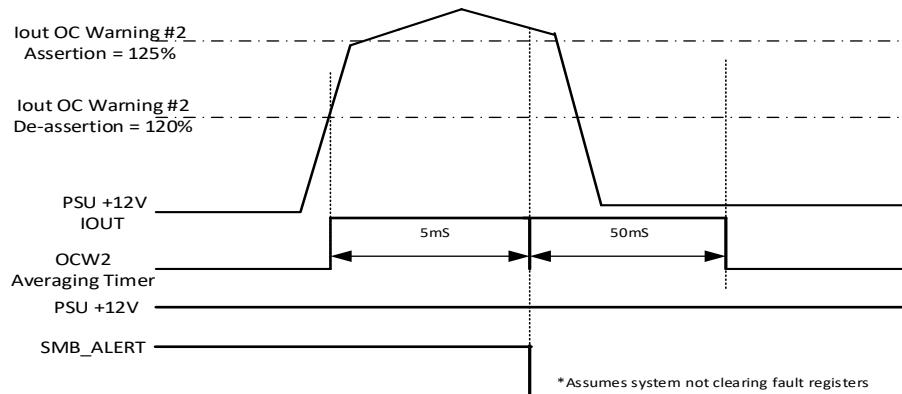
Figure 8-13 SMBAlert# assertion OCW2 Timing (Default Setting)
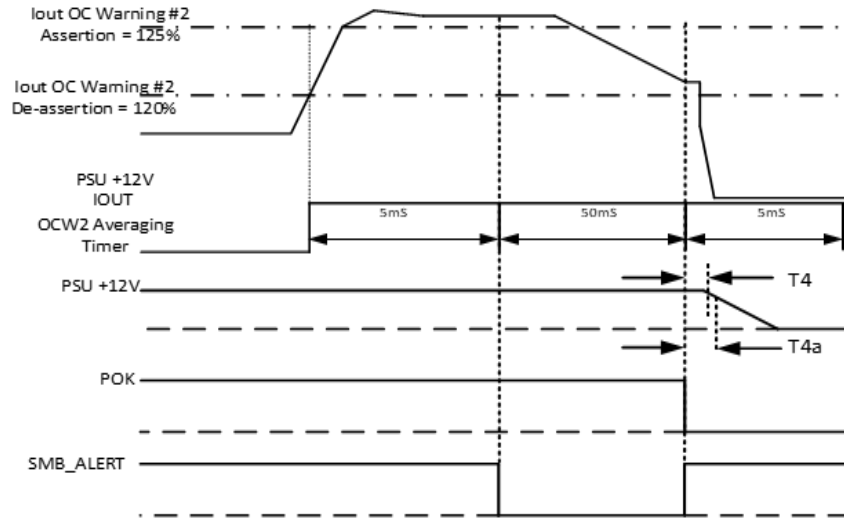
Figure 8-14 OCW2 Timing (Default Setting) with PWOK de-assertion
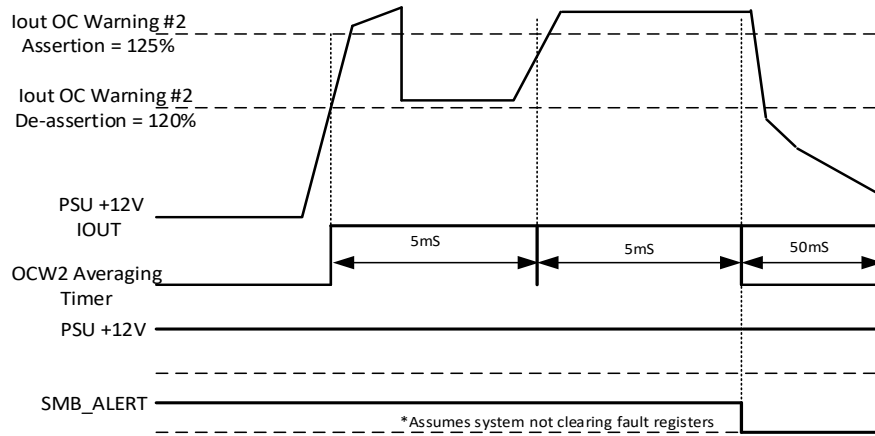
Figure 8-15 SMBAlert# assertion OCW2 Timing (Default Setting)
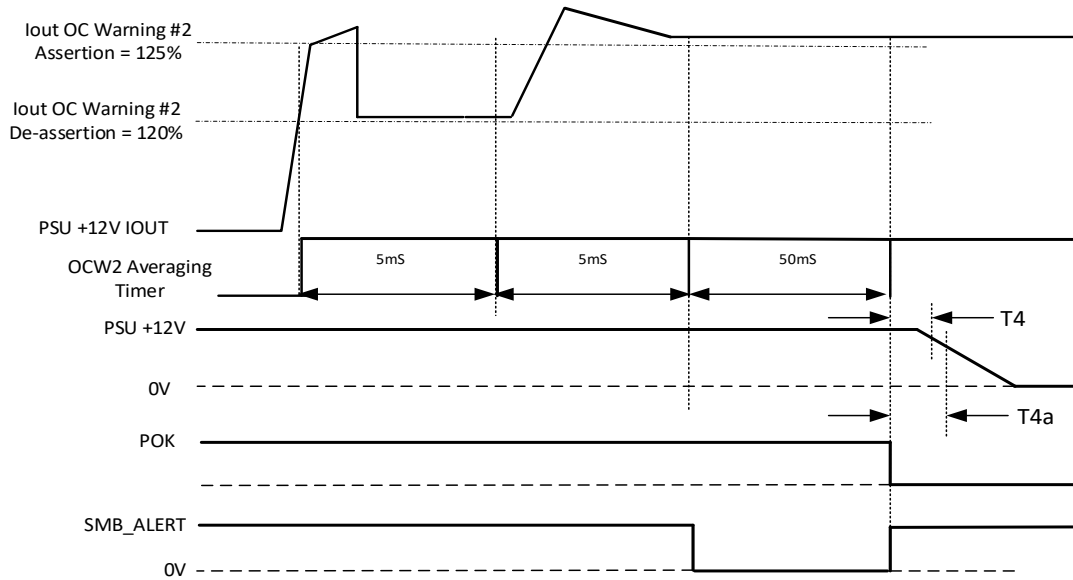
Figure 8-16 SMBAlert# assertion OCW2 Timing (Default Setting) with PWOK de-assertion

8.1.4.3   Over Current Warning 3 (OCW3)

Figure 8-17 OCW3 Timing (Default Setting)

OCW3 Behavior
(1mS Averaging Window)
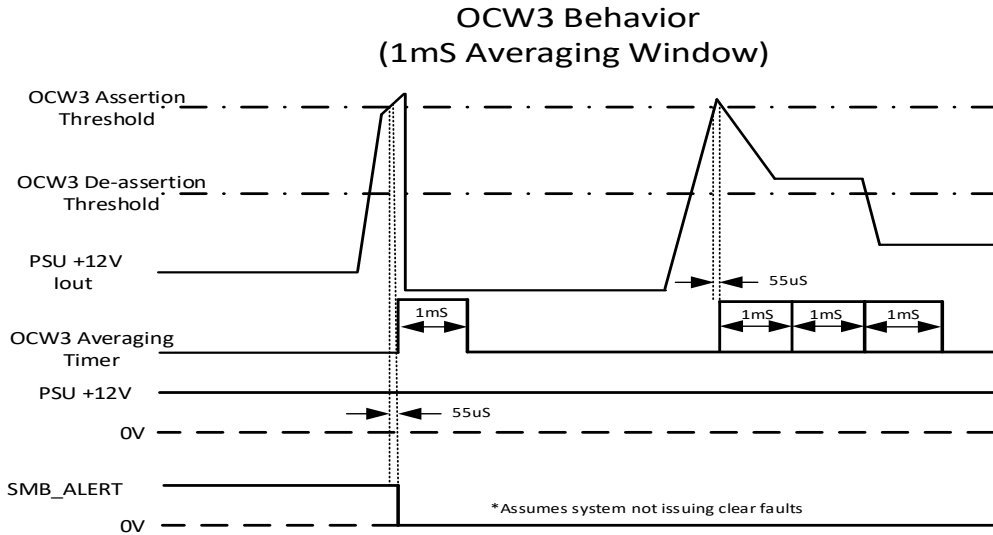
Figure 8-18 OCW3 Timing (Default Setting)

OCW3 Behavior
(5mS Average Window)
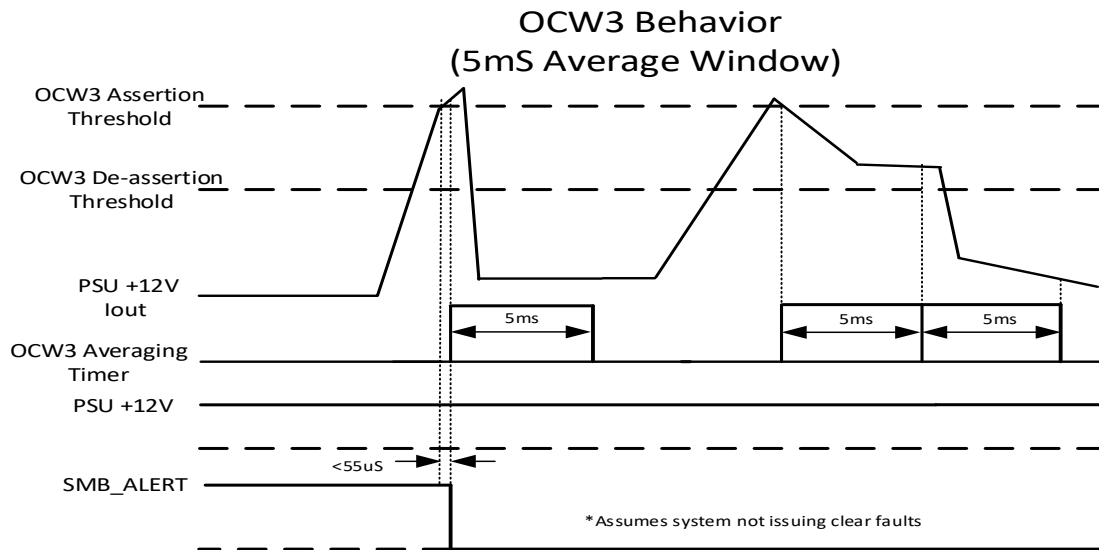
Figure 8-19 OCW3 Timing (Default Setting)
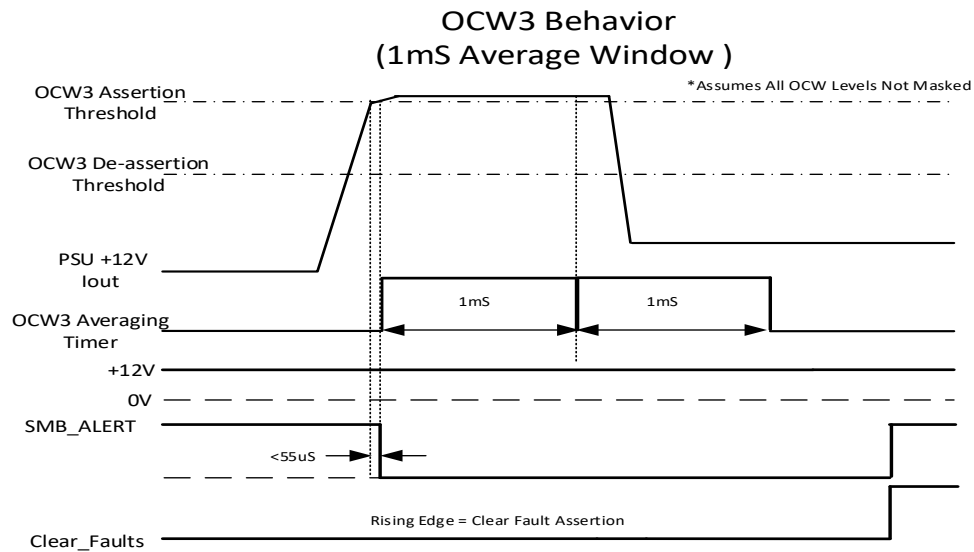
Figure 8-20 OCW3 Timing (1ms Averaging Window)
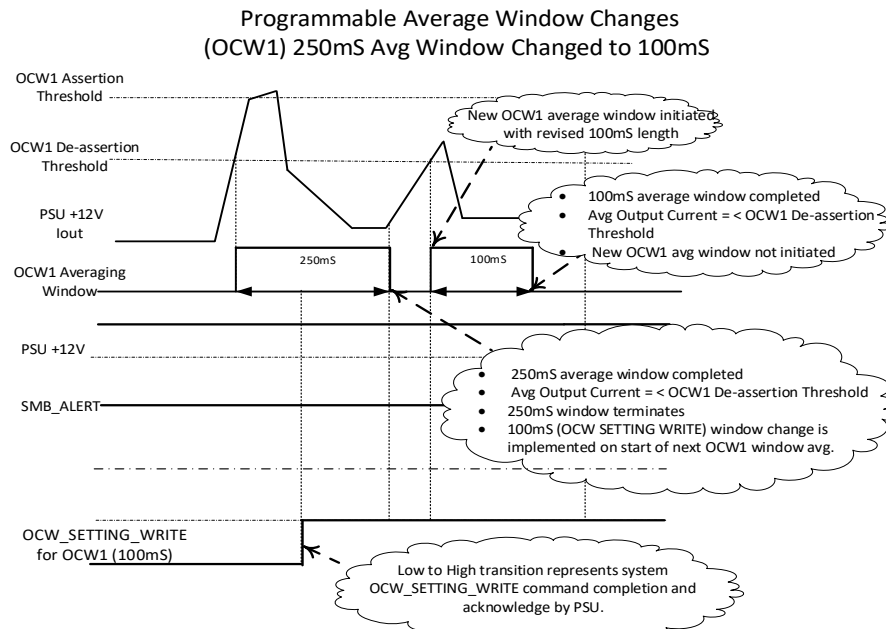
Figure 8-21 OCW3 Timing (Programmable Averaging Window)

8.1.5 Over Current Protection & Over Power Protection (OCP & OPP)

For purposes of definition, the operational range (over the specified time segment per *Figure 8-22 PSU Output Current vs. Time)* of the power supply has been divided up into 4 categories. The graph is intended to provide an illustrative means of describing PSU regulation & protection behaviors based on time vs. load. It does not capture tolerances and or programmable aspects such as assertion thresholds and timings.

- **<100% Load:** This load range represents the sub 100% loading area of the PSU. The voltage regulation limits, slew rate and capacitance are called out in this specification.

- **Extended Voltage Regulation:** This load range represents load step levels >50% to ≤ 100%the PSU. Depending on the size of the load step and starting point, will dictate the regulation range the PSU shall comply with *Table 7-4 Transient load requirements.*

- **Constant Current:** This load range represents the PSU transitioning from a voltage controlled current source to a fixed current source. This mode of operation is considered a protection mode, for which the PSU shall limit its current to a fixed value.

- **Primary Power Limit:** PSU shall contain a primary pulse by pulse current / power limit set at the equivalent output current levels located in *Table 8-3* below. Upon entering this range, the PSU shall limit the power until such time as secondary constant current has been asserted.

Specification	Description	Min	Typ	Max	Units
Initial Constant Current Set Point	Value represents the constant current set point of the PSU. This set point represents the output current that the PSU will clamp its output to.	145	147.5	150	(% of full load rating)
Constant Current Level Drift	Value represents the amount of change in the output current once it is clamped to its set point value. This is measured over a 5ms time period.			+/- 2.5	(% of full load rating)
Constant Current Assertion Time	PSU shall not transition to constant current mode in less time than the minimum time specified. This time is used to establish the amount of time it takes the PSU output to transition from being a voltage controlled current source to a fixed constant current source.	2		3	ms
Constant Current Settling Time	The amount of time starting from constant assertion to the PSU output current reaching the initial constant current set point. Measurement made with minimum output capacitance under section 3.4	200		6000	us
Transition Limits Constant Curent to Constant Voltage	Upon the PSU clamping its output current to its fixed value, the criteria for exiting constant current mode shall be the load falling below the clamped output current level. During this transition the PSU shall maintain the extended output voltage regulation.	Refer to Section *Table 7-4 Transient load requirements* at location referred to as regulation limits.			
Primary Power Limit	PSU shall contain a primary pulse by pulse current / power limit set at the equivalent output current levels located to the right.	170		180	(% of full load rating)

Table 8-3 PSU vs. Load Behaviors – Constant Current and Primary Power Limit

PSU OUTPUT CURRENT Vs. TIME

PSU OUTPUT CURRENT (% Load)

Primary Power Limit
Operation is considered a protection mode for the PSU. PSU shall use a primary side pulse by pulse current/power limit.

CONSTANT CURRENT

Constant Current mode of operation is considered a protection mode for the PSU. During this mode of operation, loss of voltage regulation due to output under-voltage or OCP, may result. Voltage regulation will be a function of load & system capacitance & time.

PSU OCP SHUTDOWN

PSU load levels above 100%, of the PSU rating, are considered transient events. Duty cycle and peak load levels shall not exceed the average power rating of 100%. If these levels are exceeded the PSU may shutdown due to over temperature protection.

170%
160%
150%
140%
130%
125%
120%
110%
100%

2mS
3.0mS
5mS
55mS
100mS

Time

Max Constant Current Assertion Time

Note: Values are typical and do not include programmed set points or hysteresis levels. Values are not to scale.

Figure 8-22 PSU Output Current vs. Time

8.1.5.1 Constant Current During Start Up into Overcurrent Condition

In an event when output current exceeds constant current thresholds defined in *Table 8-3 PSU vs. Load Behaviors – Constant Current and Primary Power Limit*, the power supply shall go into constant current

mode. In the event of an overcurrent start up condition, in which POK does not assert and the start condition is valid the PSU shall issue an OC_FAULT and OCW2 for conditions that triggered a shutdown due to OCW2 only, the OCW1, OCW3 and the under-voltage protection (UVP) shall remain disabled. In an overcurrent startup condition, in which POK is asserted before the 495ms window has expired, the PSU shall Turn ON and average value of Iout Average should be reset and OCW2 should reset to default value. In this condition OCW1, OCW3 and Vout_UV shall get enabled before the PSU is Turned ON.

In a startup condition where average value of Iout is below the OCW2 threshold, the PSU should follow normal Turn ON sequence. The reporting of status register related with over current conditions and Status Word are as shown in the flow chart shown in *Figure 8-23 PSU Start up in to Over Current Condition*.

Flow Chart – Constant Current During Start Up
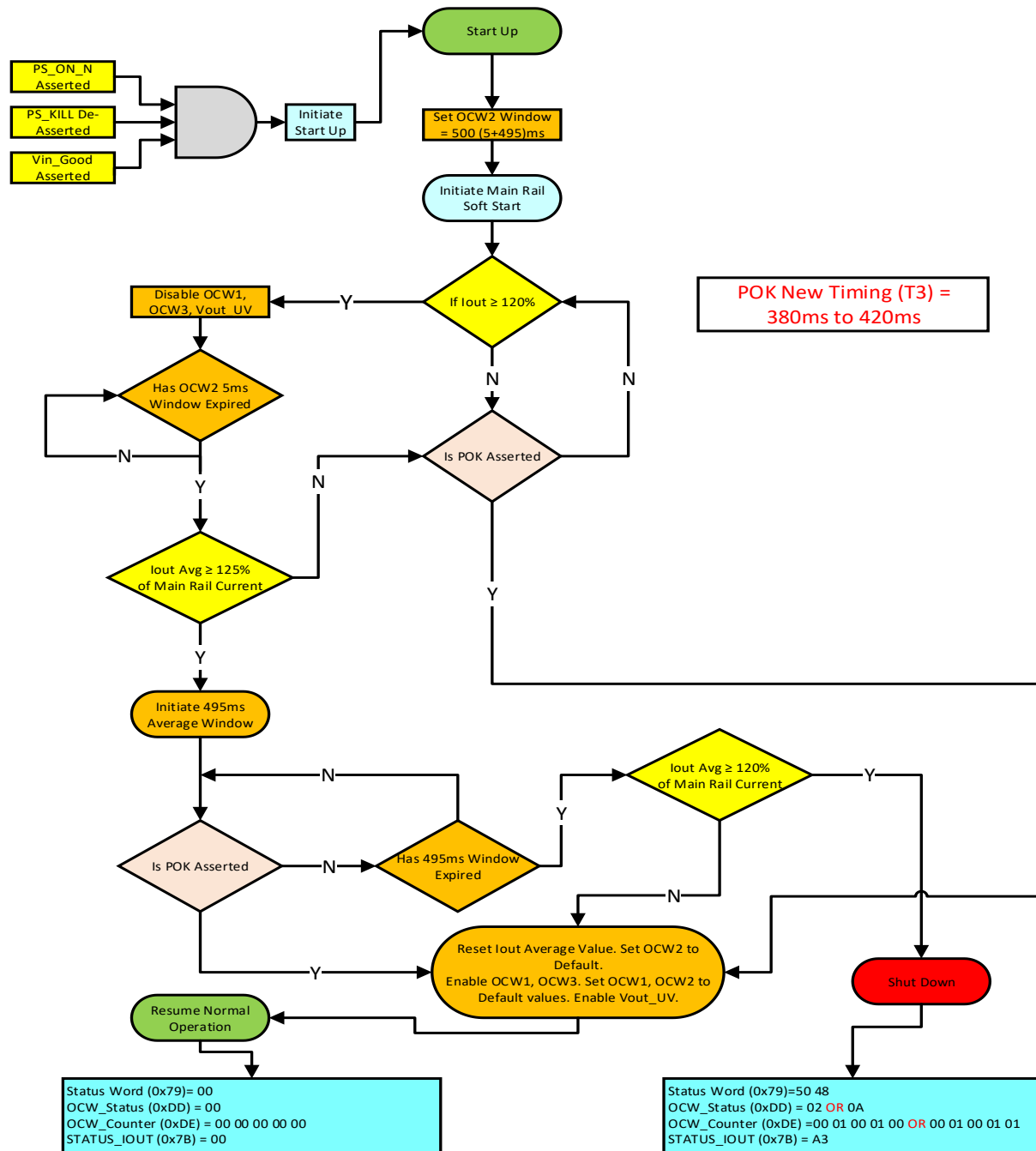
Figure 8-23 PSU Start up in to Over Current Condition

8.1.6   Fast Output Current Sensing for Fast Over Current Warning

The power supply shall have a circuit to quickly assert the SMBAlert# signal when the output current exceeds the over power protection threshold in the PSU. The SMBAlert# signal must always assert before

the overpower protection threshold is exceeded. SMBAlert# must always latch for about 100msec before being released.

8.1.7   Over Voltage Protection (OVP)

The power supply over voltage protection shall be locally sensed and hardware based. The power supply shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON# signal or by an AC power interruption. The values are measured at the output of the power supply's connectors. The voltage shall never exceed the maximum levels when measured at the power connectors of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power connector. 12VSBwill be auto-recovered after removing OVP limit.

Table 8-4 Over Voltage Protection (OVP) Limits

Output Voltage	MIN (V)	MAX (V)
+12V	14.0	15.0
+12VSB	14.0	15.0

8.1.8   Over Temperature Warning (OCW)

The power supply shall be able to alert the system by asserting the SMBAlert# signal to take action when the temperature in any of the temperature sensors reach a predefined threshold in the Temperature Configuration Block (see *12.8.3.2 Temperature Configuration Block*) of the configuration file (see *12.8 Configuration File*)

8.1.9   Over Temperature Protection (OTP)

The power supply shall be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition the PSU will shutdown. OT warning SMBAlert# assertion must always precede the OTP shutdown. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 12VSB remains always on. The OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition. The OTP trip temperature level shall be at least 4°C higher than Over Temperature Warning threshold level. The Over Temperature Protection threshold shall be configurable, See *12.8.3.2 Temperature Configuration Block* in section *12.8 Configuration File* for more details.

8.2   Auxiliary (Stand-by) Output

8.2.1   Over Current Protection Behavior

During initial power on, 12VSB output OCP is blanked for a period *Tblank_startup* to allow starting into rated load with the maximum external capacitive loading across the auxiliary (Stand-by) output. At end of the period *Tblank_startup* 12VSB output shall be in regulation if the 12VSB current is ≤ ISTBY_RATED.12VSB output shall support peaks currents (after start-up – 12VSB output in regulation) as defined in the diagram shown in figure below.
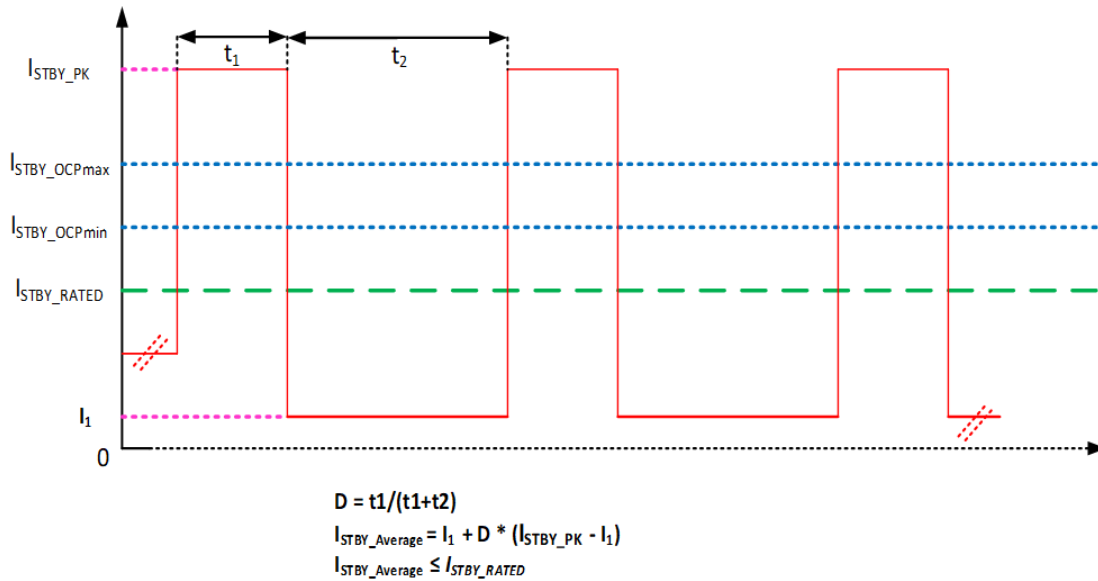
Figure 8-24 Auxiliary (Stand-by) OCP behavior

Notes:
1. If either the duration of ISTBY_ PK > t1 AND / OR the peak current is > ISTBY_ PK, 12VSB output shall enter in OCP Mode.
2. Standby Output shall be capable of handling repetitive peaks as long as the Average value of 12VSB output current is (Averaged over 100ms- 120ms) ≤ ISTBY_RATED. If the Average during repetitive peak event exceeds ISTBY_RATED (-0%,+5%), but falls within the 12VSB OCP limits, 12VSB output shall enter in OCP Mode.
3. If the Average value of 12VSB output current exceeds ISTBY_RATED but is lower than value of ISTBY_OCP, 12VSB output is allowed to Droop, but should remain > UVP Limit and shall continue to operate without hazard OR may shut down due to OTP.
4. Each PSU design shall be tested by disabling OCP on 12VSB and setting the 12VSB load to 0.95 * Max Value of ISTBY_OCP limit of the design (which should be the maximum value of OCP obtained by WCEPTA) to ensure that the PSU satisfies the either of the conditions defined in "1" above. This test is only a design validation test performed at each stage during development.

9   Control and Indicator Functions

9.1   PSON# Input Signal (Input)

The power supply shall have a PSON# signal to remotely turn ON/OFF the power supply. It shall be able to be configured via firmware to work as a two-state (default) or three-state PSON# signal based in the configuration provided by the configuration file. To accomplish the two/three-state modes the power supply shall incorporate the circuit below.
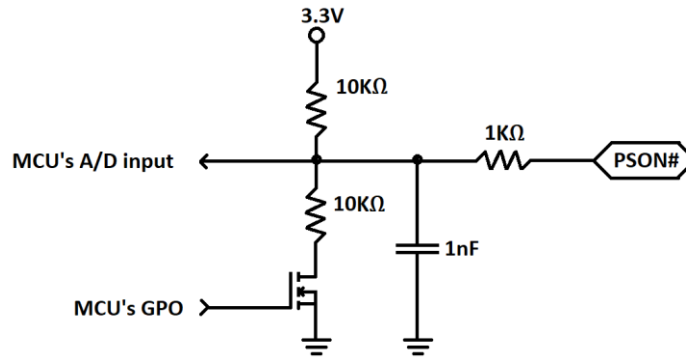
Figure 9-1 Required PSON# input signal circuit for two/three-state operation

Notes:
1. Applying a logic 0 to the MOSFET will configure the PSON# input signal as three-state.
2. Applying a logic 1 to the MOSFET will configure the PSON# input signal as two-state.

The specifications for these two different configurations are described in the following subsections.

9.1.1   Two-State Signal

When the PSON# signal is configured as two-state it shall be active low to turn ON the +12V main power output. When this signal is not pulled low by the system, or left open, the +12V main output shall be turn OFF while the 12VSB output shall remain ON. This signal is pulled to a standby voltage by a pull-up resistor internal to the power supply. The table below lists the required characteristics of the PSON# signal when configured as two-state input.

Table 9-1 Two-state PSON# signal characteristics

Signal Type	Accepts an open collector/drain input from the system. Pull-up to VSB located in power supply.	
PSON# = Low	ON	
PSON# = High or Open	OFF	
	MIN	**MAX**
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	3.46V
Source current, Vpson = low		4mA
Power off delay: Tpson_off_delay		5msec
Power up delay: Tpson_on_delay	5msec	400msec
PWOK delay: T pson_pwok		5msec
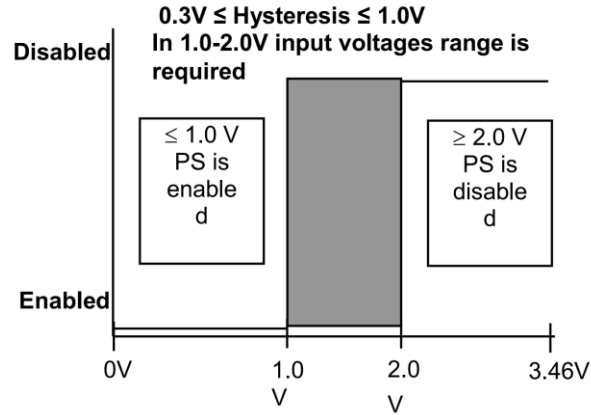
Figure 9-2 Two-state PSON# required signal characteristics.

9.1.2　Three-State Signal

When configured as three-state input, the PSON# signal shall be able to detect logic 0, logic 1 and high impedance (pin floating). The thresholds to detect these three states are depicted in the following figure.
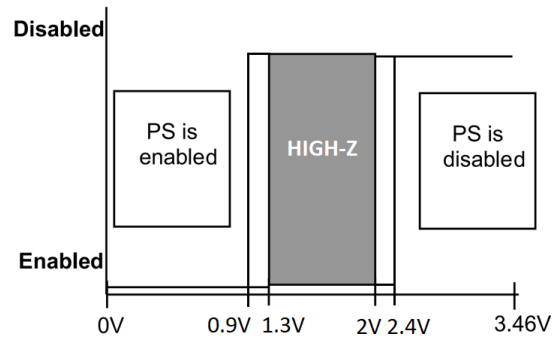
Figure 9-3 Three-state PSON# Required signal characteristics.

PSON# stage shall be designed to follow the logic as shown in the table below for assertion and de-assertion states when used in three-state PSON# mode.

Figure 9-4 PSON# transition states when using 3-state mode

#	VINOK	System State Of PSON#	PSON# Transition State	PSU Main Output State
1	HIGH	Initialization (HI-Z, HIGH)	Hi-Z, High	Remain OFF
2	HIGH	LOW	LOW	Stays ON
3			HIGH	Turns OFF
4			HI-Z	Stays ON
5	HIGH	HIGH	LOW	Turn ON
6			HIGH	Remain OFF
7			HI-Z	Remain OFF
8	HIGH	HI-Z	LOW	Turn ON if OFF || Remain ON
9			HIGH	Turn Off if On || Remain OFF
10			HI-Z	Preserve Last State
11	LOW	LOW	LOW	Remain ON until PWOK drops

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12			HIGH	Turn off
13			HI-Z	Remain ON until PWOK drops
14	LOW	HIGH	LOW	Turn ON until PWOK drops
15			HIGH	Remain OFF
16			HI-Z	Remain OFF
17	LOW	HI-Z	LOW	Turn ON until PWOK drops
18			HIGH	Turn Off if On || Remain OFF
19			HI-Z	Preserve Last State

9.2 PWOK# Input Signal (Output)

PWOK is a power OK output signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. See the table below for a representation of the timing characteristics of PWOK. The start of the PWOK delay time shall be inhibited as long as any power supply output is in current limit.

Table 9-2 PWOK signal characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to VSB located in the power supply.	
PWOK = High	Power OK	
PWOK = Low	Power Not OK	
	MIN	MAX
Logic level low voltage, Isink=400uA	0V	0.4V
Logic level high voltage, Isource=200μA	2.4V	3.46V
Sink current, PWOK = low		400uA
Source current, PWOK = high		2mA
PWOK delay: Tpwok_on	380ms	420ms
PWOK rise and fall time		100μsec
Power down delay: T pwok_off	1ms	
Any PSU fault to PWOK deasertion delay		100μsec

A required circuit implementation of the Power Ok circuit is shown below. The Power Ok circuits shall be compatible with 5V pull up resistor (>10k) and 3.3V pull up resistor (>6.8k).
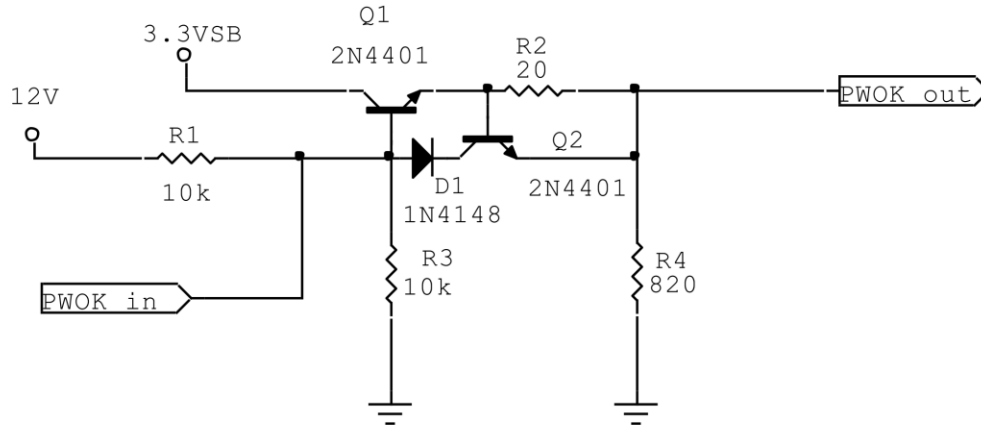
Figure 9-5 PWOK circuit implementation

9.3   SMBAlert# Output Signal (Output)

This signal indicates that the power supply is experiencing a problem that the user should investigate. This signal shall be asserted due to Critical events or Warning events as configured in the configuration file. The signal shall activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits. This SMBAlert# signal is to be asserted in parallel with LED color code selected in the configuration file.

Table 9-3 SMBAlert# signal characteristics

Signal Type (Active Low)	Open collector / drain output from power supply. Pull-up to VSB located in system.	
Alert# = High	OK	
Alert# = Low	Power Alert to system	
	MIN	MAX
Logic level low voltage, Isink=4 mA	0 V	0.4 V
Logic level high voltage, Isink=50 µA		3.46 V
Sink current, Alert# = low		4 mA
Sink current, Alert# = high		50 µA

9.4   VINOK Output Signal (Output)

VINOK signal indicates that the input voltage is within the range where the power supply can operate normally. Details of the operation are described in section *7.15 Timing Requirements*.

Table 9-4 VINOK Signal characteristics

Signal Type (Active High)	Open collector/drain output from power supply. 1KΩ Pull-up to VSB located in the power supply.	
PWOK = High	Input voltage is within the operational range	
PWOK = Low	Input voltage not within the operational range	
	MIN	MAX
Logic level low voltage, Isink=10mA	0V	0.4V

Logic level high voltage, Isource=4mA [1]	3.0V	3.46V
Sink current, VINOK = low		10 mA
Source current, VINOK = high		4mA
VINOK rise and fall time		100µsec

Notes:
1. Using 100KΩ load resistor in the system side.

9.5 Imon Output Signal (Output)

The power supply shall incorporate an output current monitoring pin which will act as a current mirror of the main 12V output, I_{mon} signals from other power supplies in the system can be tied together to provide a mechanism for the system to measure the total output current of all the power supplies combined. The signal shall include an output diode to prevent the current from other power supplies' I_{mon} signal from entering a power supply that is not energized. The characteristics of the signal are described in the table below.

Table 9-5 I_{mon} signal characteristics

Signal type	Current source
Sensitivity	0 to 2mA (representing 0 to 200% of rated current)
Minimum bandwidth	40 kHz
Compliance voltage	10.5V
Time constant	2.9us to 4.0us
Signal delay	< 100ns

Note: The I_{mon} signal shall be able to provide information beyond PL4 levels

The required accuracy for the I_{mon} signal shall be:

% Tolerance = ±1%(10% ≤ Iout ≤ 140%); N/A (140% < Iout ≤200%)
% Read Tolerance = ±1% (10% ≤ Iout ≤ 140%); ±2% (140% < Iout ≤200%)
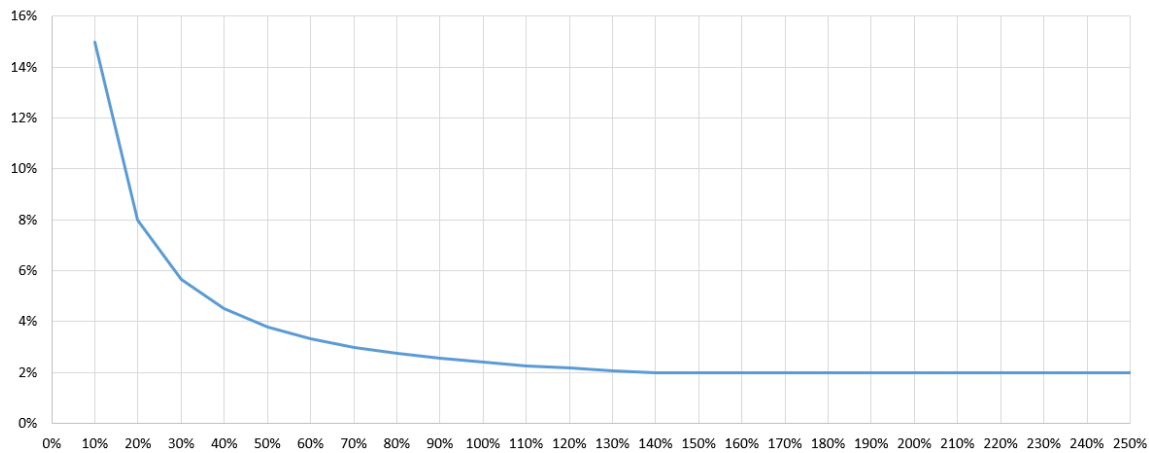
Table 9-6 I_{mon} signal % of tolerance versus % of loading condition

9.6 A0 and A1 Signals (Inputs)

The power supply shall be able to set its SMBus address and FRU address by checking the voltage levels in the A0 and A1 input pins, up to 6 SMBus addresses can be set combining logic states and analog voltage levels in these signals, the characteristics of these two signals are described in the following sections.

9.6.1 A0 Input Addressing

The power supply The A0 input pin shall be analog and able to measure a voltage from 0 to 3.3V to select between logic addressing mode and analog addressing mode. The power supply shall sample the A1 and A0 pins and average the voltage to filter out noise/glitches as defined in the table below.

Table 9-7 A0 input signal characteristics

Signal Type	Analog input. 470KΩ 1% 100ppm Pull-up resistor to 3.3VSB located in the power supply.	
	MIN	MAX
Dynamic range	0V	3.3V
Sampling period (T)	0.9ms	1.1ms
Number of samples (N)	8	8

The power supply shall follow the flow diagram shown in Figure *9-6 Flow diagram to detect between logic and analog SMBus addressing* to determine if the addressing mode is based on logic levels or analog levels.

Start

Wait 10ms

$$A0_{avg} = \frac{1}{N}\sum_{n=1}^{N} A0[n] \qquad A1_{avg} = \frac{1}{N}\sum_{n=1}^{N} A1[n]$$

Sample period = T

$0.85V \geq A0avg \leq 1.95V$

No

Yes

Set SMBus address based on logic states of A0 and A1

Set SMBus address based on A0 analog levels and ignore A1

End
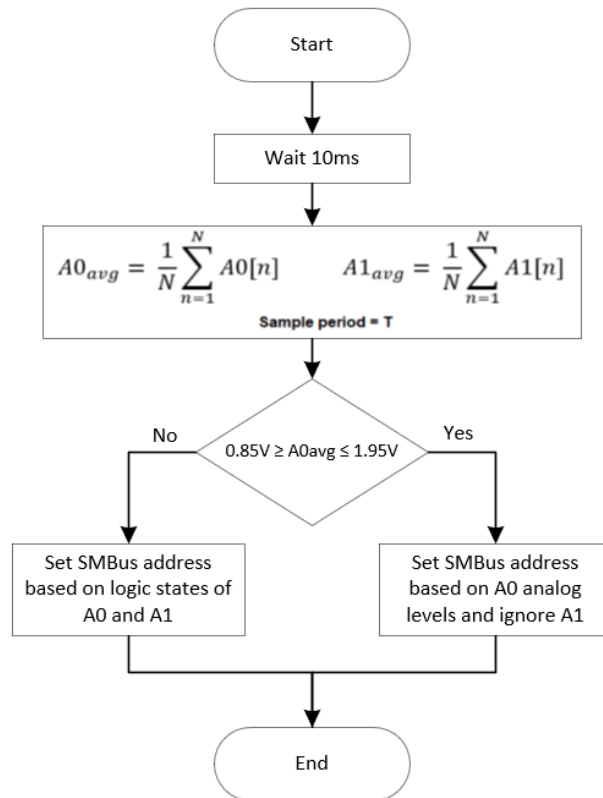
Figure 9-6 Flow diagram to detect between logic and analog SMBus addressing

Note: Refer to *Table 9-7 A0 input signal characteristics* for N and T values.

Table 9-8 Power supply's SMBus addressing using logic levels (up to 4 addresses)

PSU Number	SMBus address PSU / FRU	A1 state	A0 state	Power supply must detect A1 / A0 voltage within this range			System must set A1 / A0 voltage within this range		
				Min (V)	Nominal (V)	Max (V)	Min (V)	Nominal	Max (V)
0	0xB0 / 0xA0	Logic 0	Logic 0	0 / 0	-	0.8 / 0.8	0 / 0	-	0.5 / 0.5
1	0xB2 / 0xA2	Logic 0	Logic 1	0 / 2	-	0.8 / 3.3	0 / 2.4	-	0.5 / 3.3
2	0xB4 / 0xA4	Logic 1	Logic 0	2 / 0	-	3.3 / 0.8	2.4 / 0	-	3.3 / 0.5
3	0xB6 / 0xA6	Logic 1	Logic 1	2 / 2	-	3.3 / 3.3	2.4 / 2.4	-	3.3 /3.3

Table 9-9 Power supply's SMBus addressing using A0 analog levels (up to 6 addresses)

PSU Number	SMBus address PSU / FRU	A1 Voltage (V)	A0 Voltage (V)	Power supply must detect A0 voltage within this range			System must set A0 voltage within this range		
				Min (V)	Nominal (V)	Max (V)	Min (V)	Nominal	Max (V)
0	0xB0 / 0xA0	N/A[1]	0.9	0.8	0.9	1	0.85	0.9	0.95
1	0xB2 / 0xA2	N/A[1]	1.1	1	1.1	1.2	1.05	1.1	1.15
2	0xB4 / 0xA4	N/A[1]	1.3	1.2	1.3	1.4	1.25	1.3	1.35
3	0xB6 / 0xA6	N/A[1]	1.5	1.4	1.5	1.6	1.45	1.5	1.55
4	0xB8 / 0xA8	N/A[1]	1.7	1.6	1.7	1.8	1.65	1.7	1.75
5	0xBA / 0xAA	N/A[1]	1.9	1.8	1.9	2	1.85	1.9	1.95

Notes:
1. A1 pin is used as Data & Sidebands Serialization Interface when the addressing mode is based on analog levels, see *12.7 Data & Sideband Serialization Interface (DSSI)*.

To stablish the address using the A0 analog level mode the system shall place a 1% tolerance 100ppm resistor from the A0 pin to ground with the required value for a given SMBus address as shown in table below.

Table 9-10 Recommended 1% tolerance 100ppm temperature coefficient resistor values for A0 analog addressing mode

PSU Number	Nominal voltage	Required resistor value 1% Tol 100ppm
0	0.9	178 KΩ
1	1.1	237 KΩ
2	1.3	309 KΩ
3	1.5	392 KΩ
4	1.7	499 KΩ
5	1.9	637 KΩ

9.6.2   A1 as Data & Sideband Serialization Interface (DSSI)

The A1 pin shall be dual purpose, the first one is to stablish the SMBus address of the power supply base on the method described in the previous section *9.6.1 A0 Input Addressing*. The second purpose is as a 1-wire communication link. This communication link is only available when the PSU is using only A0 pin to stablish the SMBus address, for more details see *12.7 Data & Sideband Serialization Interface (DSSI)*.

10 Environmental Requirements

10.1 Temperature

Minimum start-up and operating ambient: -5°C
Maximum operating ambient: See *Section 3.1* for operating requirements.
Non-operating ambient: -40°C to +70°C   (Maximum rate of change of 20°C/hour)

10.2 Humidity

Operating: To 85% relative humidity (non-condensing)
Non-Operating: To 95% relative humidity (non-condensing)

NOTE: 95% relative humidity is achieved with a dry bulb temperature of 55°C and a wet bulb temperature of 54°C.

10.3 Altitude

Operating: to 3050 m
Non-operating: to 15200 m

10.4 Mechanical Shock

Non-operating: 50 G Trapezoidal Wave, Velocity change = 170 in. / sec.
                           Three drops in each of six directions are applied to each of the samples

10.5 Random Vibration

Non-operating
Sine sweep:
5Hz to 500Hz @ 0.5gRMS at 0.5 octave/min; dwell 15 min at each of 3 resonant points;
Random profile:
5Hz @ 0.01g²/Hz to 20Hz @ 0.02g²/Hz (slope up); 20Hz to 500Hz @ 0.02g²/Hz (flat);
Input acceleration = 3.13gRMS; 10 min. per axis for 3 axis on all samples

10.6 Thermal Shock (Shipping)

Non-operating: -40°C to +70°C, 50 cycles, 30*C/min. * transition time * 15*C/min., duration of exposure to temperature extremes for each half cycle shall be 30 minutes.

11 FRU Requirements

11.1 FRU Data

The FRU data format shall be compliant with the IPMI ver.2.0 specification. The current version of these specifications is available at https://www.intel.com/content/www/us/en/products/docs/servers/ipmi/ipmi-second-gen-interface-spec-v2-rev1-1.html the following is the exact listing of the EEPROM content. During testing this listing shall be followed and verified.

11.2 Device Protocol

The FRU device will implement the same protocols as the commonly used AT24C02 device, including the Byte Read, Sequential Read, Byte Write, and Page Read protocols.

11.2.1 Data Format

The information to be contained in the FRU device is shown in the following table.

Area Type	Description
Common Header	As defined by the FRU document
Internal Use Area	Not required, do not reserve
Chassis Info Area	Not applicable, do not reserve
Board Info Area	Not applicable, do not reserve
Product Info Area	As defined by the IPMI FRU document. Product information shall be defined as follows:
Field Name	Field Description
Manufacturer Name	{Formal name of manufacturer}
Product Name	{Manufacturer's model number}
Product part/model number	Customer part number
Product Version	Customer current revision
Product Serial Number	{Defined at time of manufacture}
Asset Tag	{Not used, code is zero length byte}
FRU File ID	{Not required}
PAD Bytes	{Added as necessary to allow for 8-byte offset to next area}

Multi-Record Area	As defined by the IPMI FRU document. The following record types shall be used on this power supply:
	   Power Supply Information (Record Type 00h)
	   DC Output (Record Type 01h)
	No other record types are required for the power supply.
	Multi-Record information shall be defined as follows:

Field Name (PS Info)	Field Information Definition
Overall Capacity (watts)	Rated power in watts
Peak VA	Peak power
Inrush current (A)	Inrush current in Amperes
Inrush interval (msec)	5
Low end input voltage range 1	Minimum low line voltage
High end input voltage range 1	Maximum low line voltage
Low end input voltage range 2	Minimum high line voltage

High end input voltage range 2	Maximum high line voltage
A/C dropout total. (msec)	10
Binary flags	Set for: Hot Swap support, Auto switch, and PFC
Peak Wattage	Peak power in watts
Combined wattage	None
Predictive fail tach support	Supported
Field Name (Output)	Field Description: Two outputs are to be defined from #1 to #2, as follows: +12V and +12VSB.
Output Information	Set for: Standby on +12VSB, No Standby on all others.
All other output fields	Format per IPMI specification, using parameters in this specification.

11.2.2 Write Protection

The contents of the FRU shall have write protection mechanism using the PMBus command MFR_FRU_PROTECTION with the hexadecimal number DBh using Write Byte and Read Byte types of commands with PEC. A read value of 00h means the FRU can be written and a value of 01h means the device can't be written (write protection activated), same values apply for Write operation.

12 Firmware Requirements

12.1 PMBus

12.1.1 Related Documents

- PMBus™ Power System Management Protocol Specification Part I – General Requirements, Transport And Electrical Interface; Revision 1.2
- PMBus™ Power System Management Protocol Specification Part II – Command Language; Revision 1.2
- System Management Bus (SMBus) Specification Version 2.0
- System Management Bus (SMBus) Specification Version 3.0

12.1.2 Addressing

The PSU PMBus device address locations are shown below. For redundant systems there are up to two signals to set the address location of the PSU once it is installed in the system: Address1 (A1) and Address0 (A0). For non-redundant systems the PSU device address location should be B0h.

Table 12-1Power supply PMBus device address locations

Addresses used:	X	X	X	X	X	X
System addressing Address1/ Address0	0/0	0/1	1/0 [3]	1/1 [3]	Note 3	Note 3
PMBus device read / write addresses [2]	B0h/B1h[1]	B2h/B3h	B4h/B5h	B6h/B7h	B8h/B9h	BAh/BBh

Notes:
1. Non-redundant systems (single PSU) will use the 0/0 address location.
2. The addressing method uses the 7 MSB bits to set the address and the LSB to define whether a device is reading or writing. The addresses defined above use 8 bits including the read/write bit.
3. See more details in section *9.6 A0 and A1 Signals (Inputs)*.

The PSU shall have an IPMI FRU (field replaceable unit) serial EEPROM. It shall be located at the following addresses. This shall be a separate physical device from the PMBus device. This is intended to align with existing IPMI standards.

Table 12-2 Power supply IPMI FRU device address locations

Addresses used:	X	X	X	X	X	X
System addressing Address1/ Address0	0/0	0/1	1/0 [3]	1/1 [3]	Note 3	Note 3
FRU device read/write addresses [2]	A0h/A1h [1]	A2h/A3h	A4h/A5h	A6h/A7h	A8h/A9h	AAh/ABh

Notes:
1. Non-redundant systems (single PSU) will use the 0/0 address location.
2. The addressing method uses the 7 MSB bits to set the address and the LSB to define whether a device is reading or writing. The addresses defined above use 8 bits including the read/write bit.
3. See more details in section *9.6 A0 and A1 Signals (Inputs)*.

12.1.3 Hardware
The device in the power supply shall be compatible with both SMBus 2.0 'high power' specification for I2C Vdd based power and drive (for Vdd = 3.3V). This bus shall operate at 3.3V.

12.1.4 PMBus Power Sourcing
The circuits inside the power supply shall derive their power from the standby output. For redundant power supplies the device(s) shall be powered from the system side of the OR'ing device. The PMBus device shall be on whenever AC power is applied to the power supply or a parallel redundant power supply in the system.

12.1.5 Pull Ups
Only week pull-up resistors shall be on SCL or SDA inside the power supply connected to 3.3VSB. The main pull-up resistors are provided by the system and may be connected to 3.3V or 5V. For the system design, the main pull-ups shall be located external to the power supply and derive their power from the standby rail.

12.1.6 Data Speed
The PMbus device in the power supply shall operate at the SMBus speed stated in below table and avoid using clock stretching that can slow down the bus. For example, the power supply can clock stretch while parsing a command or a power supply servicing multiple internal interrupts or NACK may require some use of clock stretching. Unsupported commands may respond with a NACK but must always set the communication error status bit in STATUS_CML.

Table 12-3 SMBus speed range

Parameter	Value
SMBus speed	50 kHz to 400 kHz

The PMBus device shall support SMBus cumulative clock low extend time (Tlow:sext) if < 25msec. This requires the device to extend the clock time no more than 25msec between START and STOP for any given message.

12.1.7 Bus Errors

The PMBus device shall support SMBus clock-low timeout (Ttimeout). This capability requires the device to abort any transaction and drop off the bus if it detects the clock being held low for >25ms, and be able to respond to new transactions 10ms later.

The device must recognize SMBus START and STOP conditions on ANY clock interval. (These are requirements of the SMBus specifications but are often missed in first-time hardware designs.) The device must not hang due to 'runt clocks', 'runt data', or other out-of-spec bus timing. This is defined as signals, logic-level glitches, setup, or hold times that are shorter than the minimums specified by the SMBus specification. The device is not required to operate normally but must return to normal operation once 'in spec' clock and data timing is again received. Note if the device 'misses' a clock from the master due to noise or other bus errors, the device must continue to accept 'in spec' clocks and re-synch with the master on the next START or STOP condition.

12.1.8 Additional SMBus hardware requirements

- 300ns maximum fall time with a 400pF capacitive load and 2.7Kohm pull up to 3.3V.
- 10ns minimum fall time with a 20pF capacitive load and 2.7Kohm pull up to 3.3V.
- The power supply shall not load the SMBus if it has no input power.

12.1.9 Writing to the power supply

When responding to read commands the power supply shall extend the clock until all writing of data to the command is complete. The power supply must still meet the Tlow:sext max time of 25msec described in section *12.1.6 Data Speed*. This is needed to make sure if the system performs a series of write and then and immediate read to the same command the power supply returns the value just written to the power supply.

12.1.10   PAGE

Setting a PAGE value of FFh is used to clear all status bits in all PAGEs with the CLEAR_FAULT command.

12.1.11   PAGE_PLUS_WRITE and PAGE_PLUS_READ (05h/06h)

The new PAGE_PLUS_WRITE and PAGE_PLUS_READ commands are used with the STATUS_WORD, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT, and STATUS_CML to create two instances of the same command. Each instance is set by the same events but cleared by their own master in the system. The instances at PAGE 00h are controlled by the system BMC and the instances at PAGE 01h are controlled by the system ME. Below are the protocols used to read and clear the STATUS_ commands using the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands.

Reading STATUS_WORD
Block Write – Block Read Process Call with PEC

1	7	1	1	8	1	8	1	8	1	8	1
S	Power supply address	W	A	PAGE_PLUS_READ command code	A	Byte Count = 2	A	PAGE 1st instance = 00h 2nd instance = 01h	A	STATUS_WORD command	A

1	7	1	1	1	8	1	8	1	8	1	1
Sr	Power supply address	R	A	Byte count = 2	A	STATUS_WORD Low Byte	A	STATUS_WORD High Byte	A	PEC	A	P
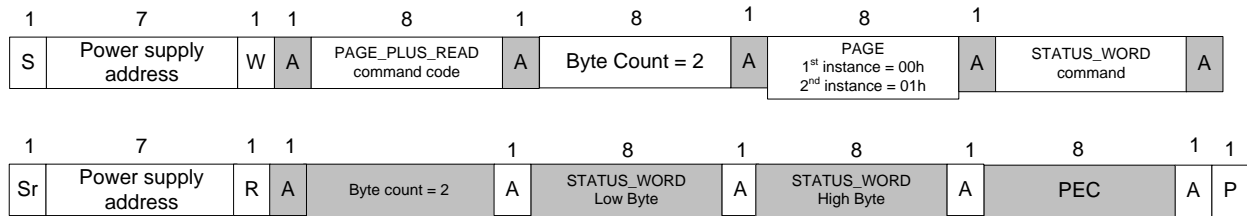
Reading STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML
Block Write – Block Read Process Call with PEC

1	7	1	1	8	1	8	1	8	1	8	1
S	Power supply address	W	A	PAGE_PLUS_READ command code	A	Byte Count = 2	A	PAGE 1st instance = 00h 2nd instance = 01h	A	STATUS command	A

1	7	1	1	1	8	1	8	1	1
Sr	Power supply address	R	A	Byte count = 1	A	STATUS_XXX Byte	A	PEC	A	P
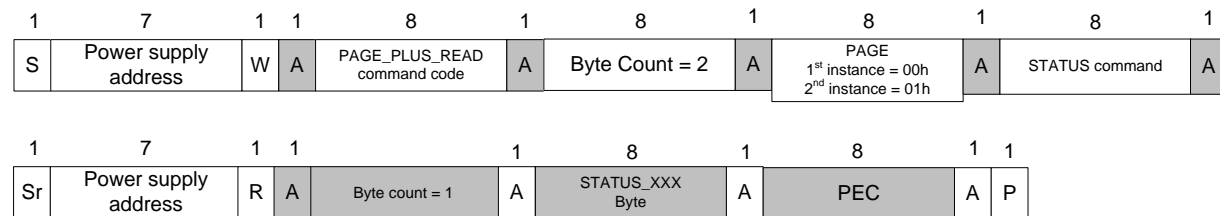
Figure 12-1 Writing/Reading STATUS commands with PAGE_PLUS_READ

Clearing STATUS commands (write '1' to clear a bit)
STATUS_TEMPERATURE, STATUS_IOUT, STATUS_INPUT, STATUS_CML
Block Write with PEC

1	7	1	1	8	1	8	1	8	1
S	Power supply address	W	A	PAGE_PLUS_WRITE command code	A	byte count = 3	A	PAGE 1st instance = 00h 2nd instance = 01h	A

8	1	8	1	8	1	1
STATUS_command	A	Clearing bits '1' = clear	A	PEC	A	P
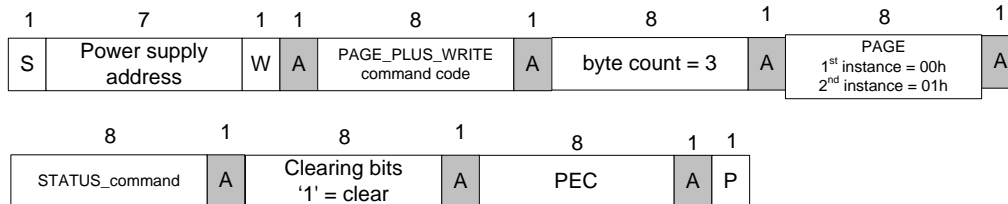
STATUS_WORD cannot be cleared directly It is cleared
based on lower level status commands

Figure 12-2 Clearing STATUS commands using PAGE_PLUS_WRITE

12.1.12   Sensors

The following PMBus commands shall be supported for the purpose of monitoring current, voltage, and power. All sensors shall continue providing real time data as long as the PMBus device is powered. This means in standby mode the main output of the PSU shall be zero amps and zero volts. Sensors shall meet requirements from 100VAC to 127VAC and from 200VAC to 240VAC (or -36VDC to -75VDC for DC input power supplies). They shall be tested down to 5% load.

Table 12-4 Current/Power/Temperature monitoring PMBus commands

PMBus command	Description
READ_EIN	New input energy counter described below. Added to PMBus rev 1.2 spec. Uses direct format for the power accumulator; unsigned integer value for the sample count.
READ_PIN	Input power meter based on PMBus rev 1.1 spec. Uses Linear formatting.
READ_IOUT	Output current in amps for the total 12V current. The other outputs are not sensed. Uses linear format.

READ_EOUT	New output energy counter described below. Added to PMBus rev 1.2 spec. Uses direct format for the power accumulator; unsigned integer value for the sample count.
READ_TEMPERATURE_1	Returns the temperature in °C of the inlet temperature. Based on PMBus rev 1.1 spec. Uses linear format.
READ_TEMPERATURE_2	Returns the temperature in °C of the hot spot temperature. Based on PMBus rev 1.1 spec. Uses linear format.

12.1.13 Sensor Functionality in Different PSU States and Configurations

The functionality of READ_EIN and READ_EOUT in different PSU configurations is stated in the below table. The PSU must continue incrementing the sample counter even if AC power is not present to the PSU but the PMBus device in the PSU is powered from the other power supplies in parallel.

Table 12-5 READ_EIN & READ_EOUT Functioning in differing states

Number of PSUs in system	One PSU state (PSU$_1$)	Rest of PSU states (PSU$_n$)	PSU$_1$ Power Accumulator	PSU$_1$ Sample counter
1 or more	ON & AC present	All ON & AC present	New power values continue to add to the power accumulator based on loading condition	Sample counter increments every sample period
1 or more	*Stby & AC present*	*All ON & AC present*	*New power values continue to add to the power accumulator based on loading condition*	*Sample counter increments every sample period*
1 or more	OFF & no AC present	All OFF & no AC present	Reset power accumulator values to 00 when AC power is re-applied	Reset sample counter to 00 when AC power is re-applied
2 or more	AC power not present	Rest of PSUs in standby mode & AC present	Continue adding 0W to accumulator every sample period	Incrementing sample counter every sample period
2 or more	AC power not present	Rest of PSUs ON & AC present	Continue adding 0W to accumulator every sample period	Incrementing sample counter every sample period

READ_PIN, READ_IOUT, and READ_TEMPERTURE_x shall continue to report accurate values when the PSU is in standby mode or when it has no AC power but is in parallel with another PSU(s) with AC power and standby power present.

12.1.14 READ_PIN (97h)

The power supply shall provide input power data in watts.   The data shall be reported using the PMBus linear format. The data shall be the average input power or filtered input power. If a simple average is used to provide average input power, the minimum averaging duration shall be 2 seconds. If filtering is used; the maximum filter bandwidth shall be 0.5 Hz. The accuracy shall be tested by polling with the READ_PIN command at a rate ranging from 1 sample / second to 10 samples / second.

Table 12-6 READ_PIN requirements summary

	MIN	MAX	Description
Format	PMBus linear format		PMBus data format; refer to PMBus specification for details
Averaging period	2 seconds	10 seconds	The AC input power shall be averaged using a simple averaging method of a filtering method. This defines the max/min period for simple averaging and the bandwidth range if the filter method is used.
Filtering bandwidth	0.1 Hz	0.5 Hz	
Accuracy	+/-1%		

(>125W – Max load/Peak Power)			The input power data shall meet these accuracy requirements over 100-240VAC and under the defined system polling rate.
Accuracy (50W - 125W load)	+/-1.25W		
Accuracy (<50W load)	+/-5W		
System polling rate	1 sample/ second	10 samples / second	The power supply shall be polled over this range of rates while testing accuracy.

12.1.15   READ_IOUT (8Ch)

The power supply shall provide output current data in amperes.   The data shall be reported using the PMBus linear format. The data shall be the average output current or filtered output current. If a simple average is used to provide average output current, the minimum averaging duration shall be 2 seconds. If filtering is used; the maximum filter bandwidth shall be 0.5 Hz. The minimum accuracy is specified in the table below. The accuracy shall be tested by polling with the READ_IOUT command at a rate ranging from 1 sample / second to 10 samples / second.

Table 12-7 READ_IOUT requirements summary

	MIN	MAX	Description
Format	PMBus linear format		PMBus data format; refer to PMBus specification for details
Averaging period	2 seconds	10 seconds	The output current shall be averaged using a simple averaging method of a filtering method. This defines the max/min period for simple averaging and the bandwidth range if the filter method is used.
Filtering bandwidth	0.1 Hz	0.5 Hz	
Accuracy (300W – Max load/Peak Power)	+/-1%		The output current data shall meet these accuracy requirements over 100-240VAC and under the defined system polling rate.
Accuracy (150W - 300W load)	+/-3%		
Accuracy (40W – 150W load)	+/- 0.9A		
System polling rate	1 sample/ second	10 samples / second	The power supply shall be polled over this range of rates while testing accuracy.

12.1.16   READ_EIN (86h)

The new READ_EIN command is used to allow the system to apply its own input power filtering. This will allow the system to get faster input power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

Table 12-8 READ_EIN requirements summary

	MIN	MAX	Description
Format	PMBus Direct format m = 01h, R = 00h, b = 00h		PMBus data format; refer to PMBus specification for details.
P_{sample} averaging period	4 AC cycles		Period instantaneous input power is averaged over to calculate P_{sample}.
READ_EIN update period	80/66.7ms (50/60Hz)		Period at which the power accumulator and sample counter are updated
Accuracy	+/-1%		

(>125W – Max load/Peak Power)			
Accuracy (125W - 125W load)	+/-1.25W		The input power data shall meet these accuracy requirements over 100-240VAC and under the defined system polling rate.
Accuracy (<50W load)	+/-5W		
Range of System polling period	1 sec	100 ms	The PSU shall be polled over this range of rates while testing accuracy.
IMPORTANT: The PSU READ_EIN update period MUST always be less than the system polling period. To make sure the PSU is compatible with all possible system polling periods; the PSU must update the READ_EIN power accumulator and sample counter at a period less than 100msec (required period is 4 AC cycles 80/67msec).			

12.1.17 READ_EOUT (87h)

The new READ_EOUT command is used to allow the system to apply its own output power filtering. This will allow the system to get faster output power data while preventing aliasing. The command returns an accumulated power value and an associated sample count of number of accumulated power values. This allows the system to calculate its own average power value each time the system polls the PSU.

Table 12-9 READ_EOUT requirements summary

	MIN	MAX	Description
Format	PMBus Direct format m = 01h, R = 00h, b = 00h		PMBus data format; refer to PMBus specification for details.
P_{sample} averaging period	Nominal 8msec		Period instantaneous input power is averaged over to calculate P_{sample}.
Sampling period	Nominal 8msec		Period at which the power accumulator and sample counter are updated
[P_{accum} / N] Accuracy (5% to 100% load)	±2%		The calculated output power data shall meet these accuracy requirements over 100-240VAC and under the defined system polling rate.
System polling rate	1 sample /s	10 samples /s	The PSU shall be polled over this range of rates while testing accuracy.

12.1.18 READ_EIN & READ_EOUT Formats

The READ_EIN and READ_EOUT commands shall use the PMBus direct format to report an accumulated power value and the sample count. The PMBus coefficients m, R, and b shall be fixed values and the PSU shall report these values using the PMBus COEFFICIENT command. The coefficient m shall be set to 01h, coefficient R shall be set to 00h, and coefficient b shall be set to 00h.

READ_EIN and READ_EOUT shall use the SMBus Block Read with PEC protocol in the below format.

1	7	1	1	8	1	1	7	1	1	8	1
S	Power supply address	W	A	READ_EIN command code	A	Sr	Power supply address	R	A	Byte Count = 6	A	…

8	1	8	1	8	1	8	1	8	1
Accumulated power – low byte	A	Accumulated power – high byte	A	Accumulated power roll over count	A	Sample count – low byte	A	Sample count – middle byte	A	…

8	1	8	1	1
Sample count – high byte	A	PEC	A	P
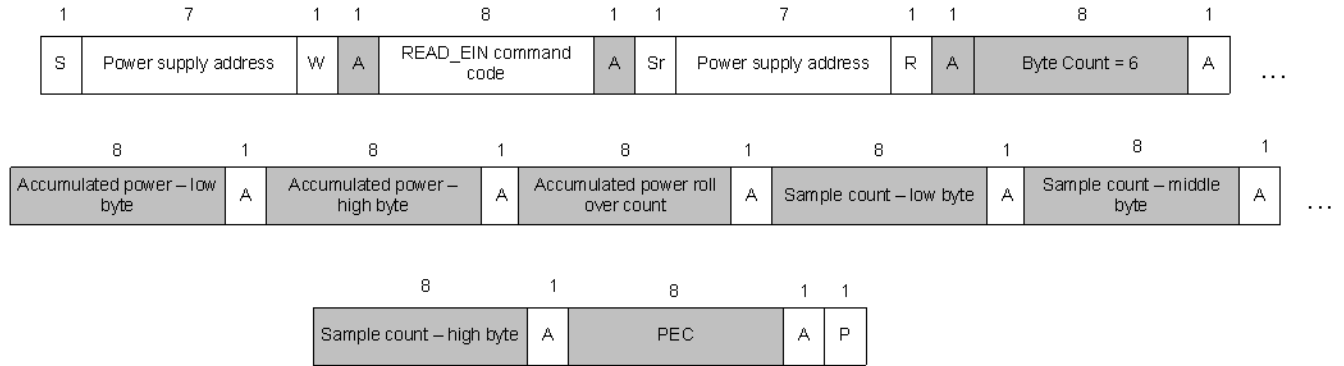
Figure 12-3 READ_EIN command format

READ_EIN and READ_EOUT Accumulators

The accumulated power data shall be the sum of input power values averaged over 4 AC cycles (or over 50ms for READ_EOUT). The value shall automatically roll-over when the 15 bit maximum value is reached (> 7FFFh). The sample count should increment 1 for each accumulated power value. The system shall calculate average power by dividing the accumulated power value by the sample count. The system must sample READ_EIN and READ_EOUT faster than the roll-over period to get an accurate power calculation. Below is a block diagram depicting the accumulator function in the PSU.

Important note: When the PSU responds to the system requesting READ_EIN or READ_EOUT data; the data in the sample count must always alignment with the number of samples accumulated in the power accumulator. To achieve this power accumulator, power rollover counter, and sample counter shall be loaded into a READ_EIN and READ_EOUT register at the same time.
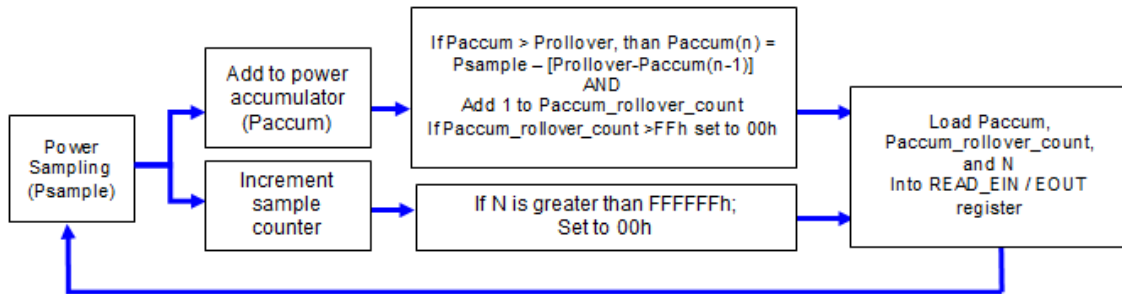
Figure 12-4 READ_EIN functional diagram

Table 12-10 READ_EIN variables description

Parameter	Description
Psample:	The sampled power value in linear or direct format
Paccum:	2 bytes in PMBus linear or direct format. The accumulated power values made up of Psample(0) + Psample(1) + … + Psample(n)
N:	3 byte unsigned integer value. The number of accumulated power values summed in Paccum
Prollover:	The max value of Paccum before a rollover will occur
Paccum_rollover_count:	1 byte unsigned integer counting the number of times Paccum rolls over. Once this reaches FFh; it will automatically get reset to 00h

12.1.19 COEFFICIENT (30h)

The power supply shall support the PMBus COEFFICIENT command. The system shall use this to read the values of m, b, and R used to determine READ_EIN accumulated power values.

Table 12-11 m, B, R coefficients

Command	COEFFICIENTS support	m	B	R
READ_EIN	Yes	01h	00h	00h
READ_EOUT	Yes	01h	00h	00h
all other commands	*Optional*	*X*	*X*	*X*

12.1.20 Status Commands

The following PMBus STATUS commands shall be supported. All STATUS commands stated in Table below as supporting PAGE instances shall support the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands since they are used by both the BMC and ME. The BMC and ME refer to the two instances of the commands accessed via the PAGE_PLUS_WRITE and PAGE_PLUS_READ commands. The status bits shall assert whenever the event driving the status bit is present. Once a bit is asserted it shall stay asserted until cleared using one of the methods shown in section 10.1.21.

The STATUS commands that are supported with the PAGE_PLUS_READ and PAGE_PLUS_WRITE commands shall still support direct access of the base STATUS_XXX commands using the read word, write word, read byte, and write byte protocols.

STATUS_FAN_1_2 command is only accessed by the system BMC. It uses the standard read byte protocol to read status and write byte protocol to clear bits.

The STATUS events are also used to control the SMBAlert# signal. The new SMBALERT_MASK command is used to define which status event control the SMBAlert# signal. Default values for these mask bits are shown in the table below.

Table 12-12 PMBus* STATUS commands summary

PMBus command	Bit location	PSU state when bit is asserted ('1')	Instances No PAGE'ing [2] PAGE 00h = BMC PAGE 01h = ME	SMBALERT_MASK defaults for each of the three instances (No PAGE, PAGE 00h, PAGE 01h) 0 = causes assertion of SMBAlert# 1 = does not cause assertion of SMBAlert#
STATUS_WORD			No PAGE, 00h, 01h	
OFF	6 (lower)	OFF		NA
IOUT_OC_FAULT	4 (lower)	Refer to STATUS_IOUT		NA
TEMPERATURE	2 (lower)	Refer to STATUS_TEMPERATURE		NA
VIN_UV_FAULT	3 (lower)	Refer to STATUS_INPUT		NA
CML	1 (lower)	ON		NA
VOUT	7 (upper)	Refer to STATUS_VOUT		NA
IOUT/POUT	6 (upper)	Refer to STATUS_IOUT		NA
INPUT	5 (upper)	Refer to STATUS_INPUT		NA
FANS	2 (upper)	Refer to STATUS_FANS		NA

STATUS_VOUT			No PAGE'ing	
VOUT_OV_FAULT	7	OFF		1, NA, NA
VOUT_UV_FAULT	4	OFF		1, NA, NA
STATUS_IOUT			No PAGE'ing, 00h, 01h	
IOUT_OC_FAULT	7	OFF		1, 1, 1
IOUT_OC_WARNING	5	ON		1, 1, 0
POUT_OP_FAULT	1	OFF		1, 1, 1
POUT_OP_WARNING	0	ON		1, 1, 1
STATUS_INPUT			No PAGE'ing, 00h, 01h	
VIN_UV_WARNING	5	ON		1, 1, 1
VIN_UV_FAULT [1]	4	OFF		1, 1, 0
Unit off for low input voltage	3	OFF		1, 1, 1
IIN_OC_WARNING	1	ON		1, 1, 1
PIN_OP_WARNING	0	ON		1, 1, 1
STATUS_TEMPERATURE			No PAGE'ing, 00h, 01h	
OT_FAULT	7	OFF		1, 1, 1
OT_WARNING	6	ON		1, 1, 0
STATUS_FANS_1_2			No PAGE'ing	
Fan 1 fault[3]	7	OFF		1, NA, NA
Fan 1 warning[3]	5	ON		1, NA, NA

Notes:

1. The Vin Fault bit in STATUS_INPUT shall get asserted if the input power has dropped below the PSU's operating range for any duration of time, even if the PSU continues to operate normally through a momentary input dropout event.
2. 'No PAGE' is the standard STATUS_ commands accessed directly without using the PAGE_PLUS commands.
3. 3 All fans/rotors in the PSU shall be OR'ed into a single fan status bit for fault and warning conditions.

12.1.21   Resetting Status Bits

The STATUS_ commands shall be reset only by the below methods. If the event is still present that caused the assertion of the status bit, the bit shall stay assert after clearing.

- Writing a '1' to any given bit location shall reset only that bit of the command.
- Sending a CLEAR_FAULTS command to the PSU shall reset all STATUS_ bits to '0'.
  CLEAR_FAULTS shall clear all STATUS commands at a given PAGE if PAGE command is supported.
  If the PAGE is set to FFh; all STATUS bits in all PAGEs shall be cleared.
- Cycling input power OFF for 1 second or more then ON shall reset all STATUS_ bits to '0'.
- Systems with redundant power supplies where only one of the supplies cycle input power ON/OFF; the power cycled PSU shall reset the STATUS_ bits to '0' only when powered back ON.
  If the PSU is kept OFF, the STATUS_ bits shall not be reset.

- Cycling the PSON# signal from de-asserted to asserted shall reset the STATUS_ bits to '0'. The bits shall be reset only on the assertion of PSON#; not the de-assertion.

  Note: Exception for Over Current Fault shutdown; PSON# cycling shall NOT reset the over current fault bit or cause the power supply to restart. Only a cycle of the input power shall reset the over current fault bit and allow the PSU to power on again.

12.1.22 Default Limits for Warning and Faults

Warning limits shall be set with enough margin to guarantee no false warnings will occur is PSU operates within the specified requirements, but before the PSU shuts down. Fault limits shall be set at limits equal to or greater than the level at which the PSU shuts down.

12.1.23 Resetting to Default Limits

The PSU shall reset the warning and fault limits to default values for the following case.

- Input power cycling
- PSON power cycling

12.1.24 Faults and Error Checking

The PSU shall support PEC per the SMBus 2.0 specification.

12.1.25 Packet Error Checking

The PSU shall support packet error checking to support error checking and handling.

12.1.26 Capability and Inventory Reporting

The follow commands shall be supported for discovery of the power supplies capabilities.

Table 12-13 PMBus PSU capability & inventory commands summary

PMBus command	Value	Description
CAPABILITY	PEC = supported Bus speed = 400kHz SMBAlert# = supported	Defines the power supplies PEC support, bus speed, and support of SMBAlert
QUERY	Linear formats for all but READ_EIN / READ_EOUT which is Direct	Used to determine if the PSU supports a specific command. It should return the proper information about any commands listed in Table 12-18 Summary of PMBus commands
PMBUS_REVISION	0010 0010	Used to verify the PMBUS_REVISION the PSU is based on. This shall be set to revision 1.2.
MFR_TEMP1_MAX	Trip threshold for the ambient temperature sensor (TEMP1) to assert SMBAlert#	Defines the maximum inlet temperature to generate a warning condition in the STATUS_TEMPERATURE command.
MFR_TEMP2_MAX	Trip threshold for the hot spot temperature sensor (TEMP2) to assert SMBAlert#	Defines the maximum hotspot temperature to generate a warning condition in the STATUS_TEMPERATURE command.
MFR_IOUT_MAX	Rated output current using the linear format	Defines the maximum rated output current on the 12V rail.
MFR_POUT_MAX	Rated output power using the linear format	Defines the maximum rated output power of the PSU.

APP_PROFILE_SUPPORT	05h	Defines that the PSU supports this application profile.

12.1.27 SMBAlert# Signal

The SMBAlert# signal may be asserted by the PSU for any of the supported STATUS events. The events that control SMBAlert# can be masked using the SMBALERT_MASK command. Default masking is shown in section 0.

By default, the SMBAlert# signal is asserted for the following cases:

1. STATUS_INPUT (UV Fault bit): input voltage drops below the fault threshold of the PSU for > 2ms.
2. STATUS_IOUT (Iout OC Warning bit): Output current exceeds the PSU capability, but PSU has not shutdown.
3. STATUS_TEMPERATURE (OT Warning): Thermal sensor for PS inlet temperature or on a hot spot inside the PSU has exceeded its warning temperature.

Table 12-14 PSU SMBAlert# timing requirements

Item	Description	PMBus command	MIN	MAX
T_{alert_input}	Timing from input voltage dropping to 0VAC to SMBAlert# going low	STATUS_INPUT UV Fault		2 msec
$T_{OC\_Warning}$	Timing from output over current warning to SMBAlert# going low	STATUS_IOUT	10 msec	20 msec[1]
$T_{OC\_Warning\_latch}$	Time the PSU holds the SMBAlert# signal asserted after an over current warning event	STATUS_IOUT		30sec
$T_{OC\_pmaxprotection}$	Timing from output tripping	None		20µsec
T_{over_temp}	Hot spot temp > warning threshold	STATUS_TEMPERATURE Over temp warning		1 sec
$T_{smbalert\_shutdown}$	Minimum time PSU must continue to operate within voltage regulation limits and PWOK asserted after the SMBAlert# signal has been asserted due to an over temperature event.	NA	1sec	
$T_{max\_warning}$	Hot spot temperature inside the PSU that causes SMBAlert# to assert.	MFR_TEMP2_MAX	Tmax_continuous	Tshutdown

Notes:
1. This time must be shorter than OCP trip delay.
2. 2 msec Max Talert_input only applies to load higher than 10% of the rated load where SmarRT is meaningful.

12.1.28 SMBAlert# Operation in Standby Mode

The PSU shall assert the SMBAlert# signal only when the main outputs are ON. SMBAlert# shall stay de-asserted when the PSU is in standby mode when any bits in the STATUS commands get asserted.

12.1.29 SMBALERT_MASK (1Bh)

This allows the system to mask events from asserting the SMBAlert# signal and to read back this information from the PSU. SMBALERT_MASK command can be used with any of the supported STATUS events. The events are masked from asserting SMBAlert# by writing a '1' to the associated STATUS bits.

The SMBALERT_MASK command is used in conjunction with the PAGE_PLUS command and STATUS_ commands. It is not supported for masking the Non-PAGE'd STATUS_ commands. Below are the protocols.

Reading mask values using PAGE_PLUS
Block Write – Block Read Process Call with PEC

1	7	1	1	8	1	1	8	1	8	1
S	Power supply address	W	A	PAGE_PLUS_READ Command code	A	Byte count = 3	A	PAGE 1st instance = 00h 2nd instance = 01h	A	SMBALERT_MASK command code	A

8	1	1	7	1	1	1	8	1	8	1	1
STATUS command	A	Sr	Power supply address	R	A	Byte count = 1	A	Mask values 1 = masked	A	PEC	A	P
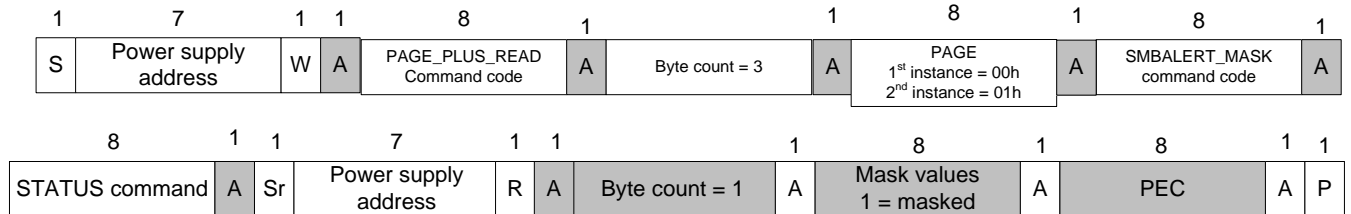
Figure 12-5 PAGE_PLUS_READ command

Writing mask values using PAGE_PLUS
Block Write with PEC

1	7	1	1	8	1	8	1	8	1
S	Power supply address	W	A	PAGE_PLUS_WRITE command code	A	Byte Count = 4	A	PAGE 1st instance = 00h 2nd instance = 01h	A

8	1	8	1	8	1	8	1	1
SMBALERT_MASK command code	A	STATUS command	A	Mask values 1 = masked	A	PEC	A	P
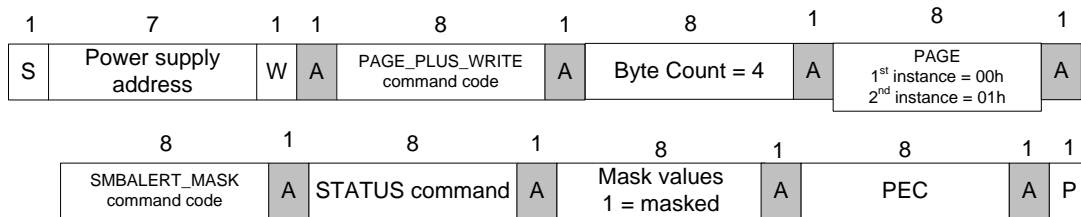
STATUS_WORD is not used with SMBALERT_MASK. Only the 'root' event bits are used to control the SMBAlert signal

Figure 12-6 PAGE_PLUS_WRITE command

12.1.30   Alert Response Address (ARA)

The PSU shall not support ARA. After asserting the SMBAlert# signal the PSU shall keep its address at it standard address; not change to 18h.

12.1.31   Setting and Resetting the SMBAlert# Signal

The SMBAlert# signal shall be asserted whenever any un-masked event has occurred. This is a level detected event. Whenever the event is present SMBAlert# shall be asserted. The SMBAlert# signal shall not de-assert at any time if the event that has caused the assertion is still present.

The SMBAlert# signal shall be cleared and re-armed by the following methods:

- Clearing STATUS bits causing the asserted SMBAlert# signal.
- Power cycling with PSON or with input power
- Masking the event with SMBALERT_MASK

12.1.32   Fan Speed Control

The PSU shall support the PMBus commands to allow the system to control and monitor the PSU's fan.

12.1.33   FAN_CONFIG_1_2 (3Ah)

The FAN_CONFIG_1_2 command is used to define the presence of a fan and the method it is controlled (by duty cycle or RPM).

Table 12-15 FAN_CONFIG_1_2 command

Bits	Value	Meaning
7	1	Fan in position 1
6	0	Fan 1 commanded in Duty Cycle
5:4	Not used	
3	0	Far or No fan in position 2
2	Not used	
1:0	Not used	

12.1.34   FAN_COMMAND_1 (3Bh)

The system may increase the power supplies fan speed through using the FAN_COMMAND_1 command. This command can only increase the power supplies fan speed; it cannot decrease the PSU fan speed below what the PSU commands.

The control is configured to be duty cycle controlled using the linear format of the PMBus protocol. The exponent N is fixed to a value of 0 (N = 0).

12.1.35   READ_FAN_SPEED_1 (90h)

The system will read the fan speed by using the READ_FAN_SPEED_1 command. This data shall return the fan speed in the PMBus linear format.

12.1.36   PSU Commands Supported For Testing Purposes

The PSU shall support the following (optional but recommended) commands for PSU testing purposes only (such as PMBus test, CLST & SmaRT test).

12.1.37   OT_WARN_LIMIT (51h)

The PSU shall allow the system to set new values to the warning threshold for the hot spot temperature sensor using the READ_TEMPERATURE_2 command, in degree Celsius. The two data bytes are formatted in the Linear Data format.

This may be used by the system test FW to simulate an assertion of the SMBAlert# signal due to a temperature warning event. This value shall be reset to the default value with any input power cycle or PSON power cycle.

12.1.38   IOUT_OC_WARN_LIMIT(4Ah)

The IOUT_OC_WARN_LIMIT command sets the value of the output current that causes an output over-current warning. The two data bytes are formatted in the Linear Data format. This may be used by the system test FW to simulate an assertion of the SMBAlert# signal due to an over-current warning event.

12.1.39   Modification to 10.2.6 and 10.3 of PMBus Part II revision 1.2

Some changes/clarifications to the PMBus revision 1.2 specification as stated in this section to allow compatibility with server systems.

12.1.40   PMBUS_REVISION

This is a correction to the table in the PMBus part II specification regarding the PMBUS_REVISION command.

Table 12-16 PMBUS_REVISION command

Bits [7:4]	Part I revision		Bits [3:0]	Part II Revision
0000	1.0		0000	1.0
0001	1.1		0001	1.1
0010	1.2		0010	1.2

12.1.41   Continuous Assertion After Clearing If Condition Is Still Present

If the warning or fault condition is present when a bit is cleared, the bit and associated SMABLERT# signal stays asserted with no momentary transition to a de-asserted state.

12.1.42   Conceptual View of How Status Bits and SMBAlert# Work

Figure 12-7 and *Figure 12-8* show conceptual schematics of how the status bits and SMBALERT# are to function. When a warning or fault event is detected a latch is set. The output of this latch becomes the status bit in the lower level status register (such as STATUS_INPUT). The latch output is OR'ed with other status bits in this command to create the corresponding bit in STATUS_BYTE or STATUS_WORD. The output of the latch is also used to drive the SMBALERT# circuitry. The output of the latch passed through a gate controlled by the corresponding SMBALERT_MASK bit. If this bit is set, the output of the latch is blocked from driving the SMBALERT# circuit. If the SMBALERT_MASK bit is cleared, the latch output is allowed to pass and drive the SMBALERT# circuit. When the SMBALERT# sees the rising edge of the latch output it asserts the SMBALERT# signal (output goes low). The SMBALERT# signal remains asserted until it is cleared. Note the behavior of the latch output and the SMBALERT_MASK. If the latch output is set, and the SMBALERT_MASK bit is changed from set to clear, the latch output is passed to the SMBALERT# circuit and will cause the SMBALERT# signal to assert. If this not desired, the latch must be cleared before clearing the SMBALERT_MASK bit. As described above, the latch can be cleared by writing a 1 to corresponding bit in the status register. It can also be cleared with the CLEAR_FAULTS command.

Commands to clear a bit are gated by the PAGE command. CLEAR_FAULTS can be made to clear all faults on all pages by setting the page command to FFh. Conceptually the bit clearing commands act as pulses, driving the reset pin on the latch only momentarily. This means that if the event is ongoing (the event detector is still active) the output latch will stay asserted (1). This will cause the SMBALERT# to also stay asserted (or stay low) if the event is ongoing and the SMBALERT_MASK bit is not set. This also means that a host won't be able to see the status bit get cleared. If a host sends the command to clear a status bit and then reads the bit as set, it should interpret that to mean that the event is still happening.
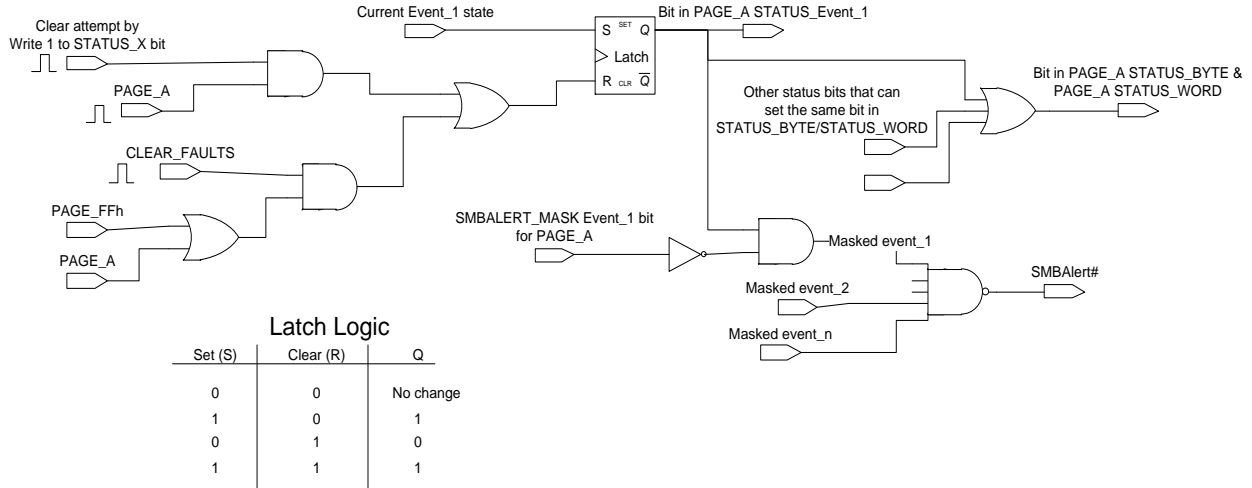
*Figure 12-7 Conceptual Schematic of STATUS bits and SMBAlert# for commands that support PAGE_PLUS_*
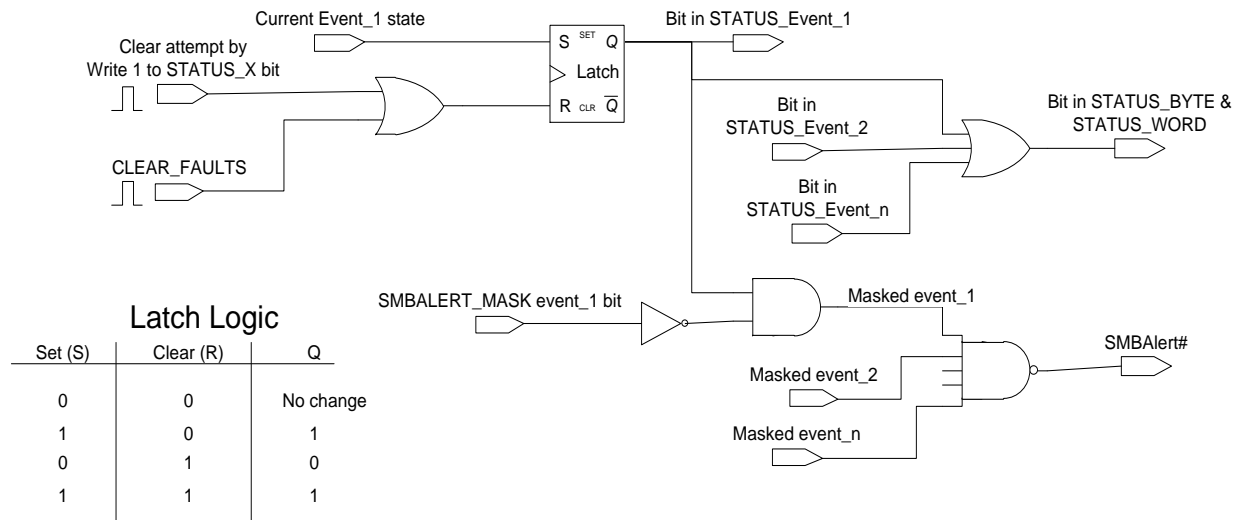
*Figure 12-8 Conceptual schematic of STATUS bits and SMBAlert# without PAGE_PLUS_*

12.1.43   MFR_MAX_IOUT_CAPABILITY (F1h)

The PSU shall provide the Current levels that can support along with their durations for the system to read using a Block Read command with a length of 14 bytes + PEC. The contents of each field are described in the following table.

Table 12-17 MFR_MAX_IOUT_CAPABILITY ccommand

Field name	Size (Bytes)	Magnitude
Irating (PL1)	2	Amperes
Ipeak (PL2)	2	Amperes
Ipeak (PL2) duration	2	ms
Ipeak.pl3 (PL3)	2	Amperes
Ipeak.pl3 (PL3) duration	2	ms
Ipeak.pl4 (PL4)	2	Amperes
Ipeak.pl4 (PL4) duration	2	us

Note: Fields with 0 as value means not supported for a given level.
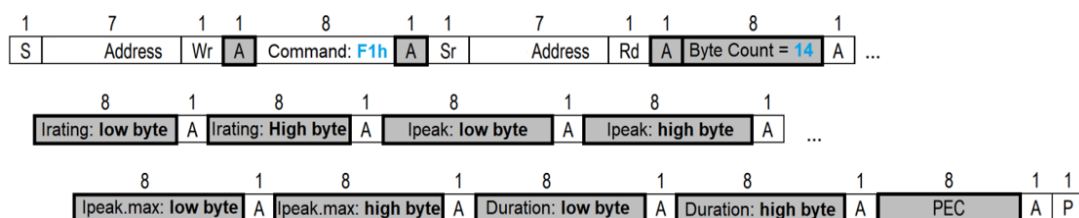
Figure 12-9 MFR_MAX_IOUT_CAPABILITY command

12.1.44   Summary of PMBus commands

Table 12-18 Summary of PMBus commands

Code	Pages	Command	SMBus Transaction Type Status bit mapping
00h		PAGE	
01h		OPERATION	
02h		ON_OFF_CONFIG	
03h	NA	CLEAR_FAULTS	Send Byte w/PEC
05h	NA	PAGE_PLUS_WRITE (used with STATUS_WORD, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE)	Block Write w/PEC Used with STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT
06h	NA	PAGE_PLUS_READ (used with STATUS_WORD, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE)	Write Block Read Block Process Call w/PEC Used with STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT, STATUS_WORD
10h		WRITE_PROTECT	
11h		STORE_DEFAULT_ALL	
12h		RESTORE_DEFAULT_ALL	
15h		STORE_USER_ALL	
16h		RESTORE_USER_ALL	
19h	NA	CAPABILITY	Read Byte w/PEC
1Ah	NA	QUERY (used with any command)	Block Write Block Read Process Call w/ PEC
1Bh	NA	SMBALERT_MASK (used with STATUS_INPUT, STATUS_TEMPERATURE, STATUS_IOUT)	Reading: Write Block Read Block Process Call w/PEC Writing: Write Word
20h		VOUT_MODE	
21h		VOUT_COMMAND	
22h		VOUT_TRIM	
24h		VOUT_MAX	
25h		VOUT_MARGIN_HIGH	
26h		VOUT_MARGIN_LOW	
27h		VOUT_TRANSITION_RATE	
28h		VOUT_DROOP	
29h		VOUT_SCALE_LOOP	
2Ah		VOUT_SCALE_MONITOR	
30h	NA	COEFFICIENT (used with READ_EIN)	Block Write Block Read Process Call w/PEC
33h		FREQUENCY_SWITCH	

35h		VIN_ON	
36h		VIN_OFF	
38h		IOUT_CAL_GAIN	
39h		IOUT_CAL_OFFSET	
3Ah	NA	FAN_CONFIG_1_2	
3Bh	NA	FAN_COMMAND_1	
40h		VOUT_OV_FAULT_LIMIT	
41h		VOUT_OV_FAULT_RESPONSE	
42h		VOUT_OV_WARN_LIMIT	
43h		VOUT_UV_WARN_LIMIT	
44h		VOUT_UV_FAULT_LIMIT	
45h		VOUT_UV_FAULT_RESPONSE	
46h		IOUT_OC_FAULT_LIMIT	
47h		IOUT_OC_FAULT_RESPONSE	
4Ah	NA	IOUT_OC_WARN_LIMIT	Write Word / Read Word w/PEC
4Fh		OT_FAULT_LIMIT	
50h		OT_FAULT_RESPONSE	
51h	NA	OT_WARN_LIMIT (used to support testing CLST)	Write word w/PEC
55h		VIN_OV_FAULT_LIMIT	
56h		VIN_OV_FAULT_RESPONSE	
57h		VIN_OV_WARN_LIMIT	
58h		VIN_UV_WARN_LIMIT	
59h		VIN_UV_FAULT_LIMIT	
5Ah		VIN_UV_FAULT_RESPONSE	
5Dh		IIN_OC_WARN_LIMIT	
6Bh		PIN_OP_WARN_LIMIT	
78h		STATUS_BYTE	
79h	00h, 01h	STATUS_WORD	Read Word w/PEC
(Low) 6		OFF	PS off
4		IOUT_OC	Indeterminate (Use STATUS_IOUT)
2		TEMPERATURE	Indeterminate (Use STATUS_TEMPERATURE)
3		VIN_UV	Indeterminate (Use STATUS_INPUT)
1		CML	
(High) 7		VOUT	Failure
6		IOUT/POUT	Indeterminate (Use STATUS_IOUT)
5		INPUT	Indeterminate (Use STATUS_INPUT)
4		MFR_SPECIFIC (Incompatible Power Supply)	
3		POWER_GOOD#	
2		FANS	Indeterminate (Use STATUS_FANS)
7Ah	NA	STATUS_VOUT	Read Byte w/PEC
7		VOUT_OV_FAULT	Failure
4		VOUT_UV_FAULT	Predictive failure
7Bh	00h, 01h	STATUS_IOUT	Read Byte w/PEC

7		Iout OC fault	Failure
5		Iout OC warning	Pedictive failure
1		Pout OP fault	Failure
0		Pout OP warning	Pedictive failure
7Ch	00h, 01h	STATUS_INPUT	Read Byte w/PEC
5		Vin UV warning	Predictive failure
4		Vin UV fault	AC Loss
3		Unit off for insufficient input	AC Loss
1		Iin over current warning	Predictive failure
0		Pin over power warning	Predicitve failure
7Dh	00h, 01h	STATUS_TEMPERATURE	Read Byte w/PEC
7		OT fault	Fault
6		OT warning	Predicitve fault
81h	00h	STATUS_FANS_1_2	Read Byte w/PEC
7		Fan 1 fault	Failure
6		Fan 2 fault	Failure
5		Fan 1 warning	Pedictive failure
4		Fan 2 warning	Predicitive failure
7Eh		STATUS_CML	
7Fh		STATUS_OTHER	
80h		STATUS_MFR_SPECIFIC	
81h		STATUS_FANS_1_2	
86h	NA	READ_EIN	Block Read w/ PEC
87h	NA	READ_EOUT	Block Read w/ PEC
88h		READ_VIN	
89h		READ_IIN	
8Ah		READ_VCAP	
8Bh		READ_VOUT	
8Ch	NA	READ_IOUT	Read Word w/PEC
8Dh	NA	READ_TEMPERATURE_1 (Ambient)	Read Word w/PEC
8Eh	NA	READ_TEMPERATURE_2 (Hot Spot)	Read Word w/PEC
8Fh		READ_TEMPERATURE_3	
90h	NA	READ_FAN_SPEED_1	Read Word w/PEC
91h		READ_FAN_SPEED_2	
94h		READ_DUTTY_CYCLE	
96h		READ_POUT	
97h	NA	READ_PIN	Read Word w/PEC
98h	NA	PMBUS_REVISION	Read Byte w/PEC
99h		MFR_ID	
9Ah	NA	MFR_MODEL	Block Read
9Bh	NA	MFR_REVISION	Block Read
9Ch		MFR_LOCATION	
9Dh		MFR_DATE	
9Eh		MFR_SERIAL	

9Fh	NA	APP_PROFILE_SUPPORT	Read Byte w/PEC
A0h		MFR_VIN_MIN	
A1h		MFR_VIN_MAX	
A2h		MFR_IIN_MAX	
A3h		MFR_PIN_MAX	
A4h		MFR_VOUT_MIN	
A5h		MFR_VOUT_MAX	
A6h	NA	MFR_IOUT_MAX	Read Word w/PEC
A7h	NA	MFR_POUT_MAX	Read Word w/PEC
A8h		MFR_TAMBIENT_MAX	
A9h		MFR_TAMBIENT_MIN	
ADh		IC_DEVICE_ID	
AEh		IC_DEVICE_REV	
B0h		USER_DATA_00	
B1h		USER_DATA_01	
B2h		USER_DATA_02	
B3h		USER_DATA_03	
B4h		USER_DATA_04	
B8h		USER_DATA_08	
C0h	NA	MFR_MAX_TEMP_1 (Ambient)	Read Word w/PEC
C1h	NA	MFR_MAX_TEMP_2 (hot Spot)	Read Word w/PEC
C2h		MFR_MAX_TEMP_3	
D0h	NA	MFR_COLD_REDUNDANCY_CONFIG	Read/Write Byte w/PEC
D1h		MFR_SPECIFIC_01	To be used by this spec
D2h		MFR_SPECIFIC_02	To be used by this spec
D3h		MFR_SPECIFIC_03	To be used by this spec
D4h	NA	MFR_HW_COMPATIBILITY	Read Word w/PEC
D5h	NA	MFR_FWUPLOAD_CAPABILITY	Read Byte w/PEC
D6h	NA	MFR_FWUPLOAD_MODE	Read/Write Byte w/PEC
D7h	NA	MFR_FWUPLOAD	Bloack Write w/ PEC (size = block size from image header)
D8h	NA	MFR_FWUPLOAD_STATUS	Read Word w/PEC
D9h	NA	MFR_FW_REVISION	Block Read w/PEC (3 bytes)
DAh		MFR_SPECIFIC_10	To be used by this spec
DBh	NA	MFR_FRU_PROTECTION	Read/Write byte w/PEC
DCh	NA	MFR_BLACKBOX	Block Read w/ PEC (230 byes)
DDh	NA	MFR_REAL_TIME_BLACK_BOX	Block Write/Read w/ PEC (4 bytes)
DEh	NA	MFR_SYSTEM_BLACK_BOX	Block Write/Read w/ PEC (40 bytes)
DFh		MFR_SPECIFIC_15	To be used by this spec
E0h		MFR_SPECIFIC_16	To be used by this spec
E1h		MFR_SPECIFIC_17	To be used by this spec
E2h		MFR_SPECIFIC_18	To be used by this spec
E3h		MFR_SPECIFIC_19	To be used by this spec
E4h		MFR_SPECIFIC_20	To be used by this spec

E5h		MFR_SPECIFIC_21	To be used by this spec
E6h		MFR_SPECIFIC_22	To be used by this spec
E7h		MFR_SPECIFIC_23	To be used by this spec
E8h		MFR_SPECIFIC_24	To be used by this spec
E9h		MFR_SPECIFIC_25	To be used by this spec
EBh		MFR_SPECIFIC_27	To be used by this spec
ECh		MFR_SPECIFIC_28	To be used by this spec
EFh		MFR_SPECIFIC_31	To be used by this spec
F0h		MFR_SPECIFIC_32	To be used by this spec
F1h		MFR_SPECIFIC_33	To be used by this spec
F2h		MFR_SPECIFIC_34	To be used by this spec
F3h		MFR_SPECIFIC_35	To be used by this spec
F4h		MFR_SPECIFIC_36	To be used by this spec
F5h		MFR_SPECIFIC_37	To be used by this spec
EDh		MFR_SPECIFIC_29	To be used by this spec
F0h	NA	MFR_PWOK_WARNING_TIME	Read/Write Word w/PEC
F1h	NA	MFR_MAX_IOUT_CAPABILITY	Block Read w/PEC (14 bytes)

12.2 Thermal Closed Loop System Throttling (Thermal CLST)

The power supply shall assert the SMBAlert# signal whenever any component in the power supply selected by the configuration file reaches a temperature warning threshold. Upon reduction of the load within 2msec after the SMBlert# signal is asserted if the load is reduced to less than the power supply rating; the power supply shall continue to operate and not shutdown.
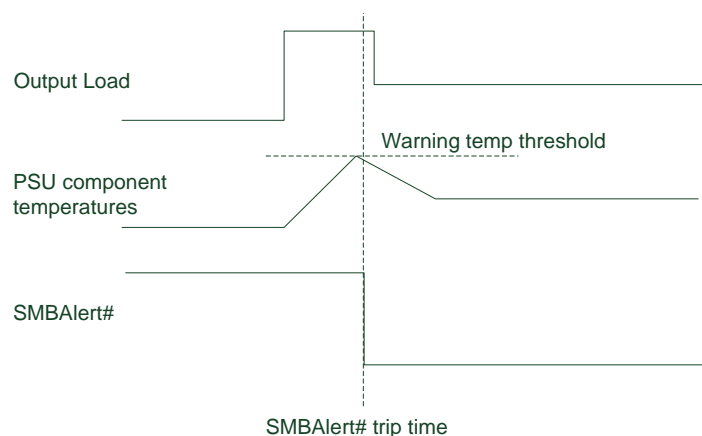
Figure 12-10 Thermal CLST timing requirements

12.3 Smart Ride-Through (SmaRT)

The power supply shall assert the SMBAlert# signal in less than the specified time in table below after AC/DC input voltage is lost to 0VAC/0VDC to throttle the system/load and allow longer hold-up time.

Table 12-19 SMBAlert# input lost delay time

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Power supply input type	SMBAlert# delay
High voltage AC/DC (240VAC/240VDC or 277VAC/380VDC)	>500us and <2ms
Low voltage +54VDC (Rack power)	< 100us
Low voltage -48VDC (Telecom)	< 100us

Note: The SMBAlert# assertion due to input lost condition can be enabled/disabled in the configuration file.

12.4 Cold Redundancy

This is a common specification defining Cold Redundancy requirements used in redundant power supplies. It covers both power supply and system requirements supporting redundant configurations of 1+1, 2+2, and 3+1. Cold Redundancy uses the PMBus manufacturer specific command area to define SMBus commands for the system to communicate with the power supplies for enabling, configuration, and monitoring.

When configured as Cold Redundant, the power supply shall have a maximum input power as specified in table below.

Table 12-20 Maximum input power when configured as Cold Redundant mode

4 Watts

Note: Input power shall be measured at the lowest nominal input voltage.

12.4.1 Overview

Below is a block diagram showing the Cold Redundancy architecture. When the power subsystem is in Cold Redundant mode; only the needed power supply to support the best power delivery efficiency are ON. Any additional power supplies: including the redundant power supply, is in Cold Standby state.

Each power supply has an additional signal that is dedicated to supporting Cold Redundancy; CR_BUS. This signal is a common bus between all power supplies in the system. CR_BUS is asserted (pulled low) when there is a fault in any power supply OR the power supplies output voltage falls below the Vfault threshold. Asserting the CR_BUS signal causes all power supplies in Cold Standby state to power ON.

Enabling power supplies to maintain best efficiency is achieved by looking at the Load Share bus voltage and comparing it to a programmed voltage level via a PMBus command.

Whenever there is no Cold Redundant active power supply on the Cold Redundancy bus driving a HIGH level on the bus all power supplies are ON no matter their defined Cold Redundant role (active or Cold Standby). This guarantees that incorrect programming of the Cold Redundancy states of the power supply will never cause the power subsystem to shutdown or become over loaded. The default state of the power subsystem is all power supplies ON. There needs to be at least one power supply in Cold Redundant Active state or Standard Redundant state to allow the Cold Standby state power supplies to go into Cold Standby state.
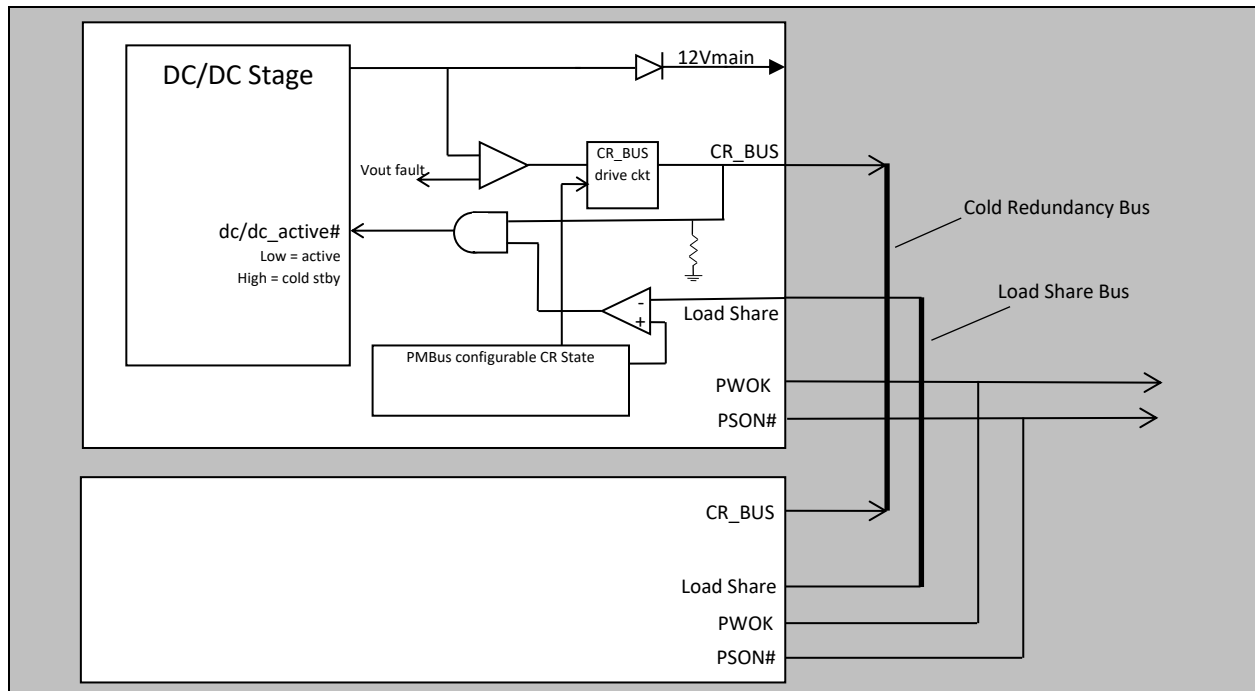
Figure 12-11 Cold Redundancy 1+1 functional block diagram
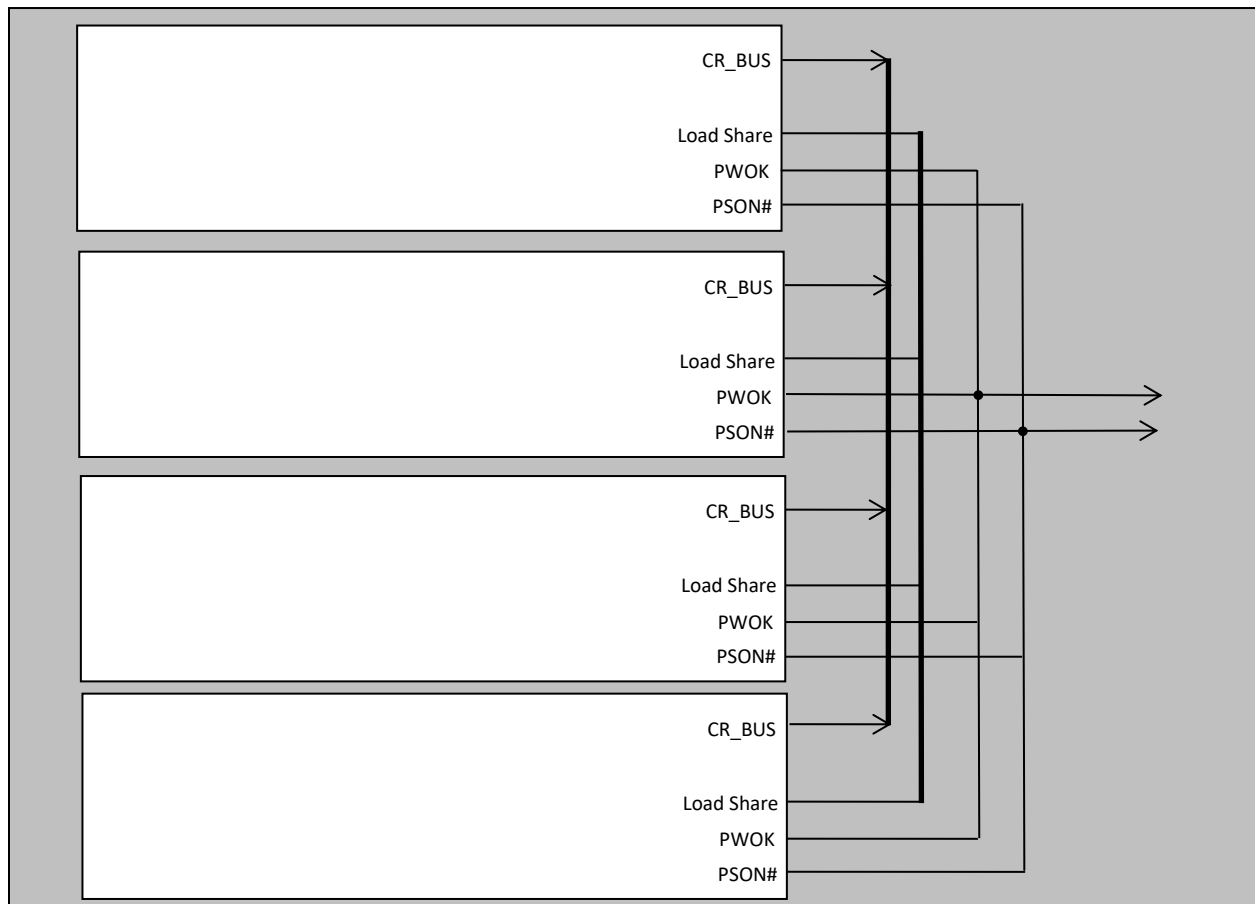
Figure 12-12 Cold Redundancy 2+2 & 3+1 functional block diagram

Table 12-21 Logic matrix for Cold Standby power supplies

CR_BUS	Load Share	dc/dc_active#	Cold Standby Power Supply State(s)
High	< V_{CR_ON}	High	Cold Standby
Low	< V_{CR_ON}	Low	Active
High	> V_{CR_ON}	Low	Active
Low	> V_{CR_ON}	Low	Active

12.4.2 Cold Standby Power Supply Operating State

A power supply is put into Cold Standby whenever PSON# is asserted, CR_ON# is de-asserted, and COLD_RED_CONFIG value is set to 02h, 03h, or 04h. In the cold standby mode, the power supply must:

1. Power ON in < 100µsec when Cold_Red bus is driven LOW
2. Turn off its output OR'ing FET
3. Keep its internal output capacitor before the output OR'ing FET charged to not less than 12.6V
4. Keep PWOK asserted
5. Disconnect any output dummy loads to prevent discharging of the recharged output capacitor
6. Power off any internal fans
7. Pre-bias its voltage error amplifier to maximum duty cycle (preventing the loop compensation from slowing up the turn on process)
8. Disable its output slow start circuit
9. Keep the PFC stage ON at lowest possible operating frequency and its output bulk capacitor charged
10. No PMBus fault or warning conditions reported via STATUS commands

12.4.3 Powering on Cold Standby Supplies to Maintain Best Efficiency

Power supplies in Cold Standby state shall monitor the shared voltage level of the load share signal to sense when it needs to power on. Depending upon which position (1, 2, 3, etc.) the system defines that power supply to be in the cold standby configuration; will slightly change the load share threshold that the power supply shall power on at. The CR_BUS of any power supply may be in one of three different states; pulled low, pulled high, or tri-stated. In tri-state the CR_BUS is a high impedance to ground; only a high impedance resistor pulling the signal to ground.

Table 12-22 Example load share threshold for activating supplies

	Enable Threshold for $V_{CR\_ON\_EN}$	Disable Threshold for $V_{CR\_ON\_DIS}$	CR_BUS De-asserted / Asserted States
Standard Redundancy	NA; Ignore dc/dc_ active# signal; power supply is always ON		OK = Tri-state Fault = Low
Cold Redundant Active	NA; Ignore dc/dc_ active# signal; power supply is always ON		OK = High Fault = Low
Cold Standby 1 (02h)	3.2V (40% of max)	90% x (3.2V x 1/2) = 1.44V	OK = Tri-state Fault = Low
Cold Standby 2 (03h)	5.0V (62% of max)	90% x (5.0V x 2/3) = 3.01V	OK = Tri-state Fault = Low
Cold Standby 3 (04h)	6.7V (84% of max)	90% x (6.7V x 3/4) = 4.52V	OK = Tri-state Fault = Low

Notes:
1. Maximum load share voltage = 8.0V at 100% of rated output power.
2. These are example load share bus threshold; for any power supply model these thresholds could be customized to maintain the best efficiency curve that specific model.
3. The defined thresholds can be change using the configuration file.

12.4.4 Powering on Cold Standby Supplies During a Fault or Over Current Condition

When an active power supply asserts its CR_BUS signal (pulling it low), all parallel power supplies in cold standby mode shall power on within 100μsec.

12.4.5 Cold Redundancy SMBus Commands

The PMBus manufacturer specific command MFR_SPECIFIC_00 is used to configure the operating state of the power supply related to cold redundancy. The command shall be called COLD_REDUNDANCY_CONFIG (D0h). Below is the definition of the values used with the Read-Write Byte SMBus protocol with PEC.

The power supplies setup to be the cold standby power supplies; shall change to standard redundancy mode (D0h = 00h) whenever the CR_BUS is pulled low.

Table 12-23 COLD_REDUNDANCY_CONFIG (D0h) values

Value	State	Description
00h	Standard Redundancy (default power on state)	Turns the power supply ON into standard redundant load sharing more. The power supply's CR_BUS signal shall be in Tri-state but still pull the bus low if a fault occurs to activate any power supplies still in Cold Standby state.
01h	Cold Redundant Active [1]	Defines this power supply to be the one that is always ON in a cold redundancy configuration.
02h	Cold Standby 1 [1]	Defines the power supply that is first to turn on in a cold redundant configuration as the load increases.
03h	Cold Standby 2 [1]	Defines the power supply that is second to turn on in a cold redundant configuration as the load increases.
04h	Cold Standby 3 [1]	Defines the power supply that is third to turn on in a cold redundant configuration as the load increases.
05h	Always Standby [1]	Defines this power supply to be always in cold redundant configuration no matter what the load condition.
06h -– FFh	reserved	

Notes:
1. When the CR_BUS transitions from a high to a low state; each PSU programmed to be in Cold Standby state shall be put into Standard Redundancy mode (COLD_REDUNDANCY_CONFIG = 00h). For the power supplies to enter Cold Redundancy mode the system must re-program the power supplies using the COLD_REDUNDANCY_CONFIG command.

12.4.6 Cold Redundant Signals

There is an additional signal defined supporting Cold Redundancy. This is connected to a bus shared between the power supplies; the CR_BUS.

12.4.7 Cold Redundancy Bus (CR_BUS)

This is a tri-state output signal of the power supply used to communicate a fault or over current has occurred in one of the power supplies. This is used to power on all the power supplies in the system via the CR_BUS. When the signal is pulled high it allows all power supplies in cold standby mode to go into cold standby state when the load is light enough. When the signal I left open on all power supplies it forces them all cold standby power supplies ON.

Table 12-24 CR_BUS state table

Cold Redundant Config	Operating State	PSU Fault State	CR_BUS
Active	On	OK	High
Cold Standby 1,2,3	On	OK	Tri-state
Cold Standby 1,2,3	Cold Stby	OK	Tri-state
Always standby	Cold Stby	OK	Tri-state
Active	Off	Fault	Low
Cold Standby 1,2,3	On	Fault	Low
Cold Standby 1,2,3	Cold Stby	Fault	Low
Always standby	Cold Stby	Fault	Low
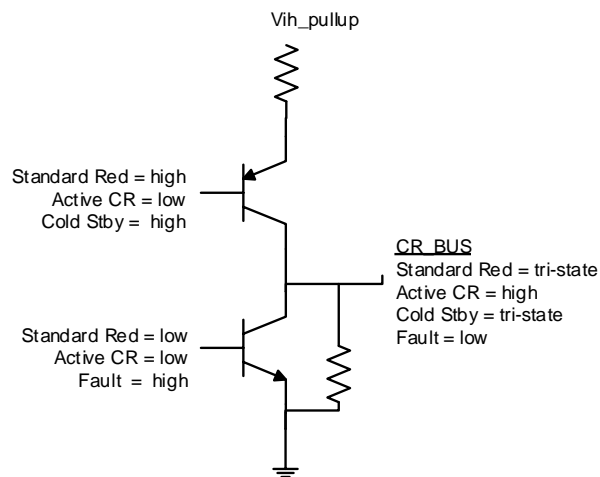
Figure 12-13 CR_BUS signal circuit

Table 12-25 CR_BUS signal characteristics

Parameter	Value	
Signal type	Custom	
	MIN	MAX
Logic level low (power supply ON)	0V	Vil_cr_bus
Logic level high (power supply OFF)	Vih_cr_bus	
Source current, Cold Red = high	Ioh_cr_bus	

Sink current, Cold_Red = low		Iol_cr_bus
Cold_Red fault delay		10 µs
Cold_Red turn on delay		100 µs

12.4.8 System BMC Requirements

The BMC uses the COLD_REDUNDANCY_CONFIG command to define/configure the power supply's roll in cold redundancy and to turn on/off cold redundancy.

The BMC shall schedule a rolling change for which PSU is the Active, Cold Stabdby1, Cold Standby 2, and Cold Standby 3 power supply. The allows for equal loading across power supply over their life.

Events that trigger a re-configuration of the power supplies using the COLD_REDUNDANCY_CONFIG command.
- AC power ON
- PSON power ON
- Power Supply Failure
- Power supply inserted into system

12.4.9 Power Supply Turn ON Function

Powering ON and OFF of the cold standby power supplies is only controlled by each PSU sensing the Ishare bus. Once a power supply turns on after crossing the enable threshold; it lowers its threshold to the disable threshold. The system defines the 'position' of each power supply in the Cold Redundant operation. It will do this each time the system is powered on, a power supply fails, or a power supply is added to the system.

The system is relied upon to tell each power supply where it resides in the Cold Redundancy scheme.

When load ramps up and crosses the CR threshold module wake up time must be <3ms (tbd)
When load ramps down and crosses the CR threshold module go-to-sleep (sdby) time must be <5ms

Table 12-26 Cold Redundancy reaction delays

Parameter	Value
CR Threshold for wake-up	< 3ms[1]
CR Threshold for sleep-mode (Standby)	< 5ms[2]

Notes:
1. When load represented by the Ishare bus ramps up and crosses the CR wake-up threshold.
2. When the load represented by the Ishare bus ramps down and crosses the CR go-to-sleep (standby) threshold.
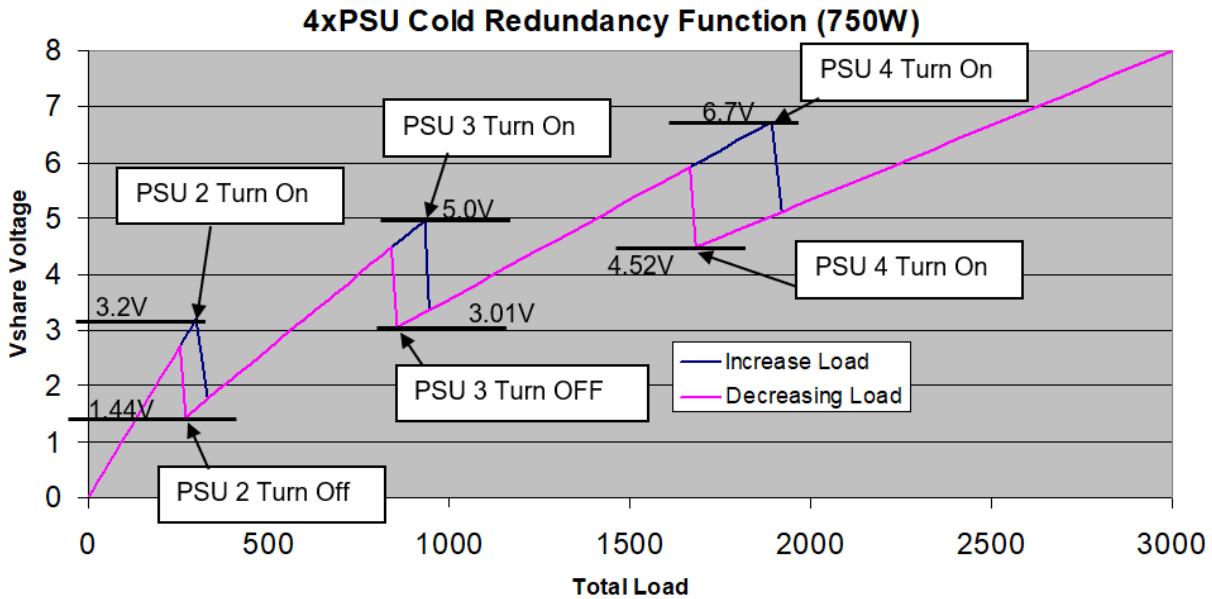
Figure 12-14 Power ON/OFF example of power supplies in Cold Redundant mode (4x750W PSUs)

12.5 In-System Firmware Upload

This specification defines the common architecture for in-system power supply firmware updates. It is required that the FW in the main microcontroller on the secondary side of the power supply must be able to be updated in the system using the In-System Firmware Update feature while in the ON state (i.e. with AC power present and PSON# asserted). Any other microcontroller in the power supply also shall be able to be updated with this same process (example: primary side microcontroller).

12.5.1 FW Image Mapping

The power supply firmware image shall be made up of two parts; 1) Boot loader; 2) Main program. The system shall contain a backup of the power supply image in its BMC whenever updating the FW to the power supply.

1. Boot Loader: This is the part of the power supply firmware that is never updated by the system. The power supply shall always be able to recover and power ON into the boot loader mode no matter the state of the power supply's main program. This code shall support the In-System FW update code and basic power supply functions to power ON/OFF, fan cooling, and protections (UV, OV, OC).
2. Main Program: This is the fully functional power supply program space. There is no requirement to keep a backup image of this code in the power supply since a copy of the power support FW image shall always for kept in the system's BMC.

12.5.2 Summary of Commands & Capabilities Supported in Bootloader Mode

When the power supply is in FW Upload mode the following commands shall be supported.

Table 12-27Supported commands during FW upload mode

Code	Command	SMBus Transaction Type
19h	CAPABILITY	Read Byte w/PEC
1Ah	QUERY (used with any command)	Block Write Block Read Process Call w/ PEC

98h	PMBUS_REVISION	Read Byte w/PEC
9Ah	MFR_MODEL	Block Read
D4h	MFR_HW_COMPATIBILITY	Read Word w/PEC
D5h	MFR_FWUPLOAD_CAPABILITY	Read Byte w/PEC
D6h	MFR_FWUPLOAD_MODE	Read/Write Byte w/PEC
D7h	MFR_FWUPLOAD	Bloack Write w/ PEC (size = block size from image header)
D8h	MFR_FWUPLOAD_STATUS	Read Word w/PEC
D9h	MFR_FW_REVISION	Block Read w/PEC (3 bytes)
Basic Function	Operating Capability	
Fan control	Fan can run at a high fixed speed to make sure power supply is cooled in the system for the duration of the FW update.	
PWOK	The PWOK signal must still function properly during power on / off cycles to reset the system	
PSON#	The PSON# signal must still be able to power ON/OFF the power supply.	
UV	Under voltage protection	
OV	Over voltage protection	
OC	Over current protection	

12.5.3 LED Status

While the PSU FW image is being updated the PSU shall blink using a pattern selected in the LED behavior configuration block of the configuration file, see *12.8.3.1 LED Behavior Configuration Block* for details.

12.5.4 Power Supply Operating Mode During and After Firmware Update

Firmware update mode in ON state with no power cycle needed:
Power supply may be able to support FW upload in the ON state. The new FW will take effect once it is taken out of FW upload load.

Bad image after firmware update:
The power supply must always be able to power on in the boot loader mode with minimal operating capabilities even if the FW image sent to the power supply is bad or corrupt. If in this mode, the power supply must be able to still enter the FW upload mode to upload a proper FW image to the PSU.

12.5.5 Firmware Image Header

The power supply's FW image shall contain a header at the beginning of the file as described in the table below.

Table 12-28 PSU FW Image header

Byte 1	CRC LowByte
Byte 2	CRC HighByte
Byte 3	Image Information
Byte 4	Image Information

Byte 5	Image Information
Byte 6	Image Information
Byte 7	Image Information
Byte 8	Image Information
Byte 9	Image Information
Byte 10	Image Information
Byte 11	M
Byte 12	-
Byte 13	C
Byte 14	R
Byte 15	P
Byte 16	S
Byte 17	
Byte 18	M
Byte 19	O
Byte 20	D
Byte 21	E
Byte 22	L
Byte 23	
Byte 24	FW_MAJOR (Bit 7: down revision control bit, Bit 0-6: Major version).
Byte 25	FW_MINOR_PRIMARY (not used by system)
Byte 26	FW_MINOR_SECONDARY
Byte 27	HW_COMPATIBILITY_FIRST
Byte 28	HW_COMPATIBILITY_SECOND
Byte 29	BLOCK SIZE LowByte
Byte 30	BLOCK SIZE HighByte
Byte 31	Write Time LowByte
Byte 32	Write Time HighByte

12.5.6 Firmware Update Process

IMPORTANT!
- PSU may be in standby mode or ON mode during FW update process
- If the FW update process is interrupted at any point during the process; the PSU must always be able to return to the boot loader code.
- The PSU must always check that the application program is not corrupted before starting to run from the application program
- During the FW upload process the PSU must always respond to any communication on the bus; acknowledging its address and the supporting commands without holding the bus. For unsupported boot loader commands the PSU may respond with Not Acknowledge or 00h.
- BMC must configure correct addresses into ME at BMC startup to avoid bad PSU address config if AC power is lost or BMC is reset while the PSU update is in progress

BMC uses these commands to determine of FW needs updating:
MFR_FW_REVISION
MFR_MODEL
MFR_FW_UPLOAD_MODE
MFR_HW_COMPATIBILITY
MFR_FW_UPLOAD_CAPABILITY

BMC determines PSU FW needs updating? — No → PSU stays in application program mode

Yes

BMC resets retry counter

BMC put PSU into Boot Load mode sends 0x01 to MFR_FWUPLOAD_MODE

Increment retry count

Delay 1s to allow PSU to enter FW update mode

PSU starts to run off of Boot Loader code (PSU may erase application memory at this time but it is preferred to wait for the MFR_FW_UPLOAD command to start erasing the application program)

BMC reads MFR_FWUPLOAD_MODE = 0x01? — No → Max retry reached? (default = 3) — Yes → EXIT

No

Yes

BMC reads FW image header in BMC for block size and delay time

BMC sends MFR_FWUPLOAD & 1st block of image

PSU writes CRC16 (byte 1 & 2 of image) to memory

PSU erases part of application memory & write the 1st image block

Write time delay

BMC sends MFR_FWUPLOAD & next block of image

PSU erases part of application memory & writes the next block of image

Write time delay

(optional) BMC reads MFR_FW_UPLOAD_STATUS

(optional) Block received OK? — No

Last data block? — No

Yes

PSU verifies that the image has been transferred properly by checking the CRC16 value

BMC reads MFR_FW_UPLOAD_STATUS

Full image received successfully? — No → BMC writes 00h to MFR_FW_UPLOAD_MODE → Max retry reached? Default = 3 — Yes → BMC writes 00h to MFR_FW_UPLOAD_MODE

No

Yes

BMC writes 00h to MFR_FW_UPLOAD_MODE

BMC sets "config error" offset of PSU status sensor

BMC reads MFR_FW_UPLOAD_MODE = 0 — No / Yes

PSU stays in boot loader mode

PSU starts running from application program

PSU application program OK? — No / Yes

PSU verifies Application Program is not corrupted with CRC16 value

Figure 12-15 FW update process

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12.5.7 Power Supply Commands

Name: MFR_HW_COMPATIBILITY
Format: Read Word
Code: D4h

Table 12-29 MFR_HW_COMPATIBILITY command format

Bytes	Value	Description
low	ASCI code for first letter/number of the PSU HW compatibility.	This is a COMPATIBILITY value used to tell if there are any changes in the FW that create an incompatibility with the FW. This value only changes when the PSU HW is changed creating an incompatibility with older versions of FW.
high	ASCI code for second letter/number of the PSU HW compatibility.	

Name: MFR_FWUPLOAD_CAPABILITY
Format: Read Byte
Code: D5h

The system can read the power supply's FW upload mode capability using this command. For any given power supply, more than one FW upload mode may be supported. The supported FW upload mode(s) must support updating all available FW in the power supply.

Table 12-30 MFR_FWUPLOAD_CAPABILITY command format

Bit	Value	Description
0 (for future use)	1 = PSU support FW uploading in standby mode only	For future use
1 (for future use)	1 = PSU supports FW uploading in ON state; but all the new FW will not take effect until a power cycle with PSON.	For future use
2	1 = PSU supports FW uploading in the ON state and no power cycle needed	Method used for updating the application program in the power supply
3-7	Reserved	

Name: MFR_FWUPLOAD_MODE
Format: Read/Write Byte
Code: D6h

Table 12-31 MFR_FWUPLOAD_MODE command format

Bit	Value	Description
0	0 = exit firmware upload mode 1 = firmware upload mode	Writing a 1 puts the power supply into firmware upload mode and gets it ready to receive the 1st image block via the MFR_FW_UPLOAD command. The system can use this command at any time to restart sending the FW image. Writing a 0 puts the power supply back into normal operating mode. Writing a 1 restarts This command will put the PSU into standby mode if the PSU supports FW update in standby mode only. If the power supply image passed to the PSU is corrupt the power supply shall stay in firmware upload mode even if the system requested the PSU to exit the FW upload mode.
1-7		Reserved

Name: MFR_FWUPLOAD
Format: Block Write (block = size as defined by the image header)
Code: D7h

Table 12-32 MFR_FWUPLOAD command format

Bytes	Value	Description
Block size defined in header	Image header & image data	Command used to send each block of the FW image.
		Header should follow the format described in S*ection 12.5.5 Firmware Image Header*
		The image shall contain block sequencing numbers to make sure the PSU puts the right data blocks into the right memory space on the PSU MCU.

Name: MFR_FWUPLOAD_STATUS
Format: Read Word
Code: D8h

At any time during or after the firmware image upload the system can read this command to determine status of the firmware upload process.
Reset: all bits get reset to '0' when the power supply enters FW upload mode.

Table 12-33 MFR_FWUPLOAD_STATUS command format

Bit	Description
0	1 = Full image received successfully
1	1 = Full image not received yet. The PSU will keep this bit asserted until the full image is received by the PSU.
2	1 = Full image received but image is bad or corrupt. Power supply can power ON, but only in 'safe mode' with minimal operating capability.
3 (for future use)	1 = Full image received but image is bad or corrupt. Power supply can power ON and support full features.
4	1 = FW image not supported by PSU. If the PSU receives the image header and determines that the PSU HW does not support the image being sent by the system; it shall not accept the image and it shall assert this bit.
5 – 15	Reserved

Name: MFR_FW_REVISION
Format: Block Read, 3 bytes
Code: D9h

Table 12-34 MFR_FW_REVISION command format

Byte	Value	Description
0	0 - 255	Minor revision; secondary
1	0 - 255	Minor revision; primary
2	0 - 255	Bit 7: 1-> Down grading of PSU FW must be avoided. System BMC can elect to ignore this bit if needed but recommended to follow.
		0→ No restriction in downgrading the PSU FW. BMC can update the PSU FW to be in sync with its known version.
		Bit 0-6: Major revision

Name: MFR_MODEL (existing PMBus command)
Format: Block Read, Maximum of 12-byte value; ending in terminator character
Code: 9Ah

Name: MFR_REVISION (existing PMBus command)
Code: 9Bh

12.6 Black Box

This specification defines the requirements for power supplies with PMBus capability to store PMBus and other data into non-volatile memory inside the power supply. The data shall be saved to non-volatile memory upon a critical failure that caused the power supply to shutdown. The data can be accessed via the PMBus interface by applying power to the 12VSB pins. No AC power need to be applied to the power supply.

12.6.1 When is Data Saved to the Black Box?

Data is saved to the Black Box for the following fault events:

- General fault
- Over voltage on output
- Over current on output
- Loss of AC input
- Input voltage fault
- Fan failure
- Over temperature

12.6.2 Black Box Events

There are two types of data saved in the Black Box; 1) System Tracking Data, 2) Power supply event data. System tracking data is saved to the Black Box whenever the system powers ON or when a power supply is added to the system.

12.6.3 Black Box Process

- System writes system tracking data to the power supply RAM at power ON
- System writes the real time clock data to the PSU RAM once every ~5 minutes
- Power supply tracks number of PSON and AC power cycles in EEPROM
- Power supply tracks ON time in EEPROM
- Power supply loads warning and fault event counter data from EEPROM into RAM
- Upon a warning event, the PSU shall increment the associated counter in RAM.
- Upon and fault event the PSU shall increment the associated counter in RAM
- Upon a fault event that causes the PSU to shutdown all event data in the PSU's RAM is saved to event data location N in the power supply's EEPROM. This data includes the real time clock, number of AC & PSON power cycles, PSU ON time, warning event counters and fault event counters.

12.6.4 Commands

Command name: MFR_BLACKBOX

Format: Read Block with PEC (238 bytes)
Code: DCh

Table 12-35 MFR_BLACKBOX record format

Field	Item	Number of Bytes	Description
System Tracking Data	System top assembly number	10	The system will write its part number for the system top assembly to the power supply when it is powered ON. This is 9 ASCI characters.
	System serial number	10	The system shall write the system serial number to the power supply when it is powered ON. This include the serial number and date code.
	Motherboard assembly number	10	The system will write the motherboard part number for the assembly to the power supply when it is powered ON. This is 9 ASCI characters.
	Motherboard serial number	10	The system shall write the motherboard's serial number to the power supply when it is powered ON. This includes the serial number and date code.
	Present total PSU ON time	3	Total on time of the power supply with PSON asserted in minutes. LSB = 1 minute.
	Present number of AC power cycles	2	Total number of times the power supply powered OFF then back ON due to loss of AC power. This is only counted when the power supply's PSON# signal is asserted. This counter shall stay at FFFFh once the max is reached.
	Present number of PSON power cycles	2	Total number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting. This is only counted when AC power is present to the power supply. This counter shall stay at FFFFh once the max is reached.
Power supply event data (N)		38	Most recent occurrence of saved black box data
Time Stamp			The power supply shall track these time and power cycle counters in RAM. When a Black Box event occurs, the data is saved into the Black Box.
	Power supply total power on time	3	Total on time of the power supply in minutes. LSB = 1 minute.
	Real Time Clock Data from System (Reserved for future use)	4	This time stamp does not need to be generated by the power supply. The system rights a real time clock value periodically to the power supply using the MFR_REAL_TIME command. Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long-standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C
	Number of AC power cycles	2	Number of times the power supply powered OFF then back ON due to loss of AC power at

			the time of the event. This is only counted when the power supply's PSON# signal is asserted.
	Number of PSON power cycles	2	Number of times the power supply is powered OFF then back ON due to the PSON# signal de-asserting at the time of the event. This is only counted when AC power is present to the power supply.
PMBus			The power supply shall save these PMBus values into the Black Box when a black box event occurs. Fast events may be missed due to the filtering effects of the PMBus sensors.
	STATUS_WORD	2	
	STATUS_IOUT	1	
	STATUS_INPUT	1	
	STATUS_TEMPERTATURE	1	
	STATUS_FAN_1_2	1	
	READ_VIN	2	
	READ_IIN	2	
	READ_IOUT	2	
	READ_TEMPERATURE_1	2	
	READ_TEMPERATURE_2	2	
	READ_FAN_SPEED_1	2	
	READ_PIN	2	
	READ_VOUT	2	
Event Counters			The power supply shall track the total number for each of the following events. This value shall be saved to the Black Box when a Black Box event occurs. Once a value has reached 15, it shall stay at 15 and not reset.
	AC shutdown due to under voltage on input	Lower ½	The power supply shall save a count of these critical events to non-volatile memory each time they occur. The counters will increment each time the associated STATUS bit is asserted.
	Thermal shutdown	Upper ½	
	Over current or over power shutdown on output	Lower ½	
	General failure shutdown	Upper ½	
	Fan failure shutdown	Lower ½	
	Shutdown due to over voltage on output	Upper ½	
	Input voltage warning; no shutdown	Lower ½	The power supply shall save into RAM a count of these warning events. Events are count only at the initial assertion of the event/bit. If the event persists without clearing the bit the counter will not be incremented. When the power supply shuts down it shall save these warning event counters to non-volatile memory. The counters will increment each time the associated STATUS bit is asserted.
	Thermal warning; no shutdown	Upper ½	
	Output current power warning; no shutdown	Lower ½	
	Fan slow warning; no shutdown	Upper ½	
Power supply event data (N-1)		38	
Power supply event data (N-2)		38	
Power supply event data (N-3)		38	
Power supply event data (N-4)		38	

Command name: MFR_REAL_TIME_BLACK_BOX
Format: Write/Read Block with PEC (4 bytes)
Code: DDh

The system shall use this command to periodically write the real time clock data to the power supply. Format is based on IPMI 2.0. Time is an unsigned 32-bit value representing the local time as the number of seconds from 00:00:00, January 1, 1970. This format is sufficient to maintain time stamping with 1-second resolution past the year 2100. This is based on a long-standing UNIX-based standard for time keeping, which represents time as the number of seconds from 00:00:00, January 1, 1970 GMT. Similar time formats are used in ANSI C.

Command name: MFR_SYSTEM_BLACK_BOX
Format: Write/Read Block with PEC (40 bytes). Low byte first.
Code: DEh

The system uses this command to write the following data to the PSU.

Table 12-36 MFR_SYSTEM_BLACK_BOX command format

Item	Bytes	Comments
System top assembly number	1-10	Low bytes
System serial number	11-20	
Motherboard assembly number	21-30	
Motherboard serial number	31-40	High bytes

Command name: MFR_BLACKBOX_CONFIG
Format: Read/Write Byte with PEC
Code: DFh

Table 12-37 MFR_BLACKBOX_CONFIG command format

Bit	Value	Description
0	0 = disable black box function 1 = enable black box function	Writing a 1 enables the power supply with black box function. Writing a 0 disables the power supply black box function. The state of MFR_BLACKBOX_CONFIG shall be saved in non-volatile memory so that it is not lost during power cycling. The customer shall receive the power supply with the black box function enabled; bit 0 = '1'.
1-7		reserved

Command name: MFR_CLEAR_BLACKBOX
Format: Send Byte with PEC
Code: E0h

The MFR_CLEAR_BLACKBOX command is used to clear all black box records simultaneously.
This command is write only. There is no data byte for this command.

12.6.5 Hardware Requirements

The SMBus interface shall be used to access the Black Box data. It may be accessed when the power supply is ON or in standby mode. It also may be accessed when no AC power is applied, and power is only applied at the standby output pins by an external source (12VSB).

12.7 Data & Sideband Serialization Interface (DSSI)

This specification defines the requirements for a Modular Common Redundant Power Supply (M-CRPS) Data & Sideband Serialization Interface (DSSI) communication protocol along with its different profiles. DSSI is a one-wire bi-directional protocol created to avoid the need of a higher pin count output interface connector in the power supply. Instead of using individual pints in the output interface connector DSSI is used to serialize those I/O signals and have a host interface in which a MCU or FPGA can be placed to send and retrieve this information and execute the appropriate action.

12.7.1 Physical Layer

The DSSI Protocol requires a physical layer that comprises an UART element, and the input/out circuit shown in below figure, for both the host and the client as shown in the figure below.
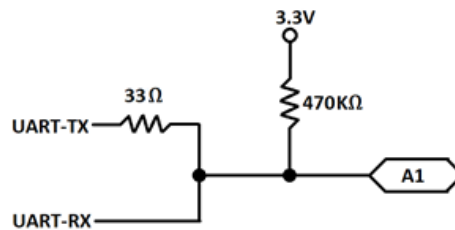
Figure 12-16 Required physical layer in the power supply for data serialization interface

The connection between a Client and a Host is shown below
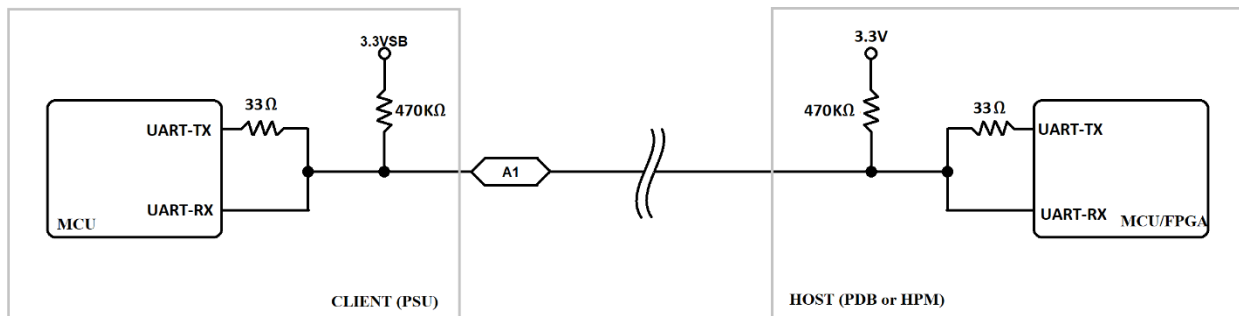
Figure 12-17 Physical layer and connections for point-to-point communication between Host and Client

12.7.2 Default configuration

The UART module used for the DSSI protocol shall be configured by default at boot time with the parameters shown in the table below.

Table 12-38 DSSI UART configuration

Parameter	
Signal type	Bi-directional 3.3V Totem-Pole Logic
Communication protocol	Half-duplex UART

Port settings	• Data bits: 8 • Parity: Odd • Stop bits: 1 • Flow control: None
Link speed	250,000 bps

Note: UART shall be capable of enable/disable its transmitter when is in listening mode.

12.7.3 Electrical Characteristics

Table 12-39 DSSI electrical characteristics

Parameter	Value
Source/Sink current	TBD
Rise time	TBD
Fall time	TBD
Maximum load capacitance	TBD

12.7.4 Protocol

At boot time the S-WIRE signal shall be sustained in logic 1 stablishing an IDLE state. DSSI communication is always initiated by the Host device when data needs to be sent/retrieved. The Host device could set the proper communication settings if the default settings do not satisfy the communication preference of the Host

Profile configuration shall be done after communication settings, the available profiles are described in *Section 12.7.6 Profiles.*

To provide a deterministic behavior the data is transferred from and to the Host following the timing diagrams shown below.
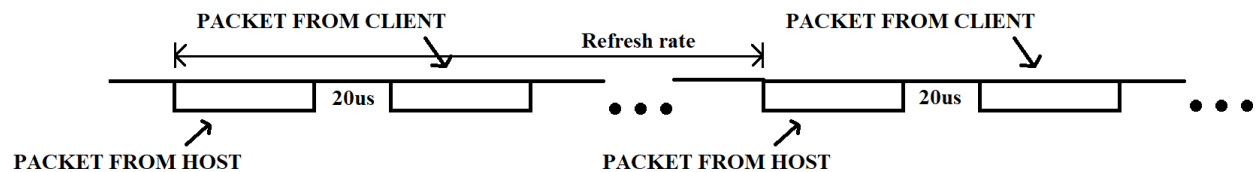
Figure 12-18 Timing diagram for bi-directional DSSI protocol.

Note: The Host shall always initiate the communication to send/retrieve data from the Client.

The protocol is divided in configuration commands, reply packets, and data packets. The configuration command is depicted in the following figure.
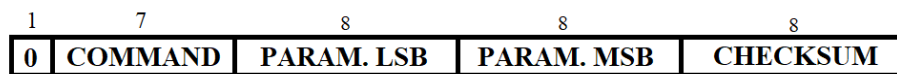
Figure 12-19 Configuration command packet structure.

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Note: MSb of the first byte is always 0 in a configuration command since the Host is the only one allowed to send a command to a client.

The Client shall reply to the configuration commands from the Host with the reply packet structure as shown in the figure below.
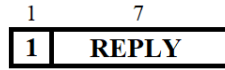
Figure 12-20 Reply packet structure.

12.7.5 Command Set

The total amount of commands is 127 (7Fh), the defined commands are listed in the following table.

Figure 12-21 Configuration commands set.

Command (Hex)	Parameter	Reply	Description
BREAK SEQ.	None	00h = OK	Restarts the communication to allow reconfiguration.
00h	[15:0] 0 = 62,500 bps 1 = 125,000 bps **2 = 250,000 bps** 3 = 500,000 bps 4 = Reserved …	00h = OK 01h = Not supported 02h = Checksum Error	Change communication baud-rate
01h	[15:8] **0 = bi-directional** 1 = Reserved 2 = Reserved 4 = Reserved … [7:0] **0 = Point-to-point** 1 = Reserved 2 = Reserved …	00h = OK 01h = Not supported 02h = Checksum Error	Communication and connection type selection
02h	[15:0] **0 = Simple GPIO expander** 1 = GPIO expander with addressing capabilities 2 = Reserved …	00h = OK 01h = Not supported 02h = Checksum Error	Profile selection
03h	[15:0] 0 = Reserved **1 = one byte** 2 = two bytes …	00h = OK 01h = Not supported 02h = Checksum Error	Bytes to send from the Host
04h	[15:0] 0 = Reserved **1 = one byte** 2 = two bytes …	00h = OK 01h = Not supported 02h = Checksum Error	Bytes to receive at the Host side
05h	[15:0] **0 = 500us** 1 = 750us 2 = 1ms …	00h = OK 01h = Not supported 02h = Checksum Error	Communication refresh rate
7Eh	[15:0] All zeroes	00h = OK 01h = Not supported 02h = Checksum Error	Start communication

Notes:
1. Bold characters shall be the default options.
2. When the Client's replies "not supported" it will keep the previous configuration.

12.7.6 Profiles

12.7.6.1 Basic GPIO Expander Profile

The data packets shall be divided in two types: one-byte and multi-byte, the structure of the one-byte data packet is shown in figure below.
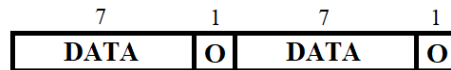
Figure 12-22 One-byte data packet structure

Notes:
1. O bit: 0 = Host originated packet, 1 = Client originated packet.
2. One-byte data packet sends the same byte twice to reduce error probability.
3. Host must send a packet to the Client as specified in the configuration command 03h to retrieve a One-byte packet.

The structure of the multi-byte data packet is shown in the following figure.

Figure 12-23 Multi-byte data packet structure

Notes:
1. O bit: 0 = Host originated packet, 1 = Client originated packet.
2. One-byte data packet sends the same byte twice to reduce error probability.
3. Host must send a packet to the Client as specified in the configuration command 03h to retrieve a One-byte packet.

12.7.6.1.1 Data and Sideband Selection
Define how to select the signals and data to be serialized

12.8 Configuration File

12.8.1 Overview

This section defines the requirements for a Modular Common Redundant Power Supply (M-CRPS) that provides the ability to modify the behavior of the Power Supply based in the following main areas:

- Thresholds for all the implemented protections like Over Current Protection, Over Temperature Protections, etc.
- LED behavior based in different events.

- Embedded executable code like Fan Speed Control algorithms.
- Data tables.

The configuration file shall be in binary format and shall be transferred at the factory line or on field by using the PMBus of the Power Supply and shall be able to update its configuration file in run time mode (live update). Figure 1 shows the four main areas that the configuration file shall be made of: 1) File header, 2) Configuration area, 3) Embedded code area, 4) Data table area.

1. **File Header:** This area contains general information about the file like CRC16, file size, customer name and offsets to other areas.
2. **Configuration area:** This is the part where all the thresholds and timings for the protections and warnings are defined along with the LED behavior based on different events that can happen in the power supply.
3. **Embedded code area:** This area contains executable code to be run by the MCU, this area can be used to have specific fan speed control or debug algorithms.
4. **Data table area:** This area contains customer specific data to be used by the power supply like extra FRU data.
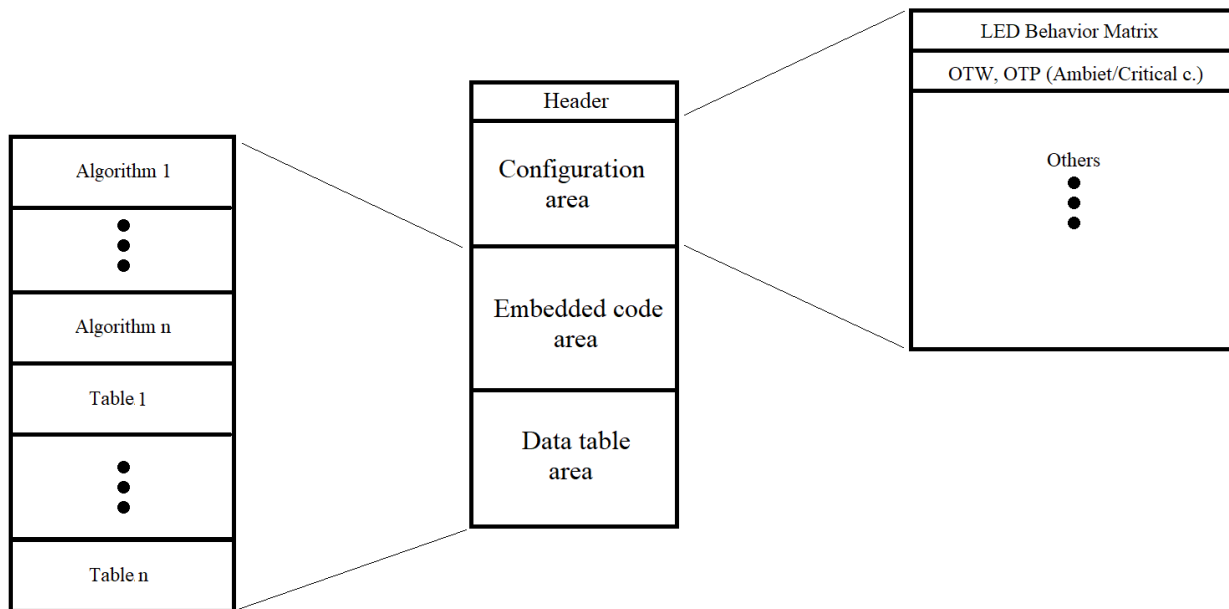
Figure 12-24 Main areas of the configuration file.

The entire configuration file shall be made of an array of 16-bit unsigned values using Little Endian encoding otherwise noted, and the addressing is represented in bytes, as an example the value 1234h is stored at address 0x0020 as follows:

Figure 12-25 Endianess (Little Endian example)

Address	Data
0020h	34h
0021h	12h

The configuration file header shall include the offsets for the beginning of each area, each one of the areas shall be made of a linked list of blocks, each block shall contain an offset to point to the next block, this offset is always an unsigned 16-bit value. A graphical representation of this structure is shown in the following figure.
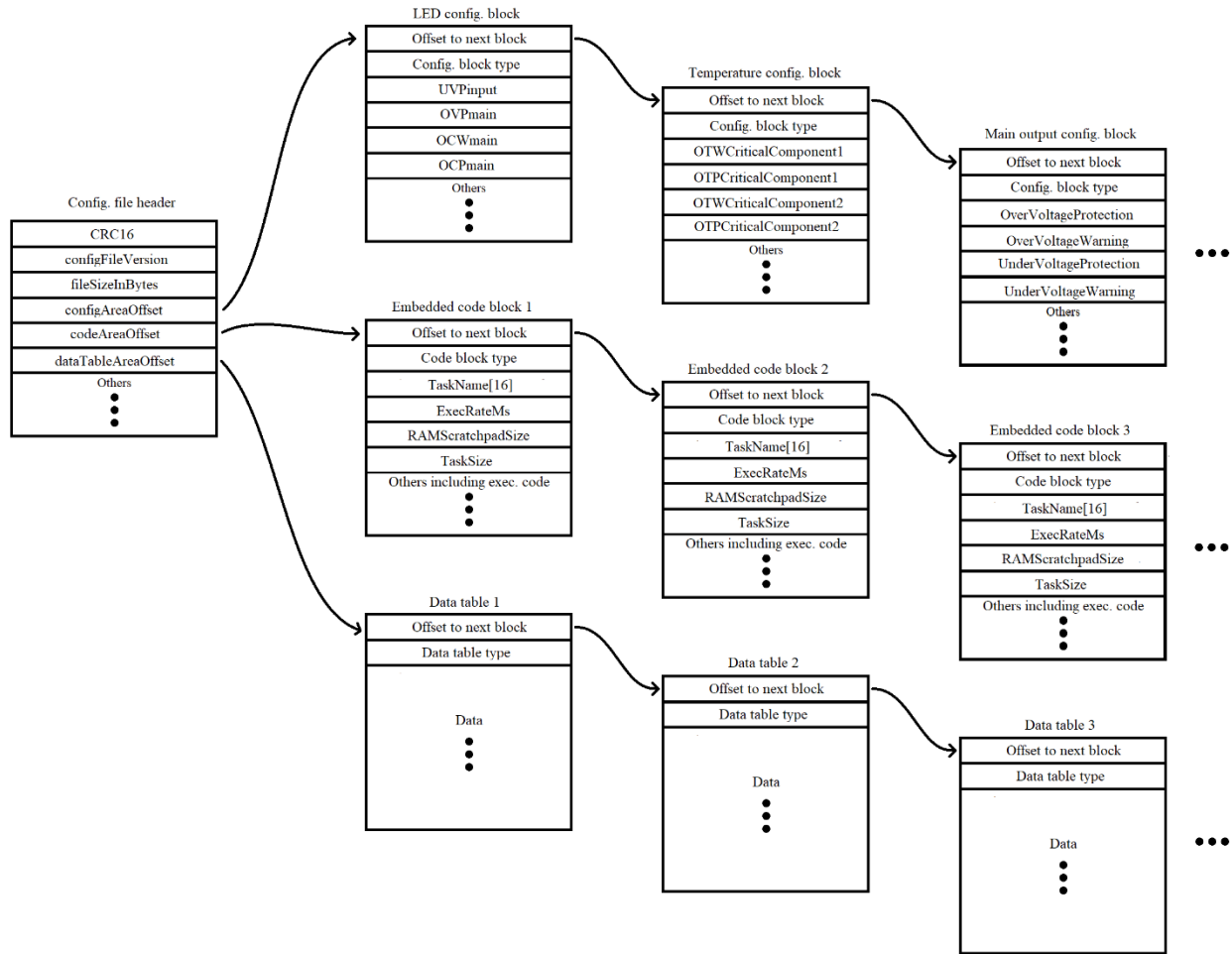
Figure 12-26 Representation of the file header and the different configuration blocks that make the areas

12.8.2 Configuration File Header

The header area shall contain the information shown in the table below.

Table 12-40 Header area

Offset	Element	Description
0000h	CRC16	16-bit CRC, the calculation must exclude the CRC16 field in the file
0002h	configFileVersion	Configuration file version
0004h	fileSizeLow	Size of the entire configuration file in bytes. Least significant 16-bit word
0006h	fileSizeHigh	Size of the entire configuration file in bytes. Most significant 16-bit word
0008h	customerInfo[16]	Customer specific information field. The string "DEFAULT" means the configuration file has the default configurations from the power supply vendor. Null terminated.
0018h	configAreaOffset	Offset in bytes from this location to the beginning of the configuration area
001Ah	codeAreaOffset	Offset in bytes from this location to the beginning of the executable code area
001Ch	dataTableAreaOffset	Offset in bytes from this location to the beginning of the data table area
…	…	…

Note: CRC16 Polynomial is TBD

12.8.3 Configuration Area Definition

The configuration area shall contain the information shown in the table below.

Table 12-41 Configuration block types

Configuration block type	Value
LED Behavior	0001h
Temperature	0002h
Main output	0003h
Standby output	0004h
Input	0005h
Fans	0006h
Timing	0007h
Latch on Fault condition	0008h
Data serialization	0009h
…	…

12.8.3.1 LED Behavior Configuration Block

Table 12-42 LED descriptor

Parameter	Bitfield	Options	Comments
Style	0-2	0 = OFF 1 = ON 2 = Blinking 3 = Blink N times then OFF 4 = Blink N times then ON	
Color	3-5	0 = OFF 1 = GREEN 2 = AMBER	
Flashing Times	6-8	0 = Zero time 1 = One time 2 = Two times …	
Frequency	9-11	0 = Zero Hz 1 = 1 Hz 2 = 2 Hz …	
Reserved	12-15	Reserved	

Table 12-43 Power supply event table

Offset	Event	Description
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block
0002h	configBlockType	Configuration block type based on *Table 12-41 Configuration block types*
0004h	UVPinput	Input Under Voltage Protection
0006h	OVPmain	Main Output Over Voltage Protection
0008h	OCWmain	Main Output Over Current Warning
000Ah	OCPmain	Main Output Over Current Protection
000Ch	OTWcrit	
000Eh	OTWamb	
0010h	OTPamb	
0012h	NonCompatible	
0014h	FWUpgrade	
…	…	…

Note: Values in each one of the events are based on the previous table. LED descriptor.

12.8.3.2 Temperature Configuration Block

Table 12-44 Power supply temperature thresholds

Offset	Event	Description	Resolution
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block	
0002h	configBlockType	Configuration block type based on *Table 12-41 Configuration block types*	
0004h	OTWCriticalComponent1		1 °C
0006h	OTPCriticalComponent1		1 °C
0008h	OTWCriticalComponent2		1 °C
000Ah	OTPCriticalComponent2		1 °C
000Ch	OTWAmbient		1 °C
000Eh	OTPAmbient		1 °C
0010h	OTWExit		1 °C
0012h	OTPExit		1 °C
…	…	…	

Note: The power supply will use a default value depending on its design for any value in the previous table that go beyond the physical limits to avoid damage.

12.8.3.3 Main Output Configuration Block

Table 12-45 Power supply main output's thresholds

Offset	Event	Description	Resolution
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block	
0002h	configBlockType	Configuration block type based on *Table 12-41 Configuration block types*	
0004h	Over Voltage Protection		0.1 Volt
0006h	Over Voltage Warning		0.1 Volt
0008h	Under Voltage Protection		0.1 Volt
000Ah	Under Voltage Warning		0.1 Volt
000Ch	Over Power Protection		1 Watt
000Eh	Over Power Warning		1 Watt
0010h	Over Current Protection		0.1 Ampere
0012h	PL4 Level		0.1 Ampere
0014h	PL4 Duration		1 us
0016h	PL3 Level		0.1 Ampere
0018h	PL3 Duration		1 ms
001Ah	PL2 Level		0.1 Ampere
001Ch	PL2 Duration		1 ms
001Eh	PL1 Level		0.1 Ampere
0020h	PL1 Duration		1 ms

Notes:
1. The power supply will use a default value depending on its design for any value in the previous table that go beyond the physical limits to avoid damage.
2. A value of 0 (Zero) in any of the Duration fields will indicate that the power supply shall not wait to trigger the event.

12.8.3.4 Standby Output Configuration Block

Table 12-46 Power supply standby output's thresholds

Offset	Event	Description	Resolution
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block	
0002h	configBlockType	Configuration block type based on *Table 12-41 Configuration block types*	
0004h	Over Voltage Protection		0.1 Volt
0006h	Over Voltage Warning		0.1 Volt
0008h	Under Voltage Protection		0.1 Volt
000Ah	Under Voltage Warning		0.1 Volt
000Ch	Over Power Protection		1 Watt
000Eh	Over Power Warning		1 Watt
0010h	Over Current Protection		0.1 Ampere
0012h	PL2 Level		0.1 Ampere
0014h	PL2 Duration		1 ms
0016h	PL1 Level		0.1 Ampere
0018h	PL1 Duration		1 ms
…	…	…	…

Notes:

1. The power supply will use a default value depending on its design for any value in the previous table that go beyond the physical limits to avoid damage.
2. A value of 0 (Zero) in any of the Duration fields will indicate that the power supply shall not wait to trigger the event.

12.8.3.5 Input Configuration Block

Table 12-47 Power supply input thresholds

Offset	Event	Description	Resolution
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block	
0002h	configBlockType	Configuration block type based on *Table 12-41 Configuration block types*	
0004h	Over Voltage Protection		0.1 Volt
0006h	Over Voltage Warning		0.1 Volt
0008h	Under Voltage Protection		0.1 Volt
000Ah	Under Voltage Warning		0.1 Volt
000Ch	Over Power Protection		1 Watt
000Eh	Over Power Warning		1 Watt
0010h	Over Current Protection		0.1 Ampere
0012h	Over Current Warning		0.1 Ampere
…	…	…	…

Notes:

1. The power supply will use a default value depending on its design for any value in the previous table that go beyond the physical limits to avoid damage.
2. A value of 0 (Zero) in any of the Duration fields will indicate that the power supply shall not wait to trigger the event.

12.8.3.6 Fans Configuration Block

Table 12-48 Power supply fans thresholds

Offset	Event	Description	Resolution
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block	

0002h	configBlockType	Configuration block type based on *Table 12-41 Configuration block types*	
0004h	Fan1FaultLowRPM		1 RPM
0006h	Fan1FaultLowRPMDelay		1 ms
0008h	Fan1MinRPM		1 RPM
000Ah	Fan1MaxRPM		1 RPM
000Ch	Fan2FaultLowRPM		1 RPM
000Eh	Fan2FaultLowRPMDelay		1 ms
0010h	Fan2MinRPM		1 RPM
0012h	Fan2MaxRPM		1 RPM
…	…	…	…

Notes:

1. The power supply will use a default value depending on its design for any value in the previous table that go beyond the physical limits to avoid damage.

12.8.3.7 Timing Configuration Block

Table 12-49 Power supply timing configuration

Offset	Event	Description	Resolution
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block	
0002h	configBlockType	Configuration block type based on *Table 12-41 Configuration block types*	
0004h	Toff_latch		1 ms
0006h	Tpson_on_delay		1 ms
0008h	Tpwok_on		
000Ah	Tpwok_off		
000Ch	Tpwok_low		
000Eh	InputLostToSMBAlertDelay		1 ms
0010h	InputLostToVINOKDelay		1 ms
0012h	InputRegainToVINOKDelay		1 ms
0014h	InputTurnONVoltage		0.1 Volt
0016h	InputTurnOFFVoltage		0.1 Volt
0018h	InputAvrgCycles		AC cycles
…	…	…	…

Notes:

1. The power supply will use a default value depending on its design for any value in the previous table that go beyond the physical limits to avoid damage.

12.8.3.8 Latch on Fault Condition Configuration Block

Table 12-50 Power supply latch on fault condition configuration block

Offset	Event	Description	Resolution
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block	
0002h	configBlockType	Configuration block type based on *Table 12-41 Configuration block types*	
0004h	MainOutputOCP		
0006h	MainOutputOVP		
0008h	MainOutputUVP		
000Ah	MainOutputOPP		
000Ch	StbyOutputOCP		
000Eh	StbyOutputOVP		
0010h	StbyOutputUVP		

0012h	StbyOutputOPP		
0014h	InputOCP		
0016h	InputOVP		
0018h	InputUVP		
001Ah	InputOPP		
001Ch	AmbientTempOTP		
001Eh	CritComponent1TempOTP		
0020h	CritComponent2TempOTP		
0022h	ExitTempOTP		
0024h	FanFault		

12.8.3.9 Black Box Save on Fault/Warning Condition Configuration Block
To be defined

12.8.3.10 Miscellaneous Configuration Block
To be defined

12.8.3.11 Data & Sideband Serialization Interface Configuration Block
To be defined

12.8.4 Embedded Code Area Definition
The configuration file shall have an embedded executable code area so the user-defined code can be run. The endianness of the executable area will depend on the MCU's endianness. Each one of the embedded code blocks shall include an offset pointing to the next block and the type of embedded code base in the following table.

Table 12-51 Embedded executable code block types

Executable code block type	Value
Fan speed control	0001h
Over temperature	0002h
Output over current	0003h
Input voltage	0004h
Data serialization	0005h
Debug	0006h
…	…

Depending on the type of embedded executable code listed in the previous table the return structure will change accordingly, the definition of each return structure is defined on each one of the following subsections.

12.8.4.1 Executable Code Block Definition

Table 12-52 Power supply event table

Offset	Event	Description
0000h	offsetToNextBlock	Offset in bytes from this location to the beginning of the next configuration block
0002h	codeBlockType	Configuration block type based on *Table 12-51 Embedded executable code block types*
0004h	TaskName[16]	String with the code block name, null terminated
0006h	ExecRateMs	Execution rate of the task in milli-seconds
0008h	RAMScratchpadSize	Amount of RAM needed by the executable code block in bytes

000Ah	TaskSize	Size of the executable code block in bytes
000Ch	executableCode	Beginning of the executable code
…	…	…

12.8.5 Data Table Area Definition

To be defined

12.8.6 Configuration File Creation
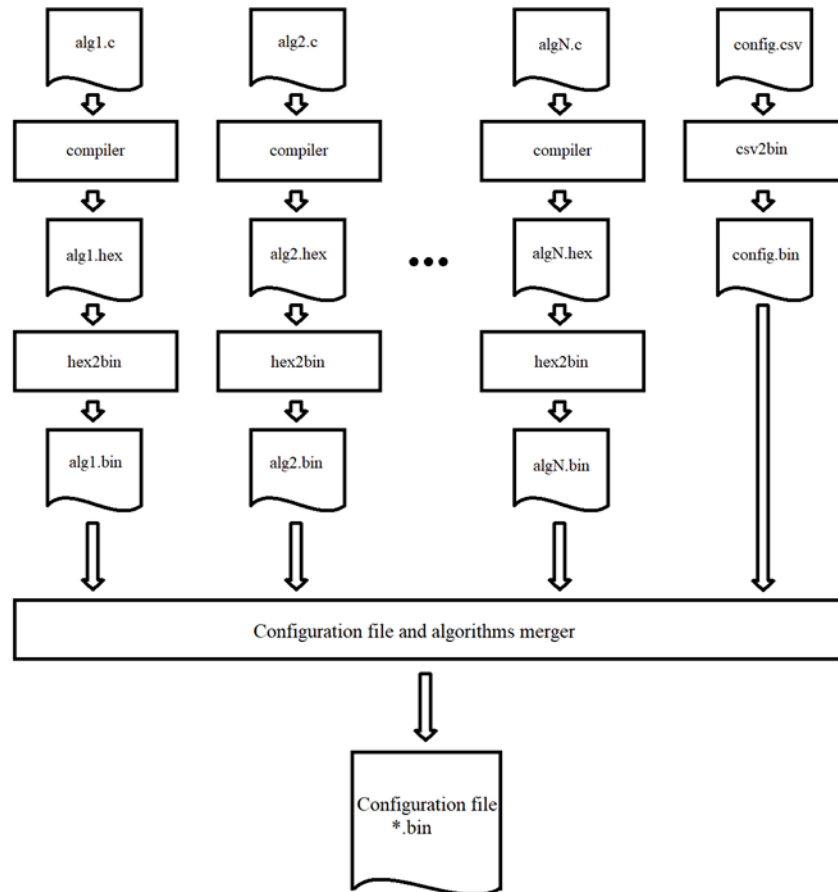
Figure 12-27 Configuration file creation graphical representation

12.9 Security

The M-CRPS shall support Firmware attestation and signed images using RSA-256 algorithm as well as measurements.

12.9.1 Measurement

To be defined

12.9.2 Firmware Attestation

To be defined

13 Reliability

13.1 Component De-Rating

A component derating analysis shall be completed in accordance with internal derating procedure which based on Electronic Derating for Optimum Performance by Reliability Analysis Center (RAC). A limited life component identification and analysis shall be performed on all aluminum electrolytic capacitors or any other potentially limited life components used in the design of the assembly. The latest supplier's equation shall be used to calculate capacitor life expectancy. Internal tool maybe utilized with an NDA in place, access will be monitored and controlled by tool administrator.

https://didtweb.com/login.aspx?ReturnUrl=%2fdefault.aspx
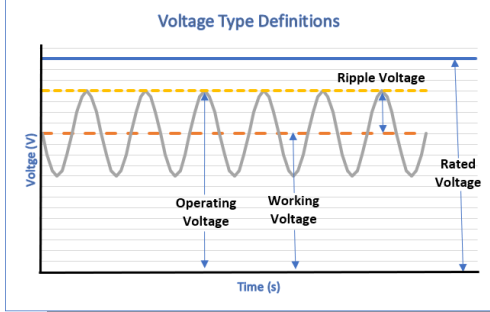
Test Conditions
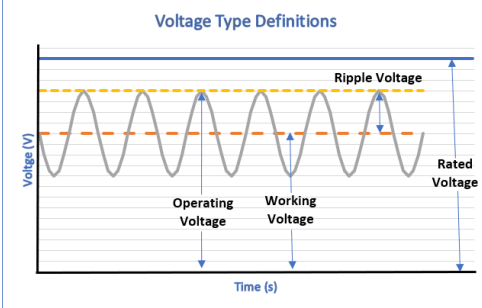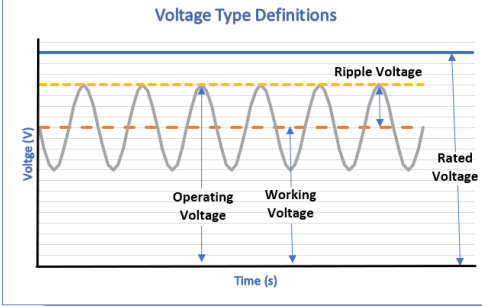
- Multiple sources shall be included in this analysis
- All components used in PSU shall be qualified in accordance with the appropriate JEDEC standard as well as Internal Component Engineering qualification procedures and requirements
- Input Voltage: Nominal (HL $200V_{AC} - 240V_{AC}$; LL $100V_{AC} - 120V_{AC}$)
- Output current: 80%, 100% full load on all rails including standby.
- Inlet Ambient Temperature: Max Ambient (per Safety submittal conditions of the Design Specification)
- Altitude: Sea Level
- Back Pressure: 0" of H_2O
- Pass/Fail Criteria
  - PSU shall comply with internal Component Derating Specification at ≤80% load
  - Components shall not exceed specs limits at >80% & ≤100% load

The following component de-rating guidelines shall be followed. Any exceptions are subject to final approval.

Table 13-1 Component de-rating guidelines

Component Type	Parameter	Derating Criteria
Capacitors		
Aluminum Liquid Capacitor (Fixed Aluminum Liquid Electrolyte Type)	DC Voltage	85%
	Ambient Rated Temperature	≥105°C
	Minimum life determined using worst-case operating condition for the capacitor and 100% System Duty Cycle.	See below for detail
	Rated Ripple Current (no adjustment for frequency or temperature factors)	80%
	Minimum Life	7 years
	High Voltage Bulk Storage Cap Max Voltage (>200V) at peak steady state conditions.	100%

Component Type	Parameter	Derating Criteria
Aluminum Solid Capacitor (Fixed Aluminum Solid Electrolyte Type (includes Organic Semi-conductive (OSCON), Conductive Polymer, Solid Aluminum))	Applied DC Voltage (Working Voltage) AC Ripple + DC (Operating Voltage)	80% 95%
	Ambient Rated Temperature	≥105°C
	Maximum measured Case Temp below Ambient Rated Temperature	Tmax - 15°C
	Minimum life calculated using worst-case operating condition for the capacitor and 100% System Duty Cycle.	See below for detail
	Ripple Current	80%
	Minimum Life	7 years
Aluminum Hybrid Capacitor (Fixed Aluminum Hybrid Electrolytic Type)	DC Voltage	85%
	Ambient Rated Temperature	≥105°C
	Minimum life determined using worst-case operating condition for the capacitor and 100% System Duty Cycle.	See below for detail
	Rated Ripple Current (no adjustment for frequency or temperature factors)	80%
	Minimum Life	7 years
	High Voltage Bulk Storage Cap Max Voltage (>200V) at peak steady state conditions.	100%
Tantalum Capacitor (Fixed Solid Tantalum Type)	Working DC Voltage:	30%
	Ambient Rated Temperature	≥105°C
	Maximum Case Temperature below Max Ambient Limit	Tmax - 20°C
	Ripple Current	70%
	Reverse Voltage (% of Forward Voltage)	2%
Ceramic Capacitor (Fixed Ceramic – Pin Through Hole (PTH))	DC Voltage	85%
	Ambient Temperature	Tmax - 10°C
MLCC (Fixed Multilayer Ceramic Capacitors – Surface Mount Device (SMD))	All Applications and Temperature Ratings Requirements: DC Voltage	85%
	Ambient Temperature	Tmax - 10°C
	Additional Power and Critical Function Applications Requirements: Ambient Rated Temperature	≥105°C
	Surface temp Max	
	105°C Ambient rated	90°C
	125°C Ambient rated	110°C

Component Type	Parameter	Derating Criteria
MLPC (Multilayer Polymer Aluminum Capacitor)	Applied DC Voltage (Working Voltage) AC Ripple + DC (Operating Voltage) 	80% 95%
	Ambient Rated Temperature	≥105°C
	Maximum measured Case Temp below Ambient Rated Temperature	Tmax - 15°C
	Minimum life calculated using worst-case operating condition for the capacitor and 100% System Duty Cycle.	See below for detail
	Ripple Current	80%
	Minimum Life	7 years
Plastic Film Capacitor (Fixed Film (Paper/Plastic) Capacitor)	Voltage (% of Max rated) Ambient Temperature	90% Tmax - 10°C
X-Y Capacitor (Fixed X and Y Capacitor (Ceramic or Film, including Safety Agency certified))	Voltage (% of Max rated) Ambient Temperature	90% Tmax - 10°C
Tantalum Polymer Capacitor (Fixed Tantalum Polymer Type (includes POS-CAP, KOCAP, Neocap, SP caps))	Applied DC Voltage (Working Voltage) Applied AC Ripple + DC Voltage (Operating Voltage) 	80% 95%
	Ambient Rated Temperature	≥105°C
	Measured Case (surface) Temp rise above Measured Ambient Operating temperature	10°C
	Surge Current	10 Amp peak
	Reverse Voltage	5% or 0.5V (Whichever is smaller)
	Minimum life calculated using worst-case operating condition and 100% System Duty Cycle.	See below for detail
	Ripple Current	80%
	Minimum Life	7 years

Component Type	Parameter	Derating Criteria
EDLC Capacitor (EDLC radial lead (includes Supercaps))	Applied DC Voltage	80%
	Case Temp below Max Case Operating Limit	20°C
	Charge / Discharge Current	90%
	Minimum life calculated using worst-case operating condition and 100% System Duty Cycle. Regarding the selection of the life formula used, failure is defined as when an EDLC's capacitance changes ±30% from its initial value. Life Formula used shall apply this definition. (Example: If EDLC's initial capacitance equals 10F, then failure is when the measured capacitance is less than 7F or greater than 13F.)	See below for detail
	Minimum Life	7 years
Resistors		
Fixed Film Resistor (Fixed Film (Chip Discrete and SMD))	Power Dissipation	70%
	Ambient Temperature	Tmax - 24°C
Zero Ohm Resistor (Zero Ohm Resistor)	Current	84%
Composition (Composition)	Power Dissipation	70%
	Ambient Temperature	Tmax - 18°C
Variable Resistor (Variable)	Power Dissipation	70%
	Ambient Temperature	
	Non-wirewound	Tmax - 31°C
	Wirewound	Tmax - 19°C
Thermistor Resistor (Thermistor)	Power Dissipation	50%
	Ambient Temperature	Tmax - 50°C
Wirewound Power Resistor (Wirewound Power)	Power Dissipation	70%
	Voltage	70%
	Ambient Temperature	Tmax - 10°C
Miscellaneous		
Metal Oxide VAR Resistor (Metal Oxide Varistors (MOV))	Power Dissipation	60%
	Max Steady State Operating Voltage/or Clamping Voltage	35%
	Max Current	90%
Module (Module) (includes Flash Memory devices)	Ambient Temperature	100%
Non-certified Circuit Breakers (Circuit Breakers)	Current	90%
Certified Circuit Breakers (Circuit Breakers with Safety Agency Rating)	Current	100%
Non-certified Fuses (Fuses)	Current	90%
	Current (time delay fuse)	85%
Certified Fuses (Fuses with Safety Agency Rating)	Current	100%
PTC (Polymeric Positive Temperature Coefficient (PTC) Overcurrent Protector)	Derating is to follow the PTC manufacturer's derating recommendations. Key parameters to consider in derating are current (Ihold, Imax) and component ambient temperature.	Manufacturer recommendation
Signal Connectors (Connectors, Signal)	Ambient Temperature	Tmax - 25°C
	Note: Wire size used in application shall comply with connector specification and rated current.	
	Voltage (% of Dielectric Withstand Voltage)	80%
	Current	85%

Component Type	Parameter	Derating Criteria
Power Connectors (Connectors, Power)	Ambient-Temperature Note: Wire size used in application shall comply with connector specification and rated current. Voltage (% of Dielectric Withstand Voltage) Current (per pin, single or parallel pin configuration) Current (per pin, parallel pin configuration with one broken pin)	Tmax - 25°C 80% 85% 100%
Dual Connector (Connectors, Combined (Signal and power pins in same connector housing))	Signal pins and power pins shall be derated separately using the worst-case-power pin and worst-case signal pin stresses. Signal pins, use same criteria as Connectors, Signal Power pins, use same criteria as Connectors, Power	 See above See above
Certified Connectors (Connectors, Power or Combined with Safety Agency Rated)	Only power or combined connectors may have a safety agency rating. Rating shall include current, voltage, and temperature.	100%
Application Specific Connectors (Connectors, Application Specific)	Derating not required for connectors developed and qualified for a specific application and are being used in that application (for example, processor sockets and DIMM sockets)	N/A
2-30 Conductors Bundled Wire Conductor (Bundled Wire Conductor) (Rack level cabling only)	2-5 Conductors, Current 6-15 Conductors, Current 16-30 Conductors, Current	70% 60% 50%
Relay (Relays)	Resistive Load Current Capacitive Load Current Inductive Load Current Ambient Temperature Motor Load Current Filament (Lamp) Contact Power	90% 90% 75% Tmax - 20°C 30% 20% 70%

General Purpose Switch / Power Switch (Switches (General Purpose and Power))	Contact Current
	    Resistive Load
	    Capacitive Load
	    Motor Load
	    Filament (Lamp) Load
	Contact Current
	    Inductive Load
	    Contact Power
	    Contact Surge Current
		
		90%
		90%
		30%
		20%
		
		75%
		70%
		80%

Certified Power Switch (Switches (Power) with Safety Agency Rating)	Contact Current Ambient Temperature	100% 100%
ESD Device (ESD & Surge Suppression components)	For all parameters use per manufacturer's specifications *Note: These are components that are used to protect system or circuit elements from transient stresses beyond those encountered during normal operation*	-
Crystals / Oscillators (Crystals and Oscillators)	Shall meet all parameters use per manufacturer's specifications considering all modes of operation including fan fault condition	-
Diodes		
Diode General Purpose General Purpose (Signal, Switching, or Power Rectifier)	Reverse Voltage Maximum Tj Forward Current	80% 0.75(Tjmax - 25°C) + 20°C <100%
Diode SiC Silicon Carbide (SiC) Power Rectifier Note: Do not avalanche SiC diodes	Reverse Voltage Maximum Tj Forward Current	80% 0.75(Tjmax - 25°C) + 20°C <100%
Diode Regulator / Zener Voltage Regulator / Reference (including Zener)	Maximum Tj Maximum Power Dissipation	0.75(Tjmax - 25°C) + 20°C 100%

Component Type	Parameter	Derating Criteria
Diode Thyristor / SCR Thyristor, SCR, and Triac	On-State Current (It) Off-State Voltage (Vr) Maximum Tj	90% 70% 0.75(Tjmax - 25°C) + 20° C
Microcircuits		
IC DrMOS (Driver MOS (DrMOS), Power Stage, Smart Power Stage)	The parameters stated in the component specification's "Absolute Maximum Ratings" table shall be used in conjunction with the derating criteria presented herein to determine maximum allowable stress levels. For the specific functions/pins (Vboot – Vsw, VCC, VCCP) DC voltage only (Working Voltage) AC + DC (Operating Voltage) For all other non-logic pins not listed above (NOTE: Logic pins require no derating) AC + DC voltage (Operating Voltage) When only $V_{(DC)}$ is specified (with no visible sign of Avalanche) Maximum duration of AC voltage excursion above derated Vdc (when only V(DC) is specified.) Maximum Junction Temperature (Tj) With worst-case steady state application loading When stressing with approved thermal virus DC voltage only (Working Voltage)	 90% 95% 95% 95% 25ns 0.75(Tjmax – 25°C) + 20°C Tjmax – 30°C 95%
IC POL (Point of Load Voltage Regulator, Voltage Controller IC, Multi Chip Module (MCM), Monolithic devices)	Derating criteria is the same as for DrMOS	N/A
IC Digital / Linear / Linear-Fixed Voltage Silicon Digital & Linear IC's (MOS & Bipolar)	Maximum Junction Temperature (Tj) Max rated Tj > 125°C Max Rated Tj ≤ 125°C	 The greater of 115°C and 0.75(Tjmax - 25°C) + 20°C Tj (rated) – 10°C

Component Type	Parameter	Derating Criteria
Transistors		
Transistor Silicon FET (Silicon FET)	Maximum Junction Temperature (Tj) Avalanche Energy ESD Rating, Human Body Model (HBM)	$0.75(Tjmax - 25°C) + 20°C$ 50% TBD
	Gate – Source Voltage (Vgs)	
	DC voltage only (Working Voltage)	85%
	AC + DC voltage (Operating Voltage)	95%
	Drain – Source Breakdown Voltage (Vds)	
	DC voltage only (Working Voltage)	80%
	AC + DC voltage (Operating Voltage)	95%

Component Type	Parameter	Derating Criteria
Dual Silicon FET (Dual MOSFET)	The same derating criteria applies to Dual FET as for a single FET. The derating on both FETs shall require stress data entry for each one individually.	See Silicon FET derating criteria
Transistor Silicon Bipolar (Silicon Bipolar)	Collector-Emitter Breakdown Voltage (Vce) Maximum Junction Temperature (Tj)	80% 0.75(Tjmax - 25°C) + 20°C

Transistor Gallium Nitride (GaN)	Maximum Junction Temperature (Tj)
	Avalanche Energy
	ESD Rating, Human Body Model (HBM)
	
	Gate – Source Voltage (Vgs)
	  DC voltage only (Working Voltage)
	  AC + DC voltage (Operating Voltage)
	Drain – Source Breakdown Voltage (Vds)
	  DC voltage only (Working Voltage)
	  AC + DC voltage (Operating Voltage)
		0.75(Tjmax – 25°C) + 20°C
		50%
		TBD
		
		85%
		95%
		
		80%
		95%

Transistor Silicon Carbide (SiC)	Maximum Junction Temperature (Tj)
	Avalanche Energy
	ESD Rating, Human Body Model (HBM)
	
	Gate – Source Voltage (Vgs)
	  DC voltage only (Working Voltage)
	  AC + DC voltage (Operating Voltage)
	Drain – Source Breakdown Voltage (Vds)
	  DC voltage only (Working Voltage)
	  AC + DC voltage (Operating Voltage)
		0.75(Tjmax – 25°C) + 20°C
		50%
		TBD
		
		85%
		95%
		
		80%
		95%

Magnetics		

Transformer (Transformers – Pulse & Power)	Current Surge (% of max rated)
	Voltage Surge (% of max rated)
	Current (Continuous)
	Hot Spot temperature: (measured on hotspot of core surface)
	For transformers with UL60950 class rating
	  Class 105 (A)
	  Class 120 (E)
	  Class 130 (B)
	  Class 155 (F)
	  Class 180 (H)
	For transformers not covered by UL 60950
	  Temp below Max Rated Hot Spot
		<100%
		<100%
		90%
		
		90°C
		105°C
		110°C
		130°C
		155°C
		
		25°C

Component Type	Parameter	Derating Criteria
Inductor Iron Powder (Inductor – Iron Powder Core with Organic binders)	Max peak current (including ripple, transient, and unbalance, where applicable) as % of rated Isat at 100°C defined with -20% inductance roll-off (Excluded are inductors when used in high frequency / noise decoupling applications)	100%
	Max operating Temperature (measured on hotspot of core surface)	Tmax – 35°C
Inductor Ferrite (Inductor – Ferrite Core)	Max operating Temperature (measured on hotspot of core surface)	Tmax – 25°C
	Max peak current (including ripple, transient, OCP and unbalance, where applicable) as % of rated Isat at 100°C defined with -20% inductance roll-off (Excluded are Ferrite Core Inductors – Rod and Bead Type when used in high frequency / noise decoupling applications)	100%
Inductor Other (Inductor – Other [High-temp powder alloys, Cool-μ, Sendust, MPP, Metaglas, etc.])	Max operating Temperature (measured on hotspot of core surface)	Tmax – 25°C
	Max peak current (including ripple, transient, and unbalance, where applicable) as % of rated Isat at 100°C defined with -20% inductance roll-off (Excluded are inductors when used in high frequency / noise decoupling applications)	100%
Inductor Wound (Inductor, Wound)	Current Surge (% of max rated)	85%
	Voltage Surge (% of max rated)	<100%
	Current (Continuous)	<100%
	Temp below Max Hot Spot (measured on hotspot of core surface)	90%
	Max peak current (including ripple, transient, and unbalance, where applicable) as % of rated Isat at 100°C defined with -20% inductance roll-off (Excluded are inductors when used in high frequency / noise decoupling applications)	100%
Optoelectronics		
LED (Light Emitting Diode)	Average Forward Current	90%
	Ambient Temperature	<100%
Opto Coupler (Optocouplers)	Power Dissipation	80%
	Current	75%
	Voltage	75%
	Maximum Tj	0.75(Tjmax - 25°C) + 20°C

13.2 Life Requirement

The power supply shall support **5 years** calculated life under the following conditions:

- 200-240VAC input
- 55°C inlet temperature
- 100% of the time at 80% load
- 950m altitude

The power supply shall support **7 years** calculated life under the following conditions:

- 200-240VAC input
- 55°C inlet temperature
- 100% of the time at 50% load
- 950m altitude

13.3 Meantime Between Failures (MTBF)

MTBF prediction shall be completed in accordance with Telcordia SR-332, Method 1 Case 3, 40°C.

- Input Voltage: Nominal (HL 200VAC – 240VAC; LL 100VAC – 120VAC)
- 100% average power (Dynamic loading per profile defined in Design Specification)
- Airflow: as specified in the PSU product specification
- Temperature: Maximum operating temperature
- Quality Level II parts required
- Greater than 400K Hours unless otherwise specified in PSU product specification
- Correction factor may be applied with supporting evidence at Reliability Engineer's discretion.

13.4 Reliability Demonstration Test

A Reliability Demonstrated Test may be conducted as an audit to demonstrate an MTBF goal of 400k hours (or greater if specified by the PSU Product Specification) at 90% Confidence Level using Arrhenius and Chi-Square Statistical methods. Audit criteria shall be based on new design and/or high-volume products. Suppliers identified for RDT audit shall be communicated during RFQ.

- Input Voltage: Nominal (HL 200V_{AC} – 240V_{AC}; LL 100V_{AC} – 120V_{AC})
- Load: 80%
- Power Cycling: 45 minutes On, 15 minutes Off
- Temperature: UOL-5, may disable OTP if needed
- Sample Size: 42 (total samples collected from selected suppliers)
- Test duration: 2,160 hours
- Test shall be time terminated (Type I Censoring), One-Sided Lower Confidence Level
- Monitor output voltages and/or PWOK signal
- Record time to fail when failure occurs

Other LOBs may require RDT be demonstrated to their predetermined MTBF goal. Consult Reliability Engineer or Power System Engineering for guidance.

13.5 Fan Reliability Qualification

- Derating - Electronic Derating for Optimum Performance (RAC)
- Reliability prediction – Telcordia SR-332
- Worst Case Electrical Parts Tolerance Analysis (WCEPTA)
- Fan L10 Bearing Life: 43,200 hours at max system ambient
- Probability Ratio Sequential Test (PRST): 128, 70C, Max RPM, 1000 hours
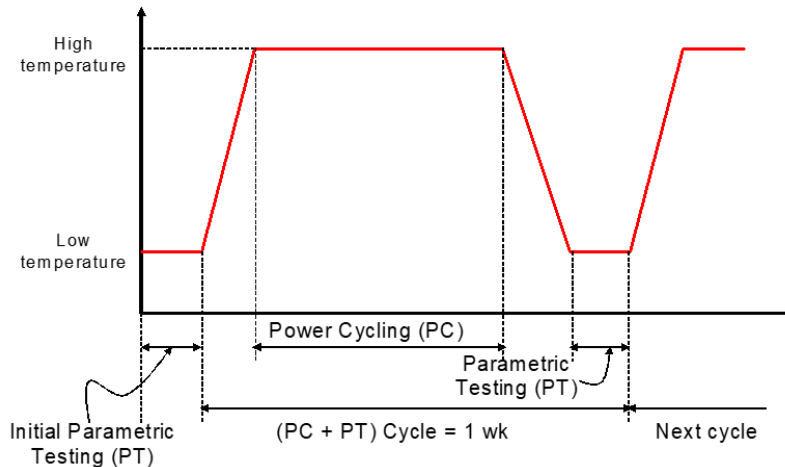
Figure 13-1 Fan accelerated life test (FALT) profile

- Combined Temperature Humidity Test (refer to TH profile below)
- Design Verification Test (DVT)

  Test shall use 12 random samples with the same bearing, lubricant, and lubricant seal as production level fans. DVT report shall include the following test sequence:
  - RPM, current and dBA measurement – T0
  - Hot /cold and humid storage test (Four corners)
  - RPM, current and dBA measurement – T1
  - Hot /cold operation test (Four corners)
  - RPM, current and dBA measurement – T2
  - Thermal shock test -40oC to 70oC, 50 cycles, 20 minutes dwell time.
  - RPM, current and dBA measurement – T3
  - RPM, current and dBA shall be within the specification at each stage
- Shock and Vibration

  The following tests shall be performed per Fan Shock and Vibration Test Procedure
  - A Non-Operational Vibration test shall be completed.
  - A Non-Operational Half Sine Shock test shall be completed.
  - A Non-Operational Square Wave Shock test shall be completed.

Table 13-2 TH profile

Test	Specification Test Parameter	Margin Test Parameter
Operational Random Vibration	• 0.5 G$_{RMS}$ using break points listed below in *Table 13-3* • All 6 sides tested • 30 minutes per side	N/A
Non-Operational Random Vibration	• 2.2 G$_{RMS}$ using break points listed below in *Table 13-4* • 15 minutes per side • All 6 sides tested	• 3.12 G$_{RMS}$ using break points listed below in *Table 13-5* • 15 minutes per side • All 6 sides tested
Operational Half Sine Shock	• 82 G ±5% with pulse duration of 2 msec ±10% (equivalent to 40 in/sec [102 cm/sec]) • All 6 sides tested	• Increase in **40G** increments until failure or **202G (2ms)**, whichever occurs first • All 6 sides tested

Non-Operational Half Sine Shock	• 142 G ±5% with pulse duration of 2 msec ±10% (equivalent to 70 in/sec [178 cm/sec]) • All 6 sides tested	• Increase in **60G** increments until failure or **322G (2ms)**, whichever occurs first • All 6 sides tested
Non-Operational Square Wave Shock	• 40 G Faired Square Wave w/Velocity Change @ 200 In/Sec [508 cm/sec] or greater • All 6 sides tested	• Increase in **20G** increments until failure or **80G (200in/sec),** whichever occurs first. • All 6 sides tested

Table 13-3 Operational random test 0.5G$_{RMS}$ profile

Frequency (Hz)	G^2/Hz
7	0.00015
20	0.014
140	0.014
312	.000065
400	.000035
600	.000035
800	.000023

Table 13-4 Non-operational random specification test 2.2 G$_{RMS}$ profile

Frequency (Hz)	G^2/Hz
5	0.01
20	0.01
500	0.01

Table 13-5 Non-operational random margin Test 3.12 G$_{RMS}$ profile

Frequency (Hz)	G^2/Hz
5	0.02
20	0.02
500	0.02

13.6 Solder Assembly Qualification

Shall be completed in accordance with Level 2 of Internal Solder-Assembly Reliability Qualification Requirements. The general lead-free qualification procedure is as described below:

1. Obtain component information (BOM, heat resistance, moisture sensitivity level).
2. Obtain printed circuit board assembly (PCBA), solder paste and process information (including measured reflow profile)
3. Ensure board assembly process, profile and factory conditions are compatible with PCB & component specifications.
4. Conduct board (PCBA) level test
   • Assemble boards at specified conditions
   • Perform C-SAM, X-ray on selected components
   • Perform thermal cycling
   • Perform post thermal cycling cross section analysis
5. Compile results and review with Reliability Engineer

PSU suppliers shall conduct a full lead-free qualification at least once per PCBA production site. An ECR need to be submitted for approval if any changes in the production site, solder paste, or re-flow profile.

13.7 Worst Case Electrical Parts Tolerance Analysis

The purpose of a Worst Case Electrical Parts Tolerance Analysis (WCEPTA) is to evaluate the performance of an electrical circuit under expected operating conditions considering component environmental variances, temperature effects, and degradation over product expected lifetime.

Typically for component sources of variation include:

- Initial tolerance
- Temperature Coefficient of Resistance
- Load Life Stability (Aging)
- Short Time Overload
- Effects of Soldering
- Temperature Cycling
- Moisture Resistance (Humidity Exposure)
- Low Temperature Operation
- High Temperature Operation
- Terminal Strength-Bend (Manufacturing Associated Stress)
- Thermal Shock
- Vibration

The WCEPTA applies to all Voltage Regulation (VR) and Over Current Protection (OCP) circuitry. However, if any circuit is considered critical it may be evaluated by Reliability Engineering, or at the request of any Product Development Engineering. The WCEPTA uses a Monte Carlo simulation approach to evaluate an electrical circuit.

13.7.1 Circuit Schematic Example

The circuit schematic shown below is for a 1.5V voltage regulation with a specification tolerance of +/-3%; therefore, the lower specification limit is 1.455V and the upper specification limit is 1.545V:
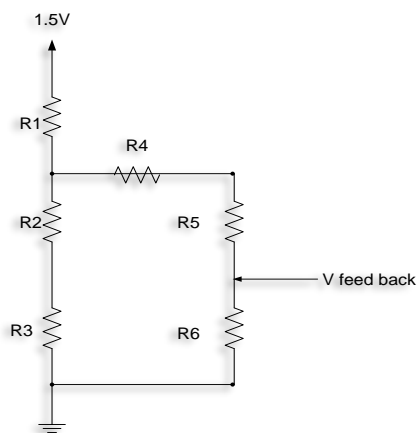
Figure 13-2 Voltage Regulation Circuit

The component assignments for the above circuit are as follows:

- R1: zero Ω jumper, +/-5% initial tolerance
- R2: 2210Ω, +/-1% initial tolerance
- R3: 2490Ω, +/-1% initial tolerance
- R4: 10Ω, +/-1% initial tolerance
- R5: 2210Ω, +/-1% initial tolerance
- R6: 2490Ω, +/-1% initial tolerance
- V feedback: Single Phase PWM Controller, 0.6V, +/-0.8%

13.7.2 Collect Component Datasheets

The analyst must review the current Bill-of-Materials (BOM) to determine which component vendors have been approved for use in the circuit identified for analysis. The WCEPTA will evaluate each of the approved component vendors for suitability of use given the voltage regulation specification limits of +/-3%. In addition, the analyst will confirm that the component nominal values and initial tolerances specified in the schematic are identical to the BOM values for each given reference designator. The component datasheets for the thick film 1/16W resistors are as follows:

13.7.3 Quantify Component Sources of Variation

A compilation of the appropriate component initial and environmental tolerances is required to develop component mean and standard deviation estimates. The product's specified operating range and worst-case component electrical stress analysis (electrical de-rating) are used to determine the temperature coefficient of resistance (TCR) effects. The de-rating analysis provides the worst-case temperature which in combination with the product's low temperature operating requirements produces a temperature spread or delta. Components identified in the circuit schematic that will be used to develop the circuit transfer function are grouped in a summary matrix. The matrix affords a means of collecting all environmental component variances to develop summary statistics (mean and standard deviation) for each circuit component. *Table 13-6* below illustrates the combined 3σ tolerances.

Table 13-6 Summary of 3σ component tolerances

Reference Designator	R1	R2	R3	R4	R5	R6	Vfb
Part Description	Zero Ohm Jumper	Thick Film Resistor	Thick Film Resistor	Thick Film Resistor	Thick Film Resistor	Thick Film Resistor	Phase PWM Controller
Applicable Parameter	Resistance	Resistance	Resistance	Resistance	Resistance	Resistance	Voltage
Nominal Parameter Value	0.05	2210	2490	10	2210	2490	0.8
Derating Report Component Tc, deg C	77	77	77	77	77	77	77
3 Sigma Sources of Variation							
Initial Tolerance	5.00%	1.00%	1.00%	1.00%	1.00%	1.00%	0.80%
Tolerance of B-value							
Tolerance with VKA variation							
Temp Coefficient (350ppm/C) or 0.035%/C	2.35%						
Temp Coefficient (200ppm/C) or 0.02%/C		1.34%	1.34%	1.34%	1.34%	1.34%	
Temp Coefficient (100ppm/C or 0.01%/C)							
Temp Coefficient (4041ppm/C or 0.4041%/C)							
Long Term Voltage Stability							
Load Life Stability	5.00%	3.00%	3.00%	3.00%	3.00%	3.00%	
Short time overload							
Effect of Soldering	1.00%	1.00%	1.00%	1.00%	1.00%	1.00%	
Temp Cycling	1.00%	1.00%	1.00%	1.00%	1.00%	1.00%	
Moisture Resistance	5.00%	3.00%	3.00%	3.00%	3.00%	3.00%	
Low Temp Operation							
High Temp Operation							
Terminal Strength-Bend	1.00%	1.00%	1.00%	1.00%	1.00%	1.00%	
Thermal Shock							
Vibration							
3σ Total Standard Deviation,	0.0914	0.0488	0.0488	0.0488	0.0488	0.0488	0.0080
1σ	0.0305	0.0163	0.0163	0.0163	0.0163	0.0163	0.0027
1σ in terms of parameter	0.00152	35.93514	40.48801	0.16260	35.93514	40.48801	0.0021

13.7.4 Circuit Transfer Function Determination

For a given circuit under WCEPTA evaluation a mathematical representation of the circuit's output   is required in order to conduct a Monte Carlo Analysis (MCA) and assess circuit compliance to specification limits. The formulation of the transfer function (1st order) is the responsibility of the Electrical Engineering Design Team or original equipment manufacturer (ODM), as applicable.   For the electrical schematic shown above, the transfer function derivation utilizing Kirchhoff's and Ohm's Law is as follows:

Monte Carlo Analysis (MCA)– Syntax:

MTB > Random 5000 'R1';
SUBC>   Normal 0.05 0.00152.
MTB > Random 5000 'R2';
SUBC>   Normal 2210 35.93514.
MTB > Random 5000 'R3';
SUBC>   Normal 2490 40.48801.
MTB > Random 5000 'R4';
SUBC>   Normal 10 0.16260.
MTB > Random 5000 'R5';
SUBC>   Normal 2210 35.93514.
MTB > Random 5000 'R6';
SUBC>   Normal 2490 40.48801.
MTB > Random 5000 'U79';
SUBC>   Normal 0.8 0.0021.

MTB > let c8=(c7/c6)*(c4+c5+c6)+((c7/c6)+(((c7/c6)*(c4+c5+c6))/(c2+c3)))*c1
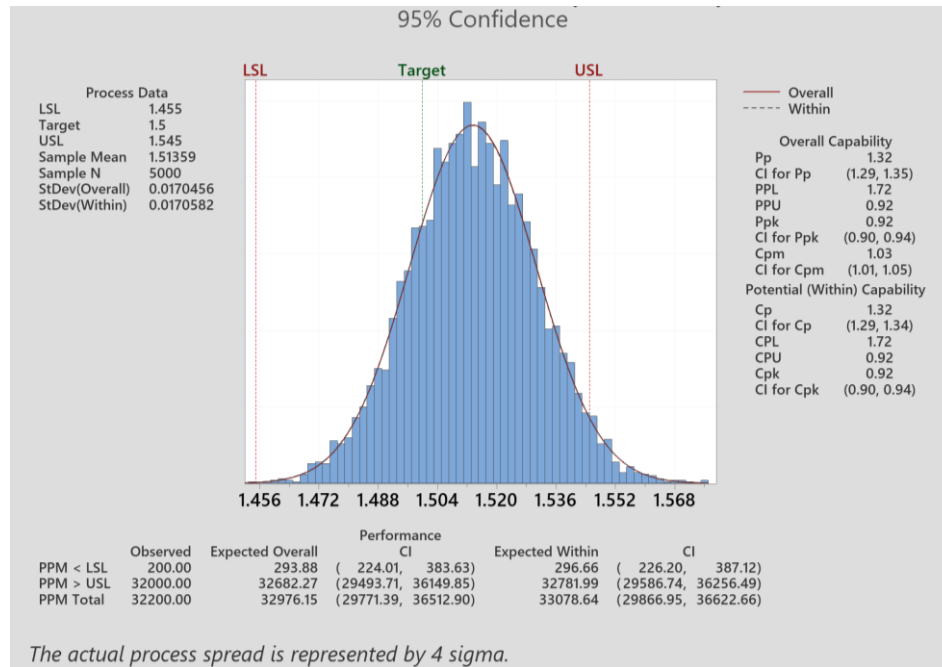
Figure 13-3 Monte Carlo analysis output example

13.7.5 Non-Conforming Circuit

The circuit shown above falls below the required Cpk, Ppk=1.33. Consequently, the overall circuit performance is noncompliant to circuit specification limits. From a visual perspective the circuit is off nominal target with an obvious shift to the right of nominal. The overall circuit performance, in this case, is falling below the lower specification limit and above the upper specification limit. The parts-per-million noncompliant to the lower specification limit is approximately 293 events and above the upper specification limit approximately 32,682 events.

he next step(s):

1. Conduct a sensitivity analysis on the circuit transfer function to affect a component value change (standard value) that would significantly affect the MCA circuit output.
2. Evaluate a +/-1% resistor with tighter environmental tolerances in the circuit, for example, migrating to a 0.5% tolerance passive device.
3. Given the above step(s) do not produce a fully capable circuit, evaluate the use of a tighter initial tolerance resistor with reduced environmental tolerances.
4. In some cases, the active device in the circuit, for example, a precision voltage reference would require a tighter tolerance.
5. All proposed circuit component value, tolerances, etc. changes must be approved by the product electrical engineering (EE) design team prior to implementation.
6. Since the WCEPTA is conducted during the engineering development phase of a product's life cycle some of the active devices suggested for use may have preliminary data sheets. All WCEPTA's must be revised prior to pilot launches with final datasheets.

13.8 Stress Life Test (STRIFE)

Output Overload Test I – OTP enable
1. Sample size = 5 (the test units shall have passed all functional tests)
2. Do not disable any protections. Critical components, all thermal sensors and hot spot areas within the PSU shall be thermo-coupled. (Shall verify IR image)
3. Run the supply at the maximum operating ambient temperature, low AC input voltage, and 100% load for two hours. Evaluate for any functional failures.
4. Repeat the test with a 5% of full load increments until the system shuts down due to OTP or OCP. At each load point, prior to the PSU shutting down, the junction temperature and electrical parameters of each thermo-coupled component shall be verified to ensure all components are within specification. Design team shall provide confirmation of which protection triggered. (OCP and OTP WCEPTAs shall be reviewed and approved prior to start of strife test)

Output Overload Test II – OTP disable
1. Sample size = 5 (the test units shall have passed all functional tests, recommend using the units that went through Output overload test I)
2. Disable all temperature and over current protection circuits
3. Set output load to the point at which the PSU protected itself in line item 4 above. A reduction of load by 10% shall be the starting load for this test.
4. Repeat the test at a 5% incremental rate.
5. When failure occurs, a complete FA shall be performed and provided to the respective reliability and power engineer for review and approval.

Pass / Fail Criteria:
1. All 5 PSU(s) shall be able to operate up to the max OCP 3 sigma limit as calculated from the WCEPTA.
2. Test units that do not meet the max OCP 3 sigma limits shall demonstrate that the failure occurs above the max OTP 3 sigma limits as calculated from the WCEPTA.
3. Vendors shall ensure that prior to OTP or OCP protecting the PSU, all components are below their max rated junction temperature Tj.

Failure Reporting:
Any failures observed for the tests described in this section shall have the following information provided:
1. During what test did the failure occur?
2. What time during the test did the failure occur?
3. What was the failure symptom?
4. What was the failure mode (failure mechanism)?
5. What change(s) could be made to correct the problem? Change(s) to increase design margin shall be evaluated by Power Engineer.

13.9 Reliability Validation

Baseline test a 24-hour bench test at ambient to verify UUT stability shall be performed prior to Reliability Validation testing.

13.10 Temperature Humidity

A Temperature Humidity Test shall be completed in accordance with Internal Procedure.

- Temperature Humidity Test – Includes, operating, non-operating, low and high humidity elements. Operating temperatures (typically 5°C to 45°C) based on product ASHRAE or custom classification. Non-operating temperatures from 65°C @ 8% and 90%RH to -40°C
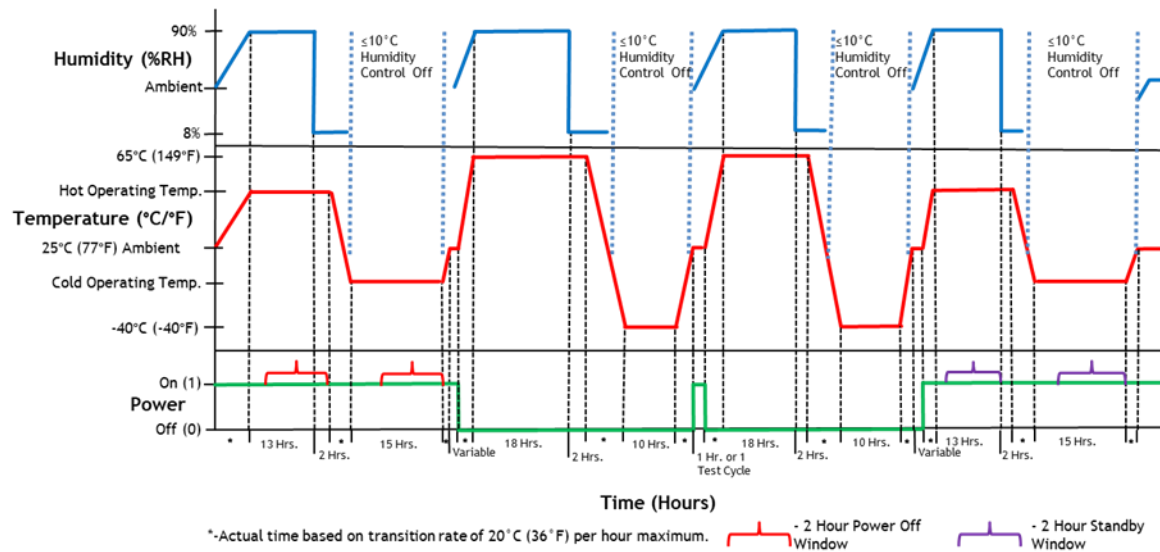
Figure 13-4 Temperature humidity profile

13.11 Mechanical Life

A Mechanical Life Test shall be completed in accordance with Internal Procedure.

- Mechanical Life Test – All mechanical elements or field replaceable unit (FRU) customer has access to. Cycles based on assembly, deployment, and typical customer utilization models. Supplemental to element, component, or subsystem qualification testing.
- Based on features that are customer can interface. For PSU the most common features are:
  - PSU – 60 Cycles – 4 samples
  - Power Connector – 55 Cycles – 2 samples

13.12 Power Cycling

Power Cycling test shall be completed:

- Input Voltage: Nominal (HL 200VAC – 240VAC; LL 100VAC – 120VAC)
- Load: 100%
- Temperature: A4 Category per Climatic & Airborne Contaminant Specification
- Sample Size: 3
- Test profile: 45 minutes On, 15 minutes OFF
- Test duration: 42 cycles each at high and low temperature
- All samples shall pass functional test before and after power cycling

13.13 Shock and Vibration

The following tests shall be performed per Power Supply Shock and Vibration Test Procedure

Test	Specification Test Parameter	Margin Test Parameter
Operational Random Vibration	• 0.5 G$_{RMS}$ using break points listed below in *Table 13-7* • All Sides except AC connector down • 30 minutes per side	N/A
Non-Operational Random Vibration	• 2.2 G$_{RMS}$ using break points listed below in *Table 13-8* • 15 minutes per side • All 6 sides tested	• 3.12 G$_{RMS}$ using break points listed below in *Table 13-9* • 15 minutes per side • All 6 sides tested
Operational Half Sine Shock	• 82 G +/- 5% with pulse duration of 2 msec +/- 10% (equivalent to 40 in/sec [102 cm/sec]) • All sides except AC connector down	• 122 G +/- 5% with pulse duration of 2 msec +/- 10% (equivalent to 60 in/sec [152 cm/sec]) • All sides except AC connector down
Non-Operational Half Sine Shock	• 142 G +/- 5% with pulse duration of 2 msec +/- 10% (equivalent to 70 in/sec [178 cm/sec]) • All 6 sides tested	• 202 G +/- 5% with pulse duration of 2 msec +/- 10% (equivalent to 100 in/sec [252 cm/sec]) • All 6 sides tested
Non-Operational Square Wave Shock	• 40 G Faired Square Wave w/Velocity Change @ 200 In/Sec [508 cm/sec] or greater • All 6 sides tested	• 60 G Faired Square Wave w/Velocity Change @ 200 In/Sec [508 cm/sec] or greater • All 6 sides tested

Table 13-7 Operational random test 0.5 G$_{RM}$S profile

Frequency (Hz)	G^2/Hz
7	0.00015
20	0.014
140	0.014
312	.000065
400	.000035
600	.000035
800	.000023

Table 13-8 Non-operational random specification test 2.2 G$_{RMS}$ profile

Frequency (Hz)	G^2/Hz
5	0.01
20	0.01
500	0.01

Table 13-9 Non-operational random margin test 3.12 GRMS profile

Frequency (Hz)	G^2/Hz
5	0.02
20	0.02
500	0.02

14 Regulatory & Ecology Requirements

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, etc.), other than an ITE application, may require further evaluation.

14.1 Scope

This section covers the design requirements for integral (internal) enclosed power supplies, including hot-swappable supplies for use in servers, networking and storage products with ac or dc or mix mode ac/dc input. This document specifies standard industry requirements for use during the development and/or qualification of internal power supplies.

14.2 EMC Requirements and Standards

The PSU shall be designed, tested, and certified to comply with the latest version of CISPR 32 Emissions standards for Class A or Class B as applicable, CISPR 24 and CISPR 35 Immunity standards, IEC 61000-3-2 or IEC 61000-3-11 Current Harmonics standards, IEC 61000-3-3 or IEC 61000-3-12 Voltage Fluctuations/Flicker standards and applicable national differences.

Test setup and methodology shall address ANSI C63.4 and CISPR standards and note the worst-case where applicable in test reports. It is recommended the certification include applicable country requirements for each country where placed on the market including US CFR Title 47, FCC Part 2 and 15, and Canada ICES-003, and to the standards under the European Union Directive 2014/30/EU.

14.3 Safety Requirements and Standards

The PSU shall be designed, tested, and certified to comply with the latest version of IEC 60950-1 and IEC/EN/UL/CSA 62368-1 and applicable national differences.
It is recommended that the PSU shall be certified to the latest national standard based on IEC 62368-1 by the same agency issuing the CB Certificate or at least one EU Notified Body with a factory surveillance program

The following shall be addressed:
a) The declared maximum ambient temperature for safety certification shall not be less than 45 degrees C, including stand-by mode.
b) If the power supply can be removed from the end product without disconnecting the power cord, investigation that no energy hazard (below 240 VA) exists at the PSU outputs in the removed condition shall be considered.
c) The power contact receptacle portion of output connectors of removable power supplies must be investigated for the interruption of current in accordance with the Overload, Temperature and Resistance to Arcing Test sequence in UL 1977, the Standard for Component Connectors for Use in Data, Signal, Control and Power Applications in accordance with the output ratings of the power supply.
d) Proper engineering consideration should be made for operation at the altitude as defined for the product

Creepages and Clearances: UL 62368-1 Clause 5.4.2.5 should be used to show creepage and clearance compliance to altitudes higher than 2000 m.

Clearances: Clearances must meet the requirements for an altitude of 5000 m for use in many countries.

e) For power supplies with a voltage selector switch, abnormal testing of the voltage selector switch should be conducted.

For a power supply rated with dual voltages and with auto range circuitry, a statement in the abnormal test section of applicable regulatory reports that the auto range circuit does not constitute a hazard should be included.

f) For power supplies for use in multi power supply systems, the touch current from ac mains to safety ground should not exceed 3.5 mA divided by the number of power supplies used in the system measured at 254 Vac 60Hz

g) Humidity conditioning for tropical climates must be conducted at a temperature of 40°C ± 2°C, and humidity of 93% +2% /-3%. The humidity conditioning duration is 5 days (120 hours) and the rated ambient temperature of such equipment must be 35° C or higher.

h) The type test for ground continuity must be done at 40 A minimum for all products having protection up to 20 A with less than 0.1 ohm from the safety ground (third wire) input pin to the power supply chassis for 2 minutes. The voltage drop shall be less than 2.5 V.

For protection exceeding 20 A, this test shall be conducted at double the branch circuit for it will be utilized.

i) Output returns must be grounded within the power supply chassis. Outputs cannot be floating and must be referenced to ground.

For dc-dc PSU, the power supply chassis shall also be provided with a grounding terminal, e.g., a metal stud secured to the chassis that is to be connected to dc mains supply earth connection. A dc return pin or additional grounding pin integrated in the dc input connector is not acceptable to NEBS.

j) There shall not be any Condition of Acceptability (CoA) and/or Engineering Consideration(s) requiring design requirements or testing on the end product.

14.4 Fire and Electrical Enclosure

A power supply must provide fire and electrical enclosures. Surface of the enclosure exposed to the user (non-service persons) when installed in the end system must comply with the opening requirements with respect to its orientation (top, side, bottom) as defined in the safety standards of IEC 60950-1, IEC 62368-1, EN 62368-1, and UL/CSA 62368-1.:

1) Minimize the possibility of entry of a foreign object into the power supply and contacting hazardous voltages
2) Minimize the possibility of emission of burning material from the power supply
3) **30 N and 250 N tests**: Tests in accordance with IEC 60950-1 standard, and IEC 62368-1, EN 62368-1, and UL/CSA 62368-1 standards shall be conducted and reported in the product safety certification and CB test reports.
4) **Impact test** should be conducted per the IEC 60950-1 standard and IEC 62368-1, EN 62368-1, and UL/CSA 62368-1 standards
5) **Accessibility:** All covers that will serve as enclosures in the end product shall comply with accessibility requirements addressed in IEC 60950-1 standard and IEC 62368-1, EN 62368-1, and UL/CSA 62368-1 standards and comply with various mechanical tests as applicable.

14.5 Telecommunications DC Mains Powered Power Supplies

Power supplies to be used in telecommunication applications shall comply with the requirements of IEC 60950-1 standard and IEC 62368-1, EN 62368-1, and UL/CSA 62368-1 standards. An input power of -48 Vdc for USA and Canada and -60 Vdc for EU member countries is used for equipment used in the central office in the telecommunications applications. Under float conditions these voltages may go up to -56.5 Vdc and -75 Vdc respectively.

In addition, the following shall be considered:
1) UL 891: Switchboards
2) CSA C22.2 no. 31: Switchgear Assemblies
3) IEC TR 62102: Electrical safety – Classification of interfaces for equipment to be connected to information and communications technology networks
4) Telcordia GR-1089

   Notes:
   1. Some customers, such as telecommunication utilities or other customers, may equire compliance to NEBS standards specifications. Such requirements should be considered for the specific use for the particular power supply and end product. NEBS requires that the equipment must be UL certified before the utilities consider it for NEBS evaluation.

14.6 Components

Any or all of the components listed in this specification may be used in the power supply. Components deemed critical other than those listed in this specification may be used if they meet and are certified per the requirements of the country of use. Components must meet the safety, EMC/EMI, energy efficiency standards, mandatory environmental requirements and be certified as applicable for the country of use. All components must meet the requirements of restricted materials as applicable in the countries of use.

14.7 Flammability requirements

Minimum flammability ratings for the following components per the test methods in the Annexes of UL/CSA 60950-1 and UL/CSA 62368-1 standard.
   a) Printed circuit boards, including all daughter cards: V-1 or better.
   b) Power connectors on the Motherboards to be V-0 for hot swappable power supplies
   c) All other PSU connectors to be V-1 or better

Flammability of other components should be considered for the location and use of the component.

14.7.1 Capacitors

14.7.1.1 Tantalum Capacitors

Tantalum capacitors are not allowed in the Power Supply.

14.7.1.2 X Type Capacitors and Y Type Capacitors

Line to line or line to neutral X Type capacitors, or line to ground or primary to secondary Y Type capacitors must be certificated to IEC 60384-14 or equivalent national standard and bear the Mark of the certifying agency.

14.7.1.3 X Type Capacitors

The voltage rating of X-capacitors must not be less than the rated voltage of the intended end use equipment. The peak impulse test voltage of X-capacitors must not be less than the applicable required withstand voltage. The peak test voltage of an X1 capacitor is 4 kV peak and that of an X2 capacitor is 2.5 kV peak.

The endurance test must not be less than 21 days and the temperature during the endurance conditioning shall be 40 ± 2 Degrees C. The relative humidity during the endurance conditioning shall be 93% ± 3% RH.

14.7.1.4 Connectors

Designer must carefully select the connector that has adequate voltage, current and temperature ratings for the intended purpose. The location of the connector within the product will determine the required safety certification requirements. Safety Certification and certifying agency Marks shall be considered depending on the final end product market. If size of the connector allows, the manufacturer should provide required Safety Approval Marks and ratings on each part.

Table 14-1 Minimum Flame Rating of Plastics used in connectors.

Connector Characteristics	Flame Rating of Plastic
Connectors carrying Mains Voltage	V-2
High Voltage/Power Connectors	V-2
Low Voltage/Power/Data Connectors	V-2
Hot swap power connectors	V-0
I/O Connectors	V-1

14.7.1.5 Fuses

The designer must use extreme care when selecting the type and V/A-rated fuse to ensure that fuse opens under abnormal conditions. At a minimum, the fuse must be certified to UL and CSA standards as applicable. The following guidelines shall be followed:

- **DO NOT** substitute IEC 60127 (Miniature Fuses)-type fuses for UL 198G (Fuses for Supplementary Overcurrent Protection)-type fuses, or vice versa. They are radically different in blow characteristics.
- For fuses certified to IEC 60127, it is recommended to use high breaking capacity fuses (HBC).
- If fuses are located on a printed wiring board, then the fuse rating must be provided on the PWB via label, silk-screen, stamp or etching. Rating must include voltage, current, and type if the type is special (slow blow, fast blow, etc.).
- Fuse type and rating selection must ensure that the fuse **DOES NOT** blow under normal operating conditions but **DOES** blow under abnormal conditions. It is recommended that failure/abnormal conditions be simulated to ensure that the fault current and power source cause the fuse to open. The fuse must not shatter when it opens.

Primary Circuit Fuse: For Pluggable Type A PSUs, the primary circuit fuse of greater than 16-amp rating generally are not permitted.

14.7.1.6 Inductors and Filters

These types of devices are typically located in the power supply in the AC input stage and are designed to filter noise before it can get out of the product. Normally one side is "line" and the other is "neutral." Ensure the wire size is adequate for carrying the current in normal and abnormal conditions without burning open.

Plastic materials used to provide isolation between the two windings must be able to withstand extreme temperatures without softening or deforming. All headers/bobbins must be molded from UL-recognized plastic with a flame rating of V-1 or better.

Toroid-type inductors must be securely mounted such that the core cannot break loose from base/header during use or shipment. Toroid-type cores must be insulated.

14.7.1.7 Metal Oxide Varistor

All Metal Oxide Varistors (MOVs) used from Line-to-Line must be UL recognized; and comply with IEC 61051-1 and IEC 61051-2 standards. MOV's must be properly placed or shielded to prevent a compromise of safety insulation in the event of a failure. A MOV must be selected with a high enough voltage trip point that it cannot operate with the normal variation of input voltage.

MOVs and gas discharge tubes cannot be used in any application where either lead is connected to ground.

If the MOV is subjected to long-term over-voltage conditions, the MOV either reaches an excessive temperature or explodes. Place a fuse between the MOV and the power inlet of the equipment to reduce the risk of fire or explosion (heat shrink tubing is required on MOVs in primary circuits).

If used in the primary circuit from line to ground, then a protective device (such as a fuse) must be provided to protect the MOV, and the equipment must be pluggable type B or permanently connected equipment. If used in a Pluggable type A equipment, then a separate earthing terminal must be provided on the outside of the equipment and this terminal must be connected to building earth by a separate protective earthing conductor.

An MOV shall not be used to bridge double or reinforced insulation.

14.7.1.8 Plastics Including Foam

Covers plastic and foam parts not used within a critical component otherwise specified within this specification.

Plastic parts inside a fire enclosure are required to be a minimum of V-2 unless it is located above bottom openings. Plastic parts located above bottom openings must be a minimum of V-1.
Foam parts inside a fire enclosure are required to be a minimum of HF-2 unless it is located above bottom openings. Foam parts located above bottom openings must be a minimum of HF-1.

Plastic and foam parts should be UL Recognized unless they are decorative only. It is recommended that material identification be molded into all parts that are large enough to bear the markings. An optional method of providing traceability is to print the information on each box or provide a certificate of

compliance in each box of parts. Traceability markings include: (a) manufacturer of plastic; (b) UL designation for the plastic; (c) part number and date of manufacture.

It is recommended that a "Certificate of Compliance" be required with each lot for the traceability of plastics.

Plastic parts over 25 grams or 200 mm2 planar area must be labeled according to ISO 11469:2016 which includes ISO 1043-1, 2, 3, & 4.

Externally Accessible Parts used in GS certified products may also be subject to Polycyclic Aromatic Hydrocarbon requirements per GS specification AfPS GS 2019:01 PAK "Examination and assessment of polycyclic aromatic hydrocarbons (PAHs) for awarding the GS Mark"" and "Supplementation of the PAH Decision 01-08".

Do not contain a metal insert or fastener that is 1) molded-in 2) heat or ultrasonically inserted, or 3) glued-in unless the metal component is either separable from plastic parts (Fan impellers are excluded)

Do not contain adhesive, coating, paint or finish that impedes recycling (unless plastic part contains at least 25% PCR). (Excluding Printed circuit board, wires, cables, connectors, electronic component, optical component, acoustic component, ESD component and EMI component. If plastic is painted or coated supplier shall provide IZOD testing reports.

14.7.1.9 Printed Wiring Boards

All printed wiring boards (PWBs) must be UL-recognized and contain a minimum V-1 or better flame rating and a minimum 105⬚C temperature rating. Depending on application, the temperature rating and CTI rating may need to be rated higher.

Each PWB should be marked according to UL approval: manufacturing identification and type designation. During the design of a PWB, consider the voltage between adjacent etch runs ensuring adequate electrical isolation. If etches are too close, arcing, tracking and carbonization of the PWB material might occur.

If the PWB is provided with a fuse location(s), the location must be provided with the reference designator and voltage/current rating of the fuse. If any supply voltage (AC or DC) is provided at external port, limit the current to less than 8 amps. If the current is more than 8 amps, then provide a current limiting device, such as a 5-amp fuse or equivalent PTC. Current limiting device must be UL and CSA approved. All input/output ports must comply with the requirements of limited power sources. PWB assembly suppliers use UL-recognized PWBs.

DO NOT use PWBs manufactured using chemicals called out in the Montreal protocol.

Printed wiring boards should support the requirements of EPEAT as a recommended design practice.

Printed Circuit Board Laminates should not contain greater than 1000 ppm chlorine or greater than 1000 ppm bromine at the homogenous level.

14.7.1.10 Switches

14.7.1.10.1.1   Main Disconnect

Power switches require safety approvals as applicable in the country of use. The most common Marks are UL, CSA, and a European Mark such as VDE, TUV, FIMKO, DEMKO, SEMKO, NEMKO or SEV, but depending on the country where sold, the product may require more.

The power switch must bear the required agency approval marks. Mark the power switch with voltage and current rating. The rating for USA/Canada might be different for Europe; therefore, there can be one set of markings associated with European approvals and another set of markings associated with UL/CSA approvals.European approvals require that the power switch bear a marking indicating the maximum operating ambient temperature. This marking is the temperature in degrees Celsius (C) followed by the letter "T", (i.e., 85T).

Power switches must have the ON and OFF positions indicated by ISO symbols. According to Standard IEC 60417 –5007, "I" indicates the ON position and in Standard IEC 60417-5008, "O" indicates the OFF position. These markings may be stamped, silk-screened, or affixed with a permanent adhesive label.
AC mains disconnect power switches must have a minimum 3 mm gap between contacts when the switch is in the open position.

14.7.1.10.1.2   Standby

A standby power switch is a switch that deactivates part of a system but does not completely remove power from some part of the circuitry. A standby power switch is not considered the mains disconnect switch and the marking required indicating the position is different. Certification requirements for a standby switch located in the primary circuit are similar to the mains disconnect switch except that the 3 mm contact gap is not required. Marking of a standby power switch is found in Standard IEC 60417-5009, "Graphic Symbols for Use on Equipment".

14.7.1.11 Transformers

The three most common configurations are linear (metal laminations), switcher (ferrite Double E Core), and switcher (toroidal ferrite core). Each of these performs step voltage functions and provides electrical isolation between primary circuits and secondary circuits. The transformer may have UL, CSA and VDE certification depending on the requirements of the power supply certification.

Ensure that the materials do not adversely interact chemically, causing a failure of the insulation. UL has evaluated many combinations of insulating systems for use in transformers.   The dielectric of this insulation system is dependent on a maximum temperature rating. If the operating temperature is above class A limits, then the insulation system must be UL recognized. Use a designated mark to identify the UL insulation system.

The manufacturers are required to perform production line (routine testing) dielectric strength tests. Test voltage settings depend on the electrical ratings of the transformer, and whether its construction includes a grounded metal barrier between primary and secondary circuits. Refer to UL Standards or IEC Standards for appropriate test voltages.

Consider electrical isolation concepts when designing a transformer: Creepage distance, clearances, and the distance through insulation and types of insulation (i.e., functional, basic, supplementary, reinforced, and double).

14.7.1.12 Wire and Cable

Use green-with-yellow-stripe of a suitable wire size wires to provide safety ground.

- **Color:** Wire used to provide safety ground is to be "Green with Yellow Stripe". This color is reserved for use ONLY as "Safety Earth Ground".
- **Insulation:** CN, PVC, TPE, PTFE, FEP or Neoprene.
- **Minimum Rating:** 80°C, 300V (AVLV2) and a minimum flame rating of VW-1
- **Marking:** The wire insulation surface shall depict UL and CSA Approval Marks and required markings: voltage, temperature, AWG, flame- rating, UL File Number and CSA File Number. The spool of wire must have UL and CSA approval marks and the following required markings: voltage, temperature, AWG, flame rating, UL file number, and the CSA file number. The ground conductor shall be as short as possible. In no case shall the ground conductor be smaller than the power supplying conductors, including consideration of conductors' size used in cord-connected equipment.
- **Routing:** Wire and Cable shall be routed away from mechanically moving parts, sharp edges, heat source, and shall be managed to prevent any damage to insulation.

14.7.1.13 Wiring Harness

A Wiring Harness is an individual wire or multi-conductor cable that has one or more terminating devices provided (connectors).

- **Material:** During material selection (connectors/wire/cable/insulating tubing or sleeving) designer must consider the application to ensure adequate voltage, current, temperature and flame ratings and appropriate safety agency certifications and meet all Marking requirements
- **Insulating tubing or Sleeving:** Insulating tubing or Sleeving shall be rated at a minimum: 105°C, 300V. The material may be FEP, PTFE, PVC, TFE or Neoprene, and shall have a flame rating of VW-1.
- **Manufacturer Selection:** Manufacturer must have UL Wiring Harness Factory Approval.
- **Routing:** Wire harness shall be routed away from mechanically moving parts, sharp edges, heat source, and shall be managed to prevent any damage to wire/cable insulation, insulating tubing, or sleeving.

14.8 Testing

All testing for safety and EMC/EMI compliance for the PSU and all critical components where necessary shall be conducted with the relevant test reports issued from a test lab that has been accredited by an internationally recognized third-party testing laboratory accreditation authority such as APLAC, A2LA, ILAC or NVLAP.

14.8.1 Wireless GSM Test

The purpose of the test is to evaluate a system's immunity to radiated fields generated by a GSM wireless device (e.g., GSM/GPRS PCMCIA Card) when placed in close proximity to the system under test. This requirement is in addition to the legal requirements set forth in CISPR 35 and IEC 61000-4-3.

The following test method was developed - Wireless Immunity "Wand Test" for this requirement. The "Wand Test" utilizes a small test antenna (Wand Antenna) to create an E-field closely matching the frequency, field level, and modulation characteristics generated by the wireless device in question. The use of the "Wand Test" allows the tester to replicate any of several GSM device transmit frequencies, as well as to replicate the typical maximum output drive that such GSM devices might produce when attempting to communicate with a remote cell tower.

The preferred equipment is:
- Boonton 4232A RF Power Meter
- IFR 2032 10kHz – 5.4 GHz Signal Generator
- Amplifier Research 10S1G4A, 10-Watt (0.8-4.2GHz) Power Amplifier
- HP8566B Spectrum Analyzer (Used for monitoring of field level – not calibrated measurement.)
- Amplifier Research DC7420 Directional Coupler (0.8-18 GHz)
- Boonton 51011(4B) Power Sensors
- Small Vertical Antenna (Log periodic dipole)
- Wireless Immunity "Wand" Antenna

The Wand antenna is a stub antenna which is fixed in length to the wavelength for the frequency band of concern. For the GSM band 850/900 and 1800/1900 bands, the antenna stub length has been set to 8.4 cm, which closely **matches the λ/4 and λ/2 wavelengths** of these bands, respectively. A 3/8-inch dielectric spacer is placed around the Wand antenna to maintain a consistent spacing during the actual "Wand Test. The antenna stub portion is created by stripping back the outer shield portion of a semi-rigid coaxial cable and leaving a stub of length as defined above.

The test setup is as illustrated in Figure *14-1 Wireless Immunity "Wand Test" Setup (PSU Level)* and *Figure 14-2 Wireless Immunity "Wand Test" Setup (External Power Supply)*. *Figure 14-1* is the test setup for a system level test. *Figure 15-2* is the test setup for an external power supply test. The signal generator is set to the signal characteristics as describe the Procedure Section and the forward power is monitored to ensure the correct field level is applied.
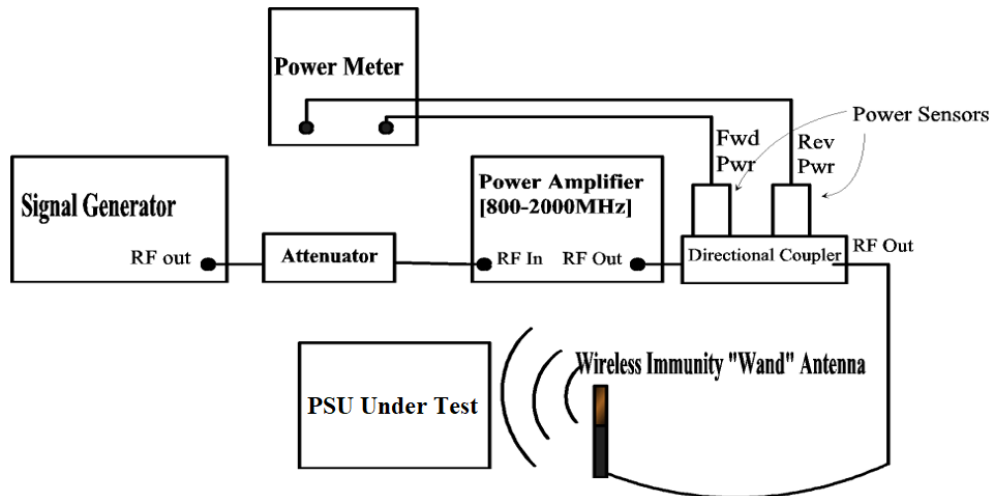
Figure 14-1 Wireless Immunity "Wand Test" Setup (PSU Level)
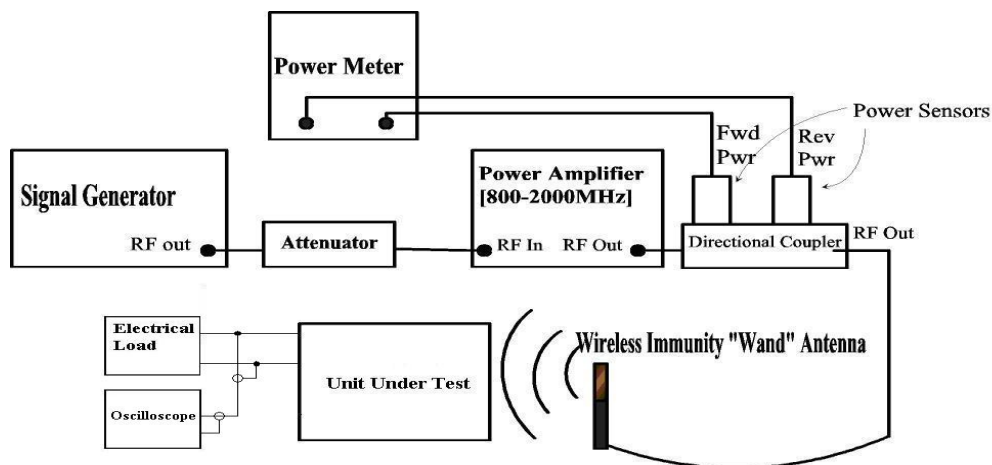
Figure 14-2 Wireless Immunity "Wand Test" Setup (External Power Supply)

14.8.2 Procedure

In performance of the "Wand Test", the wand antenna is used to create an E-field to match the frequency, field level, and modulation characteristics generated by a wireless device. The actual forward power applied to the Wand antenna is dependent on the GSM band.

For the GSM 850/900 bands the forward power is set to 5.5-Watts CW.
Test Frequencies:
- GSM 850 – 824, 836, & 849 MHz
- GSM 900 – 880, 900, & 915 MHz

Forward Power: 5.5 Watts (37.4 dBm) CW. (Forward power set without modulation).
Modulation: Pulsed with rep rate at 220 Hz and pulse width at 500 μs (11% Duty Cycle).

For the GSM 1800/1900 bands the forward power is set to 1.5-Watts CW.
Test Frequencies:

- GSM 1800 – 1710, 1750, & 1785 MHz
- GSM 1900 – 1850, 1880, & 1910 MHz

Forward Power: 1.5 Watts (31.8 dBm) CW. (Forward power set without modulation).
Modulation: Pulsed with rep rate at 220 Hz and pulse width at 500 µs (11% Duty Cycle).

Forward power to the wand is initially set without modulation applied. After the proper forward power drive level is established, the modulation is then applied.

Modulation shall be set to pulse modulation with a repetition rate of 220Hz and a pulse width of 500 µs. These levels and modulation characteristics were obtained from both product technical specifications and empirical data taken in the lab.

 In general, the Wand antenna is swept across the system/power supply (front, back, sides, top and bottom) in two orthogonal planes and the system is monitored for susceptibility.

14.8.3 Severity Levels and Performance Criteria

For System Level Testing:

The system under test should be immune to the frequencies, modulation and field levels listed above. After the test, the EUT shall continue to operate as intended without operator intervention (i.e., Performance Criteria B).

For External Power Supplies:

The performance criteria for the external power supply test is given below:

- Power good signal: Test with PS_ON high (inactive) and low (active). Power good signal should not change from high to low or from low to high.
- All DC output voltages: Test with PS_ON low (active). All DC output voltages should stay within the power supply specification.

Environmental Conditions

The environmental conditions for this testing are the same as specified in EN 61000-4-3:

- Ambient temperature: 15°C to 35°C
- Relative humidity: 30% to 60%
- Atmospheric pressure: 86 kPa (860 mbar) to 106 kPa (1060 mbar)

14.9 Energy Efficiency Requirements and Standards

The power supply must meet the following energy efficiency requirements as applicable for its use. The following are mandatory.

Table 14-2 Mandatory regulation requirements

Regulation	Version	Comments
ErP Lot 3		
ErP Lot 9	Tier I or Tier II	
ErP Lot 9	Tier III	For products shipping after the effective date of 1/1/2023

Japanese Energy Law (JEL)	Phase I Implementation, voluntary disclosure	Power supply to support the end product compliance
	Phase II mandatory disclosure	Power supply to support the end product compliance
	Phase III mandatory compliance	Power supply to support the end product compliance For products shipping after the effective date of 4/1/2022

Consider the intended use of the power supply in the final end product to comply with the following voluntary requirements.

Table 14-3 Voluntary regulation requirements

Regulation	Version	Comments
China CEC	-	
China CECP	-	
ENERGY STAR ® [2]	Server 3.0	
EPEAT for servers	NSF-426	Allowable temperature and humidity specifications
Brazil INMETRO	Small scale servers	

Figure 14-3 Brazil INMETRO Efficiency Requirements for Internal Power Supplies (tested @ 127V/60Hz)

Small- scale server		
Loading Condition (Percentage of Nameplate Output Current)	Minimum Efficiency	Minimum Power Factor
20%	0.82	-
50%	0.85	-
100%	0.82	0.90

Table 14-4 European Union ErP Lot 9 Efficiency Requirements for Internal Power Supplies (tested @ 230V/50Hz)

Computer Servers (1 March 2020) - Computer servers all single output (AC-DC) power supplies							
10% Load		20% Load		50% Load		100% Load	
Efficiency	Power Factor	Efficiency	Power Factor	Efficiency	Power Factor	Efficiency	Power Factor
-	-	90%	-	94%	0.95	91%	-
					-		
Computer Servers (1 January 2023) - Computer servers all single output (AC-DC) power supplies							
10% Load		20% Load		50% Load		100% Load	
Efficiency	Power Factor	Efficiency	Power Factor	Efficiency	Power Factor	Efficiency	Power Factor
90%	-	94%	-	96%	0.95	91%	-
					-		

Table 14-5 ENERGY STAR Requirements for Servers 3.0

ENERGY STAR Servers 3.0 Efficiency Requirements for PSUs					
Power Supply Type	Rated Output Power	10% Load	20% Load	50% Load	100% Load
Single-output (AC-DC)	All Output Levels	83%	90%	94%	91%
ENERGY STAR Servers 3.0 Power Factor Requirements for PSUs					
Power Supply Type	Rated Output Power	10% Load	20% Load	50% Load	100% Load
AC-DC Single-output	Output Rating ≤ 500 W	N/A	0.80	0.95	0.95
	Output Rating > 500 W and Output Rating ≤ 1,000 W	0.65	0.80	0.95	0.95
	Output Rating > 1,000 watts	0.80	0.90	0.95	0.95

Table 14-6 ENERGY STAR Requirements for Data Center Storage 2.0

ENERGY STAR Data Center Storage 2.0 Efficiency Requirements for PSUs				
Power Supply Type	Rated Output Power	20% Load	50% Load	100% Load
Single-output (AC-DC)	All Output Levels	90%	94%	91%
ENERGY STAR Data Center Storage 2.0 Power Factor Requirements for PSUs				
Single-output (AC-DC)	Rated Output Power	20% Load	50% Load	100% Load

Power consumption requirements for the following should be considered as a best design practice as part of an ecolabel.

- Energy efficiency for internal power supplies:
  - o 1 full 80 Plus efficiency level above minimum efficiency level U.S. ENERGY STAR specification.
  - o 2 full 80 Plus efficiency level above minimum efficiency level U.S. ENERGY STAR specification.
- Make use of energy-efficient components and techniques to reduce power consumption whenever possible.
- Consider low power components and design options as well as efficient power supply components.
- Properly specify the power supply rating to match the loading profile for an energy efficient design.
- Ensure power supplies and components meet requirements for energy efficiency.
- Consider design options to automatically switch from one power mode to another where practical.
- Consider ASIC's and other IC's that have been optimized for low power consumption.
- Consider selection of silicon device technologies noted for higher power efficiencies (CMOS over linear, etc.).
- Keep clock frequencies as low as possible to achieve a given functional task.
- For non-critical impedance circuits, keep bias currents to a minimum (pull-up/down resistors as high as possible for instance).
- Utilize drive spin down in storage systems when data on those drives is not in use over long idle periods.
- Make use of tri-state conditions during idle periods as much as possible.
- Utilize the proper cabling in power distribution paths to minimize supply loss.
- Utilize high efficiency LED's, low-power drivers, etc. whenever possible.
- Place the main power switch in a location the customer can easily locate and utilize whenever possible.
- Provide system power monitoring capabilities for the customer whenever possible.

14.10 Environmental Requirements and Standards

The following is required by law or mandated in ecolabel criteria

- Power supply must comply with applicable restriction on hazardous substances as referenced in RoHS, REACH, or other environmental and material requirements, including relevant national, regional, and international requirements.
- Consideration must be given to supporting the TCO and EPEAT declarations for the platform level commodities. The power supply must meet all TCO requirements and all EPEAT "Required'

criteria at a minimum and any requirements imposed by the platform level declarations. Refer to the latest TCO and EPEAT (NSF-ANSI-426 latest edition) standards for a full list of the requirements.

- Plastic parts exceeding 25 g shall not contain greater than 1000 ppm chlorine or greater than 1000 ppm Bromine. Reduction of Br/Cl content of plastic parts > 25 grams (Ref EPEAT 6.1.3)
- Halogenated flame retardants and plasticizers - Product housing above 0.5 grams and the power PCB laminate of the internal/external power supply unit must not contain intentionally added (additive or reactive) flame retardants or plasticizers with halogenated substances. Exempted are all other parts, such as electronic components, other PCB laminates and all kinds of cable insulation. Maximum concentration values tolerated for a restricted substance (including decaBDE) is 0.1% by weight of the material in homogeneous materials. (Ref TCO 7.2.1)
- The power supply must not contain Polybrominated biphenyls (PBB), polybrominated diphenyl ethers (PBDE) and Hexabromocyclododecane (HBCDD) (No parts of the product are exempt). (Ref to TCO 7.2.1)
- Non-Halogenated flame retardants - Product housing above 0.5 grams and the power PCB laminate of the internal/external power supply unit must only contain intentionally added (additive or reactive) non-halogenated flame retardants that have been assigned a GreenScreen benchmark score of 2, 3 or 4 by a licensed GreenScreen Profiler and appear on the public TCO Certified Accepted Substance List. All substances of a mixture must be accounted for. Non-accepted substances must not exceed concentration levels of 0.1% by weight of the flame retardant. (Ref TCO 7.3.1)
- Plasticizers – Plasticizers used in product housing and cable insulations must have been assigned a Green Screen benchmark score of 2, 3 or 4 by a licensed Green Screen profiler and appear on the public TCO Certified Accepted Substance List. The product must not contain Bis (2-ethylhexyl) phthalate (DEHP), Butyl benzyl phthalate (BBP), Dibutyl phthalate (DBP), and Di-isobutyl phthalate (DIBP). No parts of the product are exempted. All substances of a plasticizer mixture must be accounted for. Non-accepted ingredients must not exceed concentration levels of 0.1% by weight of the plasticizer. (Ref TCO 7.4.1)

The following materials are restricted by the EU RoHS Directive (2011/65/EU) and cannot be used in Power Supplies unless used as described in the exemptions.

- Lead and its compounds (0.1% w/w)
- Mercury and its compounds (0.1% w/w)
- Cadmium (0.01% w/w)
- Hexavalent Chromium (0.1% w/w)
- Polybrominated Biphenyls (PBB) (0.1% w/w)
- Polybrominated Diphenyl Ethers (PBDE) (0.1% w/w)
- Bis(2-Ethylhexyl) phthalate (DEHP) (0.1% w/w)
- Benzyl butyl phthalate (BBP) (0.1% w/w)
- Dibutyl phthalate (DBP) (0.1% w/w)
- Diisobutyl phthalate (DIBP) (0.1% w/w)

Plastic parts over 25 grams or 200 mm² planar area must be labeled according to ISO 11469 standard which includes ISO 1043-1, ISO 1043-2, ISO 1043-3, and ISO 1043-4 standards.

Materials restricted under multiple country RoHS rules include but not limited to
Lead and it compounds – not detectable

14.11 Applicable RoHS Exemptions

Only the following RoHS exemptions can be used.

Table 14-7 RoHS Exemptions

Exemption Number	Exemption
4(f)	Mercury in other discharge lamps for special purposes not specifically mentioned in this Annex
6(a)-I	Lead as an alloying element in steel for machining purposes containing up to 0.35% lead by weight and in batch hot dip galvanized steel components containing up to 0.2% lead by weight
6(b)-I	Lead as an alloying element in aluminum containing up to 0,4 % lead by weight, provided it stems from lead-bearing aluminum scrap recycling
6(b)-II	Lead as an alloying element in aluminum for machining purposes with a lead content up to 0,4 % by weight
6(c)	Copper alloy containing up to 4 % lead by weight
7(a)	Lead in high melting temperature type solders (i.e., lead- based alloys containing 85 % by weight or more lead)
7(c)-I	Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g., piezo electronic devices, or in a glass or ceramic matrix compound
7(c)-II	Lead in dielectric ceramic in capacitors for a rated voltage of 125 V AC or 250 V DC or higher
13(a)	Lead in white glasses used for optical applications
15(a)	Lead in solders to complete a viable electrical connection between the semiconductor die and carrier within integrated circuit flip chip packages where at least one of the following criteria applies: • • a semiconductor technology node of 90 nm or larger. • • a single die of 300 mm2 or larger in any semiconductor technology node. • • stacked die packages with die of 300 mm2 or larger, or silicon interposers of 300 mm2 or larger.

14.12 Sustainable Materials

Consider the criteria in IEEE 1680.1 (2009 & 2018) & NSF 426 for percentages of Post-Consumer Recycled plastics. The use of post-consumer recycled materials in plastic components is recommended. (reference EPEAT conformity packets.) Supplier must provide declaration when any part contains recycled content or other sustainable material.

The power supply shall support the end product qualification for the TCO process and product sustainability certification for servers. The specific TCO criteria for the end product type is available at:

https://tcocertified.com/files/certification/tco-certified-generation-8-for-servers.pdf
https://tcocertified.com/files/certification/tco-certified-generation-9-for-servers-edition-2.pdf

14.13 EPEAT

Consideration must be given to supporting the EPEAT declaration for the platform level commodities, the power supply must meet the following criteria at a minimum. Refer to the EPEAT criteria for a full list of the requirements.

1) All criteria listed as 'Required' (where applicable for commodities & peripherals – some criteria are at the system level).
2) Power Supply vendor should declare conformance in writing on company letterhead and signed by the appropriate authority within the company.
3) Power supply vendor should make available the EPEAT material declaration template.
4) Power supply vendor should make available upon demand third party Analytical Test Reports from a reputable lab.

14.14 Design for Recyclability

All products shall be designed with the following recyclability elements. Designing products with specific features, materials, or manufacturing processes that support ease of disassembly and reuse, recovery, or recycling efforts can meet these criteria.

The following is required by law or mandated ecolabel criteria

- Ease of disassembly by one person using commonly available tools. (Ref EPEAT)
- Ease of upgrading and/or reuse of original hardware. (Ref EPEAT)
- Ease of separation of different commodity types (i.e., minimizing fused metal-plastic parts). (Ref EPEAT)
- Elimination of molded-in or glued parts. (Ref EPEAT)
- Paints and coating on plastics part should be compatible with recycling process (IZOD impact. Reference ASTMD256). (Ref EPEAT)
- All large chassis plastics should be composed of a single plastic type. (Ref EPEAT)
- Information identifying the presence and location of all materials and components that require selective treatment. (Ref EPEAT)
- Mark all plastic components weighing 25 g or more with material code in accordance with ISO 11469:2016 labeling scheme. (Ref EPEAT)
- WEEE Documentation: Demonstrate compliance to EU WEEE directive Article 15 by keeping WEEE End of life Instructions available on a website accessible to recyclers for guidance on the presence of materials and components at the product / family level that need to be removed for treatment including disassembly instructions via owners/service manual. Disassembly instruction must show all parts and material as required per Annex VII of the European WEEE Directive, Directive 2012/19/EU. To meet the NSF 426 standard for Server the WEEE End of life instruction must be kept for at least 7 years following end of products of the product. (Ref EPEAT)

All products shall be designed with the following recyclability elements considered:
- Choose materials which are commonly accepted in recycling programs or are easily recyclable.
- Utilize a modular architecture that allows upgrades or repairs to occur easily.
- Provide ease of access to parts or components containing hazardous materials that should be removed before mechanical processing.
- Minimize adhesive backed materials on recoverable components.
- Postconsumer recycled content of rare earth elements in hard drive(s) in product - Products that contain a hard drive(s) with actuator/voice coil or spindle magnets shall contain 5% or more PCR content neodymium or dysprosium by weight of neodymium or dysprosium in the magnet (Ref EPEAT – NSF 426)

Optional (as part of an ecolabel or a recommended design practice.
All products shall be designed with the following recyclability elements in mind.

- Choose materials which are commonly accepted in recycling programs or are easily recyclable.
- Utilize a modular architecture that allows upgrades or repairs to occur easily.
- Provide ease of access to parts or components containing hazardous materials that should be removed before mechanical processing.
- Minimize adhesive backed materials on recoverable components.
- Postconsumer recycled content of rare earth elements in hard drive(s) in product - Products that contain a hard drive(s) with actuator/voice coil or spindle magnets shall contain 5% or more PCR content neodymium or dysprosium by weight of neodymium or dysprosium in the magnet (Ref EPEAT – NSF 426)

The power supply design and manufacturing processes should support the certification/registration of the end product for the following:

- EU WEEE
- EU RoHS
- EPEAT
- ISO 11469:2016
- China RoHS
- CECP
- China Environment Certification

14.15 Batteries

The following is required by law or mandated ecolabel criteria

- Batteries must comply with applicable restriction on hazardous substances as referenced in RoHS, WEEE, EU Battery Directive or other environmental and material requirements, including relevant national, regional, and international requirements.
- The main battery must withstand a minimum of 300 charging cycles with at least 60% of the initial capacity. The minimum amount of charging cycles with at least 60% of the initial capacity for the main battery must be detailed on the certificate. (Ref TCO Certified Generation 8)
- The main battery must be replaceable by the end-user and/or technician. Instructions on how to replace the battery must be available.

Recommended Design Practice
- Batteries should be easy to identify and remove.
- Battery documentation is available to the customer
  - Type of battery,
  - Locations within the product,
  - Proper & safe handling
- Include battery management features that prolong the durability of batteries in the design have
- The product shall contain a long-life battery (Ref. EPEAT 1680.1 – 2018)

- The product shall contain a minimum number of product upgrade or repair features (Ref EPEAT 1680.1 – 2018)
- Lithium-Ion batteries shall be easily removable (Ref EPEAT 1680.1 – 2018)

14.16 Production Testing

Reference EN 50514: Audio, video, and information technology equipment – Routine electrical safety testing in production.

14.17 Dielectric Strength Testing

14.17.1   Dielectric Strength for AC Input Power Supplies

Each unit of production must pass a 2150 Vdc production hi-pot test between primary to chassis ground. The voltage must be ramped up to 2150 Vdc within 1 second and must be maintained at that level for a minimum of 1.2 second without failure.

For a PSU that will be used in an ungrounded system, each unit of production must pass a 4250 Vdc production hi-pot test between primary to chassis ground. The voltage must be ramped up to 4250 Vdc within 1 second and it must be maintained at that level for a minimum of 1.2 second without failure. Each unit must be marked to indicate it passed the test.

14.17.2   Dielectric Strength for DC Input Power Supplies

14.17.2.1 Input voltage ≥ 60 Vdc

Each unit of production power supplies with an input voltage ≥ 60 Vdc supplied from a battery system

having float voltage ≤ 75 Vdc and with Protective Earth Connection must be tested by applying a minimum of 1400 Vdc between the input DC circuit and the PSU ground or chassis. The test voltage shall be ramped for a minimum of 1 second and then maintained at the Test Voltage for at least 1.2 seconds.

14.17.2.2 Input voltage 75 Vdc to 240 Vdc

Each unit of production power supplies with an input voltage between 75 Vdc to 240 Vdc with Protective Earth Connection must be tested by applying a minimum of 2150 Vdc between the primary circuit and the system/product ground or chassis. The test voltage shall be ramped for a minimum of 2.8 second and then maintained at the Test Voltage for at least 1.2 seconds.

14.17.2.3 Input voltage 240 Vdc to 400 Vdc

Each unit of production power supplies with an input voltage between 240 Vdc to 400 Vdc with Protective Earth Connection must be tested by applying a minimum of 2700 Vdc between the primary circuit and the system/product ground or chassis. The test voltage shall be ramped for a minimum of 2.8 second and then maintained at the Test Voltage for at least 1.2 seconds.

14.18 Ground Continuity Testing

Each unit of production must pass a production ground continuity test at 25 A for at least 1 s with less than 0.1 ohm from the safety ground (third wire) input pin to the power supply chassis. Each unit must be marked to indicate it.

14.19 Expectation of the Supplier

14.19.1   Change Notification

If the material, component, assembly, or product being supplied to purchaser does not meet one or more of the applicable requirements of this specification, the supplier must immediately notify the purchaser. This notification also applies if the supplier or a subcontractor(s) makes changes in their operations that will cause a material, component, assembly, or product to no longer comply with this specification.

If a restricted substance is used in a nonexempt application above the threshold limit, the following actions may be required to resolve any deviations from this specification:

- Requalification of parts to comply with specification/ phase out and replacement of use, which may result in removal of non-compliant suppliers from the approved vendors list.
- Delay of product launch
- Stop ship of product to affected regions

14.19.2   Required Documentation

The supplier shall provide copies of the latest version of the following items submitted to End-User upon request:

- All agency approval certificates and supporting test reports for EMC, Harmonics, Energy and Product Safety
- UL Descriptive and CB Test Reports
- List of any End User approved Conditions of Acceptability (CoA). While CoA are expected to be detailed in UL report, this list is the documentation showing End User sign-off and approval/acceptance of the PSU CoA.
- Schematics
- BOM (Bill of Material)
- Copy of the PSU label

14.19.3   Regulatory Model Designation

PSU vendor shall utilize a separate Regulatory Model designation for their PSU and should not use their manufacturer part designation/ marketing name/ etc for Regulatory Agency certification purposes. The Regulatory Model designation should not change due to non-Regulatory/ Safety design related features such as firmware updates, etc.

The Regulatory Model designation may include variables, e.g. XXYYZZ to preserve possible Regulatory concerned changes, and the naming scheme shall be approved by the End User Regulatory staff.

14.20 Compliance Certifications

The power supply shall comply with the following safety and EMC/EMI agency approvals.

Table 14-8 Country approval and marking requirements

Country	Agent/Agency/Mark	Certification Requirement M=Mark C=Cert [a] D=DoC	Deliverables C=Cert [a] D=DoC	Comments
Canada	SCC Accredited Agency (Safety)	M, C	C	
Canada	ISED (EMC)	M, D	D	
China	CNCA (Safety, EMC)	M, C	C	China does not require safety certifications for PSUs rated more than 1300 Watts.
European Union	CE (Safety, EMC)	M, D	D	CE Marking. For Class A PSU, the label shall also state "WARNING: Operation of this equipment in a residential environment could cause radio interference"
International CB certificate and report	NCB (Safety)	CB report and certificate	C, CB report	
National authority with factory surveillance	AHJ	M,C	C	Recommended to use the same authority issuing the CB Certificate. Must have a factory surveillance program.
India	BIS (Safety)	M, C	C, BIS report	Apply to detachable power supply (see Note 1) used for the host systems in BIS scope, e.g. server, storage, workstation, AIO, etc. Standalone Switch Mode Power Supplies (SMPS) with output voltage 48 V(max).
Morocco	Morocco (Safety, EMC)	M, D	D	Morocco DoC based on Safety and EMC is required for PSUs.
Korea, Republic of (South Korea)	KC certification (EMC, Safety) EMC – MSIP, Ministry of Science, ICT, and Future Planning	M, C	C	KC mark for EMC applies to Hot Swappable power supplies offered as Customer orderable kits. Also applies to internal power supplies if shipped as customer orderable kit or spare parts.
Eurasia Economic Commission (EEC) (Armenia, Belarus, Kazakhstan, Kyrgyzstan and Russian Federation)	Eurasia Economic Commission (EEC) AKA Customs Union mark and certificate (Safety, EMC)	M, C	C	Hot Swappable power supplies that are offered as Customer orderable kits require agency certification and marking. Also applies to internal power supplies if shipped as customer orderable kit or spare parts.
Taiwan	BSMI (Safety, EMC)	M, C	C	A dc-to-dc power supply does not require BSMI approval. NOTE: Mixed mode high voltage DC PSU that may operate with either an ac or dc input is required to obtain BSMI approval.
United Kingdom	UK CA (Safety, EMC)	M, D	D	UK CA Marking. For Class A PSU, the label shall also state "WARNING: Operation of this equipment

Country	Agent/Agency/Mark	Certification Requirement M=Mark C=Cert [a] D=DoC	Deliverables C=Cert [a] D=DoC	Comments
				in a residential environment could cause radio interference"
United States	NRTL (Safety)	M, C	C	
United States	FCC (EMC)	M, D	D	The 2-part FCC statement on all PSU.

[a] Pursuant to respective Agency certification requirements, it can be CoC (certificate of compliance); LoA (letter of authority); PC: product certificate; RC: Registration certificate; TER: Technical Evaluation Report.

NOTES

1) Definition of detachable power supply for India BIS:
   a) The power supply which is obviously removable/replaceable by the user directly from outside of the host product.
   b) The power supply which is with a mechanism or instructions to lead the user to remove/replace the power supply from outside of the host product simply.
2) The Korea KC-Safety regulates PSU Safety certification installed in a Server. For example:
   a) If PSU used for server and storage at the same time, it is under KC-Safety scope.
   b) If PSU used for storage only, it is not under KC-Safety scope.
3) Korea MSIP (KC-EMC), regulates certification if PSU is sold alone, separate from system, regardless end-system that PSU is used for. For example:
   a) Factory installed PSU used for server, network switch or storage is certified with MSIP (KC-EMC) as component of the host system. PSU that are shipped for service purpose of host is exempted to pursue KC-EMC certificate on PSU.
   b) PSU used for desktop, workstation, server, network switch or storage that are certified with MSIP (KC-EMC) as component of the host system and are marketed/sold/shipped separately from host system as spare part or expansion part shall have its own KC-EMC certificate for the PSU.
   c) For any redundant or hot-swappable PSU must obtain KC-EMC certification

15 Quality Assurance

15.1 Vendor Responsibility

When the power supply vendor takes orders for units to this specification, this vendor then assumes the responsibility of maintaining a standard of quality that meets or exceeds that of units originally qualified in the Design Verification Test.

15.1.1 General

The power supply manufacturer shall establish and maintain an effective quality program, to be submitted and approved by the customer, which will assure adequate quality in all phases of design, procurement, fabrication, and test of power supplies procured in accordance with this specification. The manufacturer shall provide to the customer with all quality program data upon request.

15.1.2 Scope

The power supply manufacturer's quality program shall control all aspects of the acquisition, inspection, storage, and handling of all materials, and the process of fabrication, assembly, test and inspection, packaging, and shipment of power supply assemblies. The program should include, but not be limited to the following elements:

1. Change control of drawings and specifications.
2. Review and control of procurement of parts, materials, and services.
3. Control of vendor/supplier quality.
4. Inspection and test of received parts and materials.
5. Control of non-conforming materials.
6. Material review.
7. Calibration control of tools, gauges, and test equipment.
8. In-process control of test and manufacturing processes.
9. Failure/non-conformance detection, analysis, and correction.
10. Inspection/Test planning.
11. Final inspection/test.
12. Control of packaging and packing.
13. Workmanship standards in conformance with customer's requirements.
14. Corrective action program.

The vendor documentation will be evaluated by The customer to ensure that the documentation is complete and accurate. The power supply will not be fully qualified until the customer approves the documentation. The vendor may be provisionally qualified pending customer's documentation approval. The vendor must provide updated information that accurately reflects any changes or modifications to the power supply.

15.2 Inspection

15.2.1 Responsibility for Inspection/Test

The power supply manufacturer is responsible for performing all inspections and tests required to verify conformance of the power supply to the requirements of this specification.

15.2.2 Inspection and Test Procedure

Inspections or tests which are required to verify that the performance of the power supply assembly complies with the performance requirements of this specification. The customer must approve these procedures prior to incorporating the procedures for production power supply inspection or test. Approval of procedures will include approval of any special test equipment used to verify conformance to the requirements of the specification.

15.2.3 Qualification Inspection/Test Procedures

When qualification is required, the power supply manufacturer will prepare a detailed procedure for the qualification of the power supply to be produced in conformance with this specification. The procedure will specify the test routines, test conditions, number of test units, and duration of tests, test data to be recorded, and the criteria for establishing qualification of the power supply. Qualification procedures are subject to approval by the customer prior to beginning the qualification program.

15.2.4 Acceptance Inspection/Test

The power supply manufacturer shall prepare a detailed procedure specifying the inspection and test routines that will verify that each production power supply conforms to the performance requirements of this specification. The acceptance procedure is subject to approval by the customer. The customer

reserves the right to 100% screening or testing for lot acceptance/rejection based upon sampling per MIL-STD-105K, LEVEL II, per parameters specified in paragraphs 3 through 9 of this specification.

15.3 Final Test Data
The vendor shall ship final test data with each supply until full product qualification.

15.4 Rejection and Retest
Failure of a power supply during acceptance testing to comply with the requirements of this specification shall be cause for rejection. Rejected items will be returned to the vendor for full credit. Rejected items may be reworked and retested for acceptance.

15.5 Corrective Action Program
The power supply manufacturer shall prepare and maintain a corrective action program to be approved by The customer, for the correction of incoming inspection, in process, and field problems when failures are in excess of 0.2%.

15.6 Failure Analysis
The power supply vendor shall provide failure analysis data on all units returned. All units returned to the vendor, shall be at full credit.

15.7 Vendor Burn-In
Minimum initial operating burn-in at 40°C ± 5°C and maximum load is to be included as part of the power supply manufacturing program. The customer may permit fewer hours upon mutual agreement. The customer may require a longer burn-in on a new product. Burn-in must be followed by a final test and inspection. Final test shall include functional, Hi-pot, ground continuity, and AC polarity testing of 100% of units after burn-in.

15.8 Enhanced Burn-In
Enhanced Burn-In test must be performed by vendor in stages EVT & DVT as mandatory and in PVT stage when is required using the following conditions:

AC input	230-240VAC
Temperature	40°C
AC cycling and DC cycling	1 per minute
Slow slew rate dynamic loading (case 1)	D = 50%; Load 0% -100% (5sec at zero, 5 sec –ramp up to 100%, 5 sec at 100%, 5 sec – ramping down)
Fast slew rate dynamic loading (case 2)	D = 50% load 0-60%; 40-100% di/dt=max
Run time	4 hours each condition
Pass criteria	no PWOK de-assertion whenever AC is applied and PSON is asserted
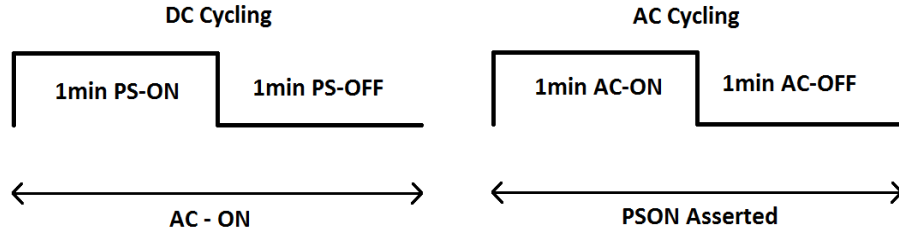
Figure 15-1 AC/DC input cycling pattern.
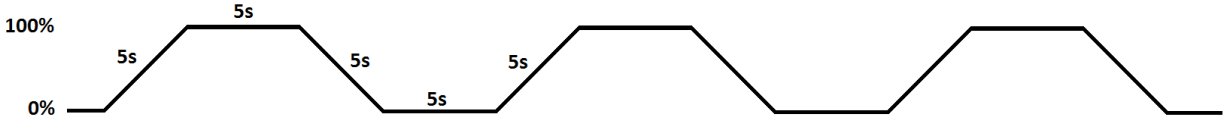
Figure 15-2 Slow slew rate dynamic loading.
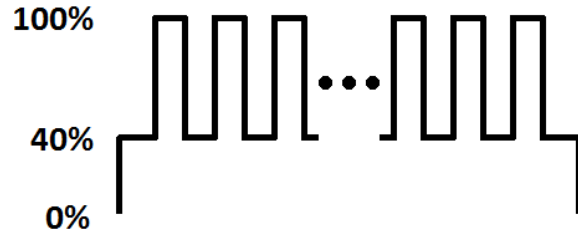
Figure 15-3 Fast slew rate dynamic loading, case 1.
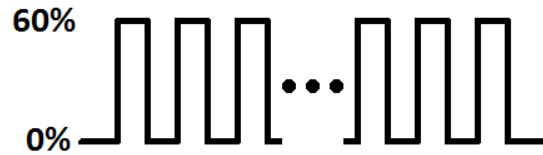
Figure 15-4 Fast slew rate dynamic loading, case 2.

15.8.1 Preparation for Delivery

Each power supply shall be packaged to enable damage-free shipping and handling by commercial carriers to assure safe delivery to the customer facilities worldwide.

Supplemental Material A. 185mm by 73.5mm M-CRPS mechanical drawing
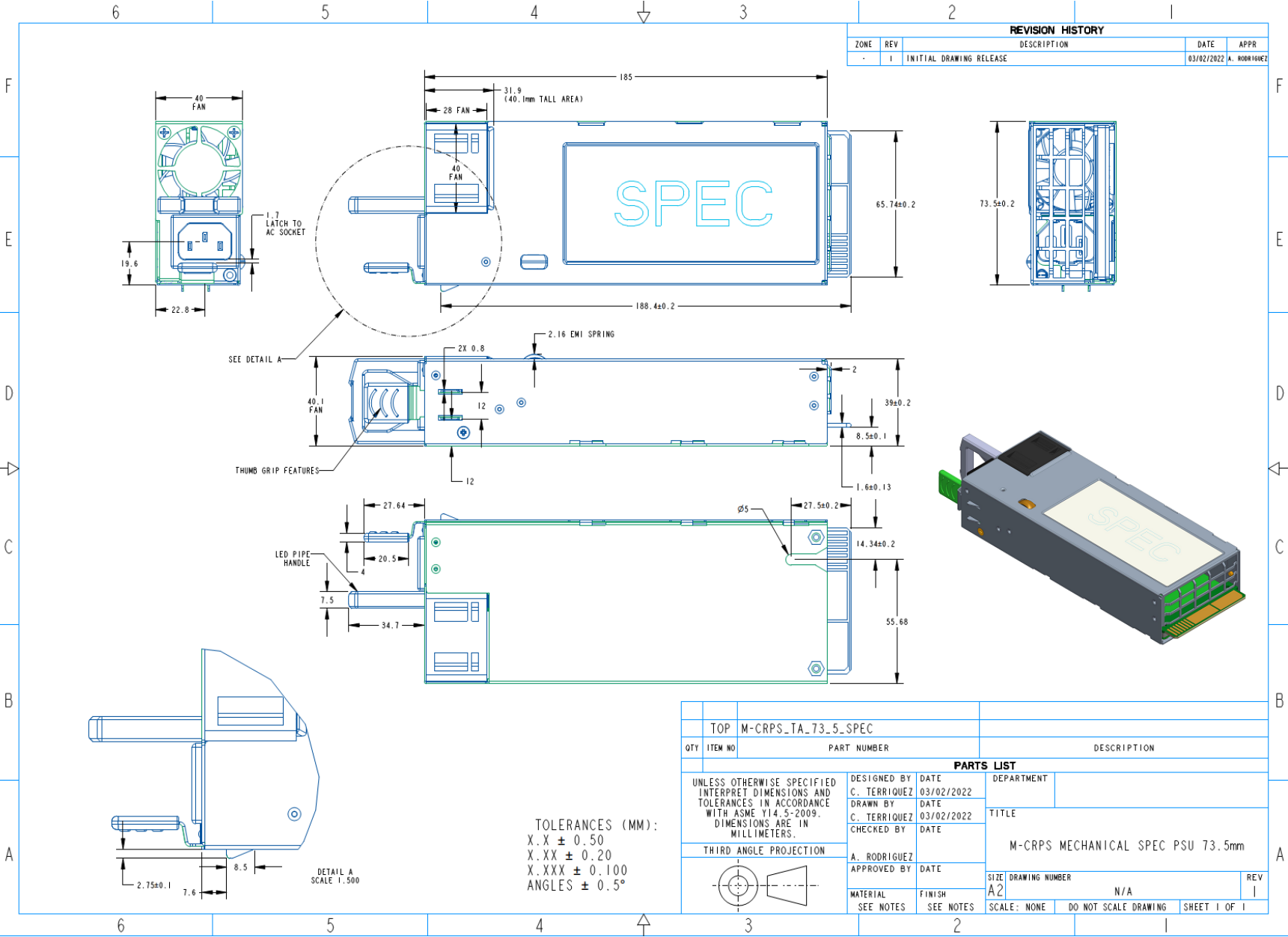
Supplemental Material B. 185mm by 60mm M-CRPS mechanical drawing
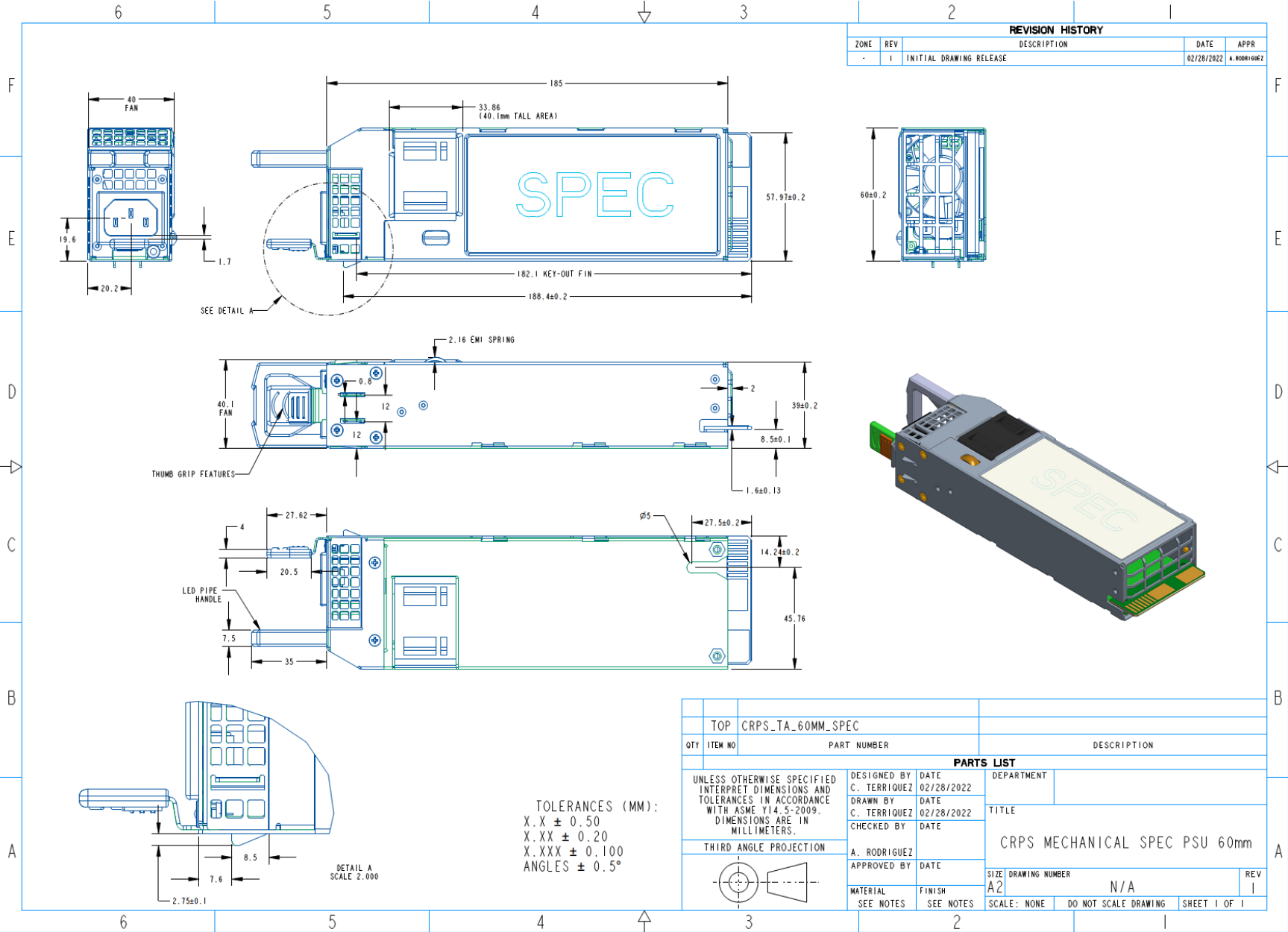
Supplemental Material C.   265mm by 73.5mm M-CRPS mechanical drawing
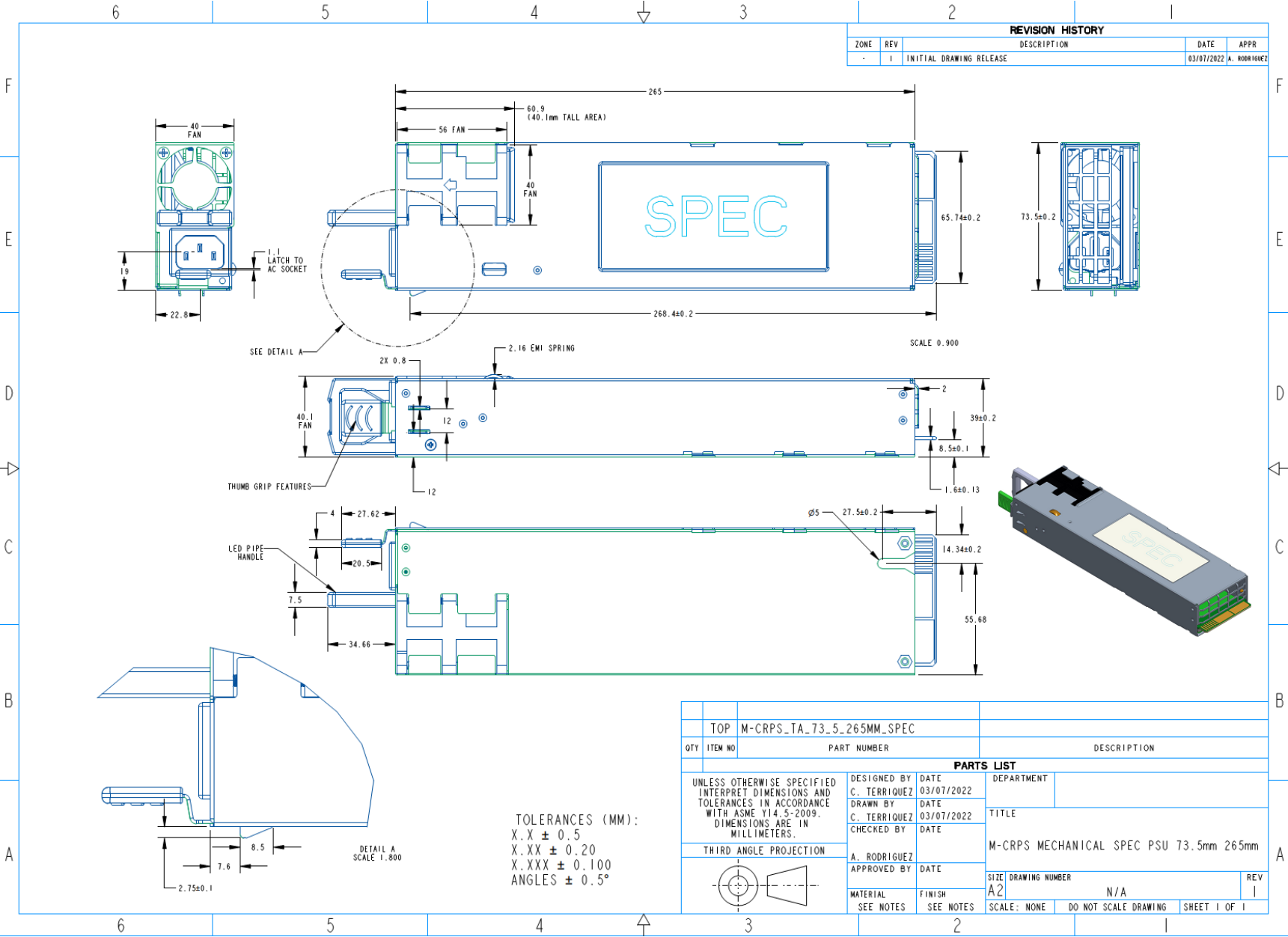
Supplemental Material D. 73.5mm in width M-CRPS card edge mechanical drawing

PCB THICKNESS

1.6±0.13

1.25

TOP VIEW

DETAIL A
SCALE 3.300

6X 2.54

7X 1.5

17.63

2.39

65.74

64.1

42.28

41.24

19.42

1.75

11

SEE DETAIL A

TOLERANCES (MM):
X.X ± 0.25
X.XX ± 0.20
X.XXX ± ---
ANGLES ± 0.5°

REVISION HISTORY					
ZONE	REV	DESCRIPTION		DATE	APPR
-	-	INITIAL DRAWING RELEASE		11/APR/2022	-

QTY	ITEM NO	PART NUMBER	DESCRIPTION
	TOP	CRPS_CARD_EDGE_73_5	CRPS_CARD_EDGE 73.5mm

PARTS LIST

UNLESS OTHERWISE SPECIFIED
INTERPRET DIMENSIONS AND
TOLERANCES IN ACCORDANCE
WITH ASME Y14.5-2009.
DIMENSIONS ARE IN
MILLIMETERS.

THIRD ANGLE PROJECTION

DESIGNED BY	DATE	DEPARTMENT	
C. TERRIQUEZ	03/30/2022	SYS DEV	
DRAWN BY	DATE		
C. TERRIQUEZ	11/APR/2022	TITLE	
CHECKED BY	DATE		
A. RODRIGUEZ	03/30/2020	CRPS_CARD_EDGE 73.5mm	
APPROVED BY	DATE	SIZE A3	DRAWING NUMBER	REV
MATERIAL SEE NOTES	FINISH SEE NOTES	SCALE: NONE DO NOT SCALE DRAWING	SHEET 1 OF 3

Supplemental Material E. 60mm in width M-CRPS card edge mechanical drawing

TOP VIEW

1.6±0.13

1.25

1.75

57.1   57.97

42.27

33.68

19.4

SEE DETAIL A

6X 2.54

17.61

7X 1.5

2.39

7X 1.75

11

DETAIL A
SCALE 3.500

TOLERANCES (MM):
X.X ± 0.25
X.XX ± 0.20
X.XXX ± ---
ANGLES ± 0.5°

PARTS LIST

	TOP	CRPS_CARD_EDGE_60MM	CRPS_CARD_EDGE_60mm
QTY	ITEM NO	PART NUMBER	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
INTERPRET DIMENSIONS AND
TOLERANCES IN ACCORDANCE
WITH ASME Y14.5-2009.
DIMENSIONS ARE IN
MILLIMETERS.

THIRD ANGLE PROJECTION

DESIGNED BY	DATE	DEPARTMENT
C. TERRIQUEZ	03/30/2022	
DRAWN BY	DATE	
C. TERRIQUEZ	11/APR/2022	TITLE
CHECKED BY	DATE	
A. RODRIGUEZ	06/MAR/2020	CRPS_CARD_EDGE_60mm
APPROVED BY	DATE	
MATERIAL	FINISH	
SEE NOTES	SEE NOTES	

SIZE: A3   DRAWING NUMBER   REV: 1

SCALE: NONE   DO NOT SCALE DRAWING   SHEET 1 OF 3

Supplemental Material F.   M-CRPS handle mechanical drawing

Supplemental Material G. M-CRPS latch mechanical drawing

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPR
-	-	INITIAL DRAWING RELEASE	08/APR/2022	-

EMBOSS

10.8

SCALE 2.000

24.74

51.69

61.69

6.5

3.5

12

1.074

4.6

6.6

100°

66.69

	TOP	CRPS-RELEASE-LATCH_1_1	
QTY	ITEM NO	PART NUMBER	DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED
INTERPRET DIMENSIONS AND
TOLERANCES IN ACCORDANCE
WITH ASME Y14.5-2009.
DIMENSIONS ARE IN
MILLIMETERS.

THIRD ANGLE PROJECTION

DESIGNED BY	DATE	DEPARTMENT	
C. TERRIQUEZ			
DRAWN BY	DATE		
C. TERRIQUEZ	08/APR/2022	TITLE	
CHECKED BY	DATE		
		M-CRPS LATCH	
APPROVED BY	DATE	SIZE	DRAWING NUMBER	REV
A. RODRIGUEZ	A. RODRIGUEZ	A3	N/A	1
MATERIAL	FINISH			
SEE NOTES	SEE NOTES	SCALE: NONE	DO NOT SCALE DRAWING	SHEET 1 OF 1

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Supplemental Material H. M-CRPS latch plastic grip option 1 (snap-in version)

ZONE	REV	DESCRIPTION	DATE	APPR
-	-	INITIAL DRAWING RELEASE	11/APR/2022	A. RODRIGUEZ

TOP	M-CRPS LATCH FINGER GRIP		

QTY	ITEM NO	PART NUMBER	DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED
INTERPRET DIMENSIONS AND
TOLERANCES IN ACCORDANCE
WITH ASME Y14.5-2009.
DIMENSIONS ARE IN
MILLIMETERS.

THIRD ANGLE PROJECTION

DESIGNED BY	DATE	DEPARTMENT
DRAWN BY C. TERRIQUEZ	DATE 11/APR/2022	TITLE
CHECKED BY	DATE	M-CRPS_LATCH_FINGER_GRIP
A. RODRIGUEZ		
APPROVED BY	DATE	SIZE A3 DRAWING NUMBER 1 REV 1
MATERIAL SEE NOTES	FINISH SEE NOTES	SCALE: NONE DO NOT SCALE DRAWING SHEET 1 OF 1

214

Supplemental Material I.   M-CRPS latch plastic grip option 2 (over molded version)

REVISION HISTORY

ZONE	REV	DESCRIPTION	DATE	APPR
-	-	INITIAL DRAWING RELEASE	11/APR/2022	-

0.5 FINGER GRIP

12 15

10 4.5

PARTS LIST

	TOP	M-CRPS_LATCH_FINGER_GRIP	
QTY	ITEM NO	PART NUMBER	DESCRIPTION

UNLESS OTHERWISE SPECIFIED
INTERPRET DIMENSIONS AND
TOLERANCES IN ACCORDANCE
WITH ASME Y14.5-2009.
DIMENSIONS ARE IN
MILLIMETERS.
THIRD ANGLE PROJECTION

DESIGNED BY — DATE — DEPARTMENT
DRAWN BY C. TERRIQUEZ — DATE 11/APR/2022
CHECKED BY — DATE
APPROVED BY — DATE
A. RODRIGUEZ

TITLE M-CRPS_LATCH_FINGER_GRIP

SIZE A3 DRAWING NUMBER REV

MATERIAL SEE NOTES FINISH SEE NOTES

SCALE: NONE DO NOT SCALE DRAWING SHEET 1 OF 1

Supplemental Material J.   185mm by 73.5mm +54VDC input M-CRPS mechanical drawing

**185mm by 73.5mm +54VDC input
M-CRPS mechanical drawing**

Supplemental Material K.   185mm by 73.5mm -48VDC input M-CRPS mechanical drawing

**185mm by 73.5mm -48VDC input
M-CRPS mechanical drawing**

Supplemental Material L. DC input impedance measurement procedure

Test Set-Up

The setup circuit is shown in *Figure L-1*, NMOS are used in parallel (number of devices in parallel depend on the maximum input current rating current of the PSU under test. Resistor R2 can be picked at 100kΩ, that capacitor could be 1uF (needs to >> MOSFET Cgs), R1 is 100Ω.

The NMOS selection depends on input voltage, if input is from 36VDC to 72VDC, this MOSFET needs to have a voltage rating of 100VDC typically. One example is IPB025N10N3, multiple NMOS transistors could be used in parallel. The power loss on these NMOS is significantly high, for example, if the DC operating point is 20A, and the voltage drop on those NMOS are same as V_{gs}, for example, 4V, this will give 80W loss. You need attach suitable heat-sink to these MOSFETs and recommend using a Fan to cool it.

For CH-B, you need check the probe attenuation (10:1 or 100:1) to make sure the signal is within the safe range of Analyzer, you can also use differential probe.

For CH-A, current probe can be used with a bandwidth at least 1MHz. Instead use of suitable shunt resistor (with low ESL) can be made to measure the current.
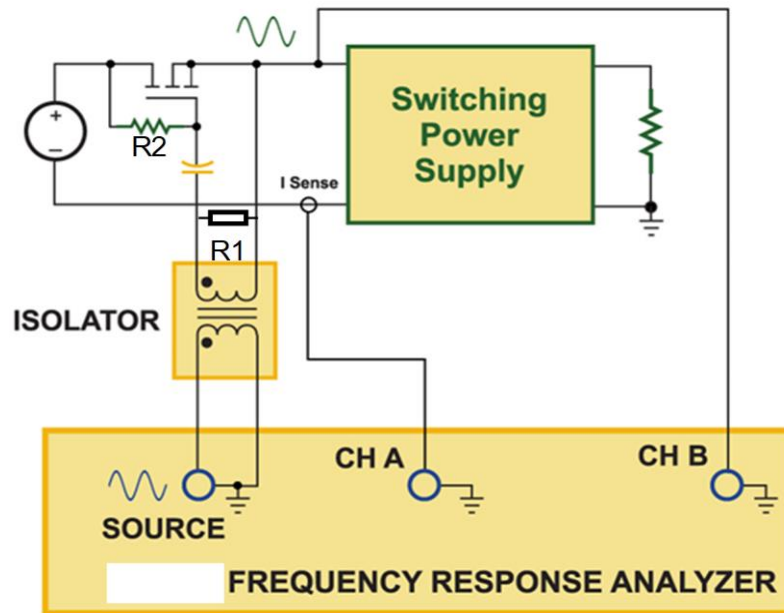

Figure L-1. Input Impedance Measurement Setup

The excitation level should be set at 50mV ~100mV. The excitation level should be as small as possible while still being able to get a clean plot. The scanning frequency span should be from 10Hz to 100kHz typically.

Once the set-up is finalized, PSU under test is ready to be tested.
The test is to be performed at following Input and Load conditions:
Input Voltage – Minimum, Typical, Maximum

Typical Examples:

- 240Vdc Input PSUs – 192Vdc, 240Vdc, 288Vdc.
- -48Vdc Input PSUs - -40Vdc (or -36Vdc as the case may be), -48Vdc, -72Vdc.
- 400Vdc Input PSUs – 192Vdc, 240Vdc, 336Vdc, 400Vdc.

The output load shall be swept from no Load to 100% load in steps of 10%. Impedance and phase plots shall be from 10Hz to 100KHz. Typical plot looks like (recommended method is to have both plot impedance and phase data in one plot):
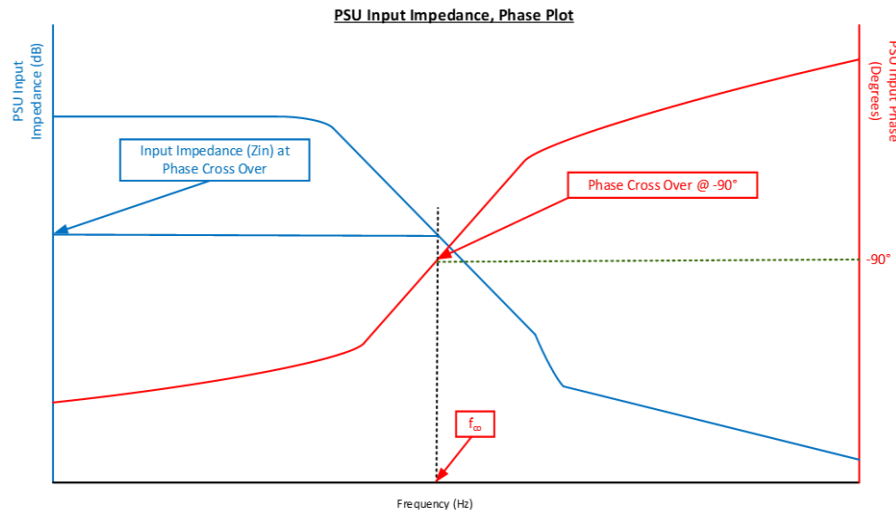

Figure L-2. Sample Impedance / Phase Plot

Once the plot is done, obtain value of f_{co}, the frequency at which the phase crosses -90° point. Then note the value of Z_{in} and after converting the value to Ohms, calculate the inductance at this point with:

$$L_{in} = \frac{Z_{in}}{2\pi F_{co}}$$

Value of L_{in} is to be calculated at each input and load conditions defined above. From the data, determine the lowest value of L_{in}, this value obtained should be ≥ minimum value called out in *Section 5.3.4 Input Impedance.* The data shall be submitted and be accompanied by raw Data from Analyzer and all plots. A sample is shown below:

Table J-1. -48VDC or 240V/380VDC input power supply input impedance

Load (%)	Frequency (Hz)	Impedance (Ω)	Lin(mH)
0%			
10%			
20%			
30%			
40%			
50%			
60%			
70%			

80%			
90%			
100%			

Note: One table per DC input condition shall be provided.

The main outputs of the power supply must turn off per Vin (turn-off) of the applicable line status range. Standby output shall turn on within the turn on thresholds of the lowest operational input voltage range and shall continue to operate at input voltages below minimum Vin (turn-off) threshold of lowest operational input voltage range.

Power supply design must assure no turn-on/off cycling occurs for DC line impedance defined in the Design Specification.

Appendix A -   Checklist for IC approval of this specification

(To be completed by contributor(s) of this Spec)

Complete all the checklist items in the table with links to the section where it is described in this spec or an external document.

> **Note:** This will be filled out at v1.0.

Appendix B - OCP Supplier Information and Hardware Product Recognition Checklist

This is a Base Specification, and no specific designs can be derived from this specification. Future Design Specifications will be established based on DC-MHS Rev 1.0 specifications, and supplier information and HW checklist will be applicable and filled by future contributors.

End of document.