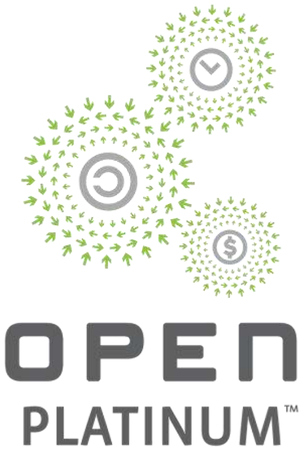
Open. Together.

OCP
REGIONAL
SUMMIT

Motivation for ODSA & Fit into OCP

Dharmesh Jani (DJ)
OCP Co-chair and Open Ecosystem Lead
Facebook



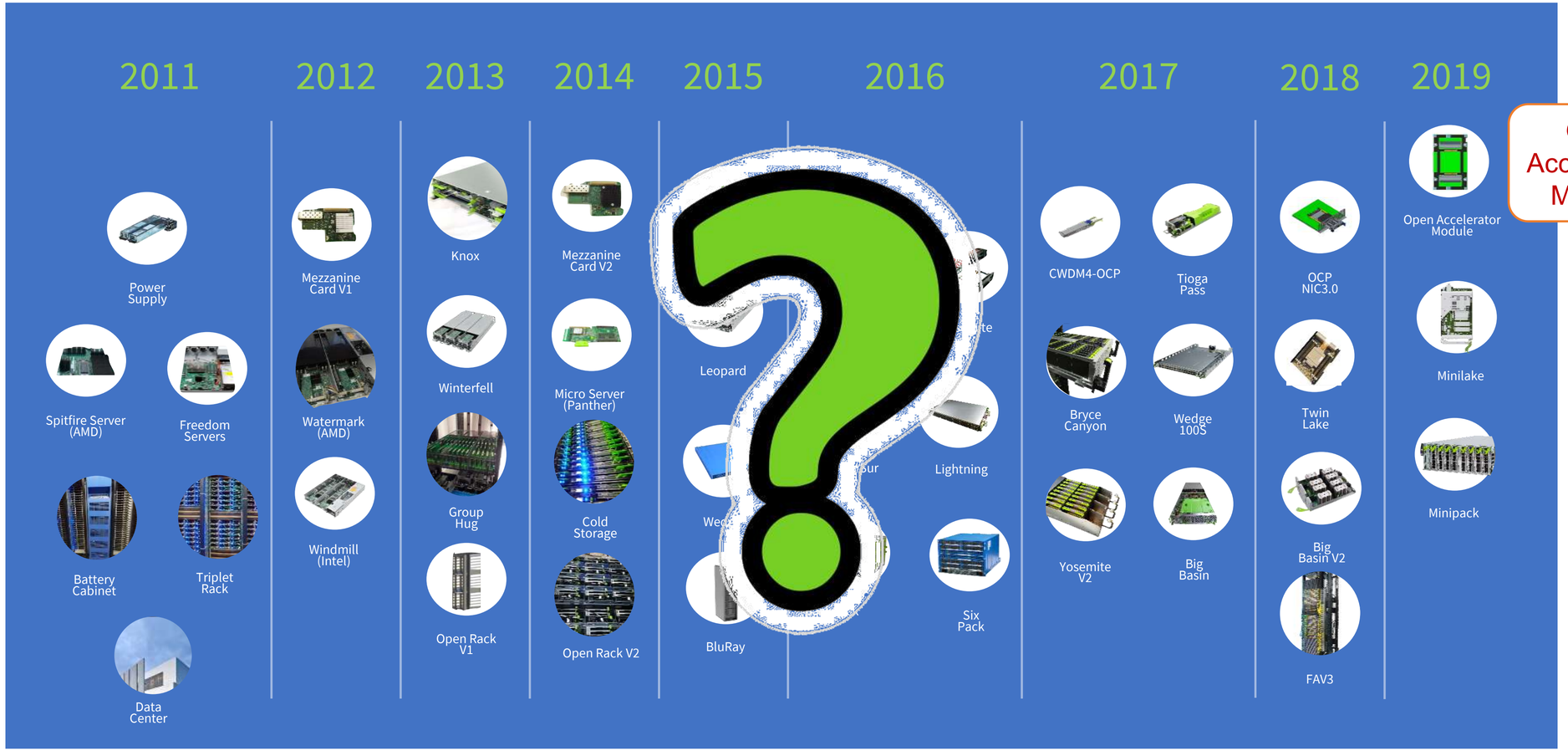
OCP continues to evolve and grow

MODULES

SUB-SYSTEMS

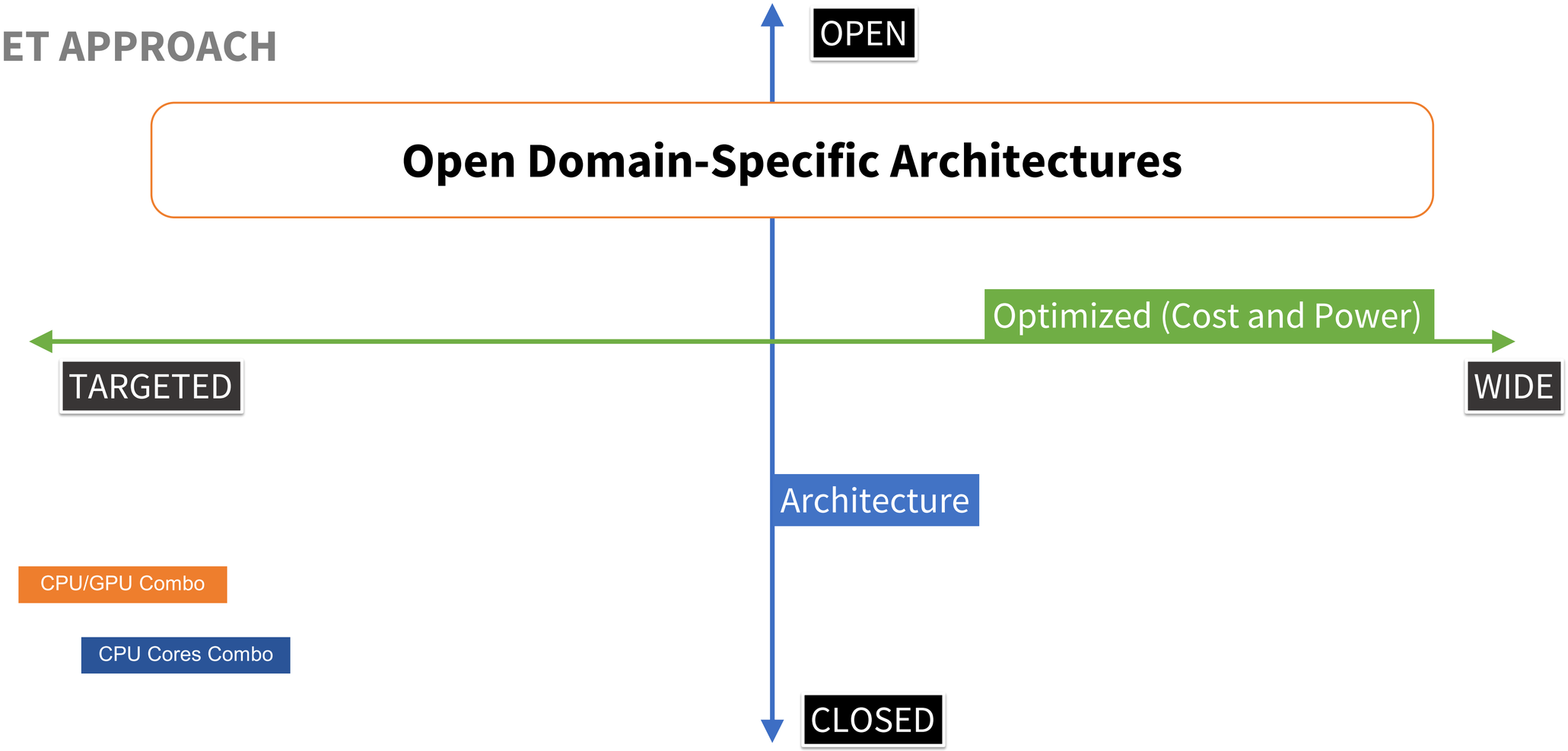
SYSTEMS

DATA CENTERS



Open Domain-Specific Architecture (ODSA)

CHIPLET APPROACH



ODSA: Natural Next Step for OCP

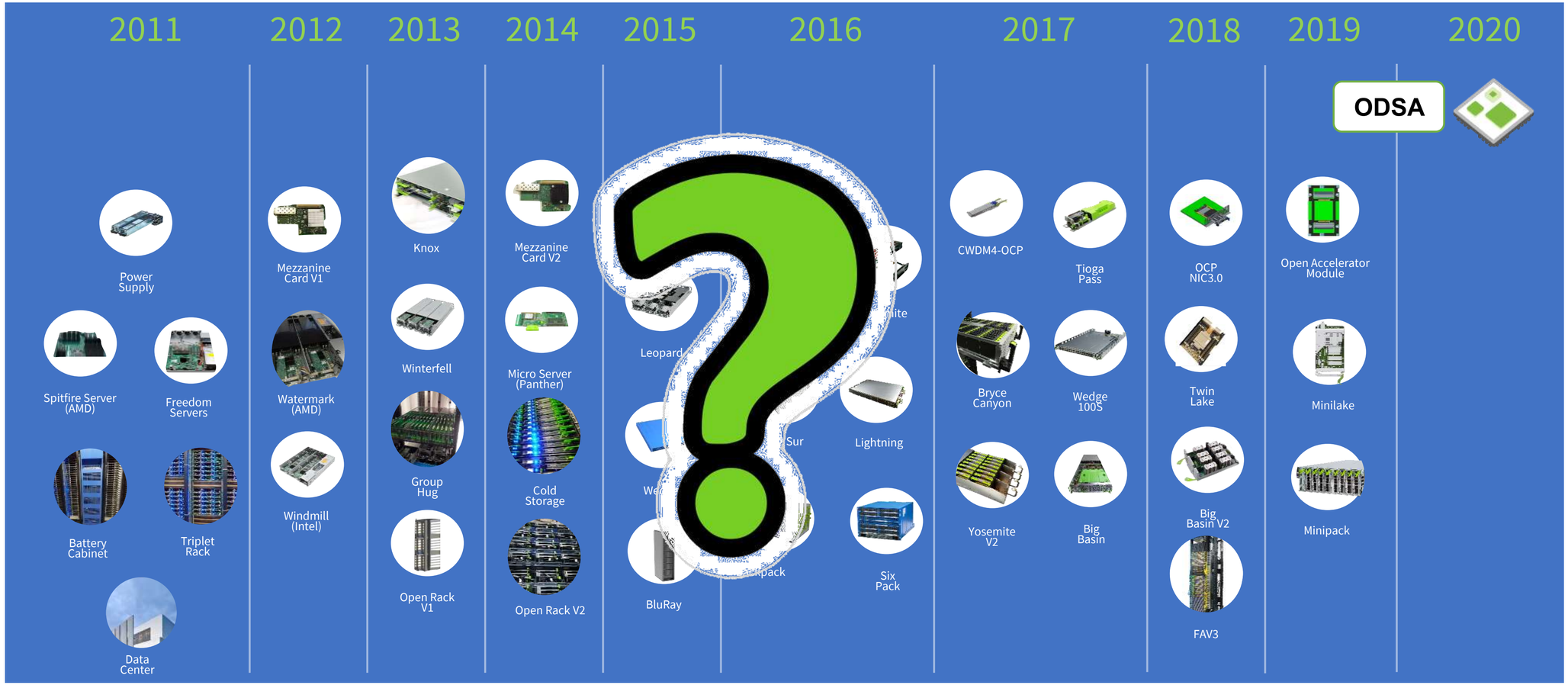
SUB-MODULES COMPONENTS

MODULES

SUB-SYSTEMS

SYSTEMS

DATA CENTERS



ODSA: Natural Next Step for OCP

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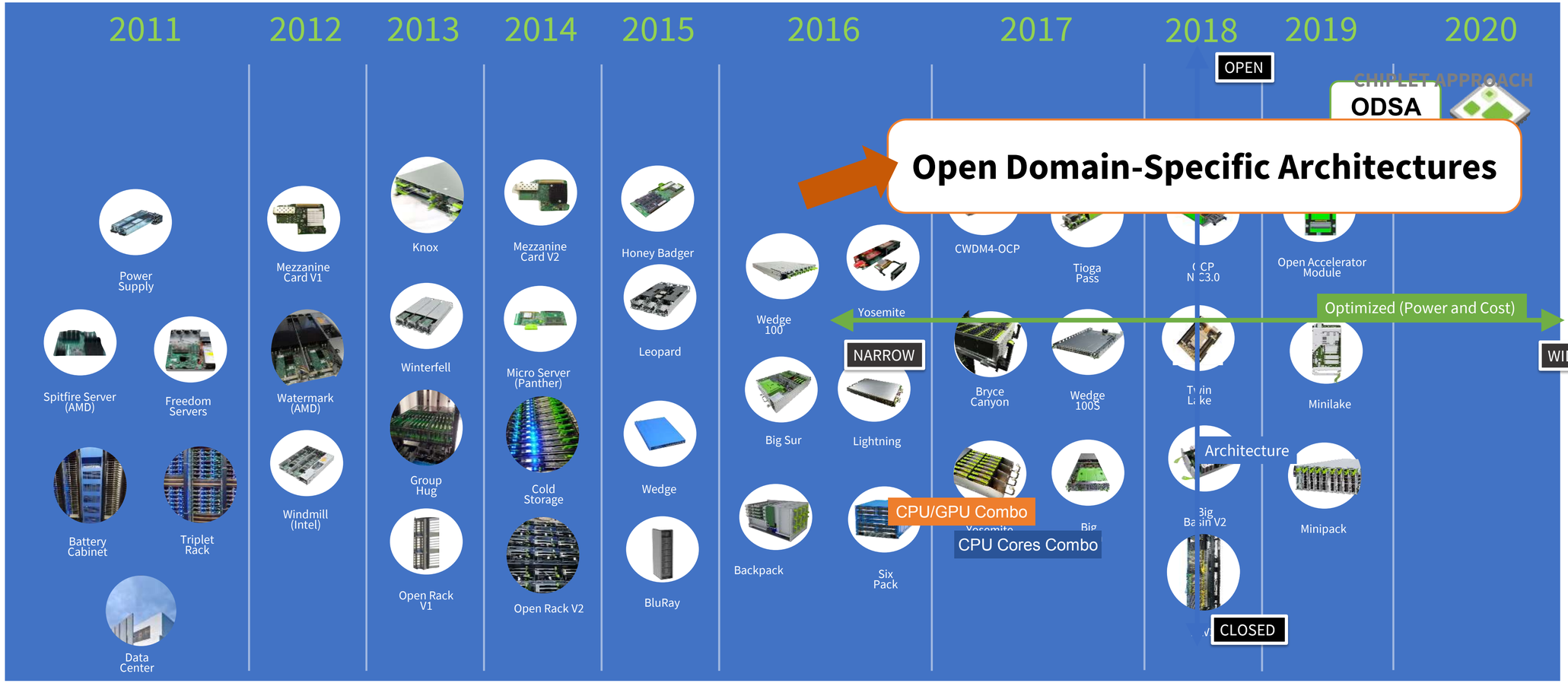
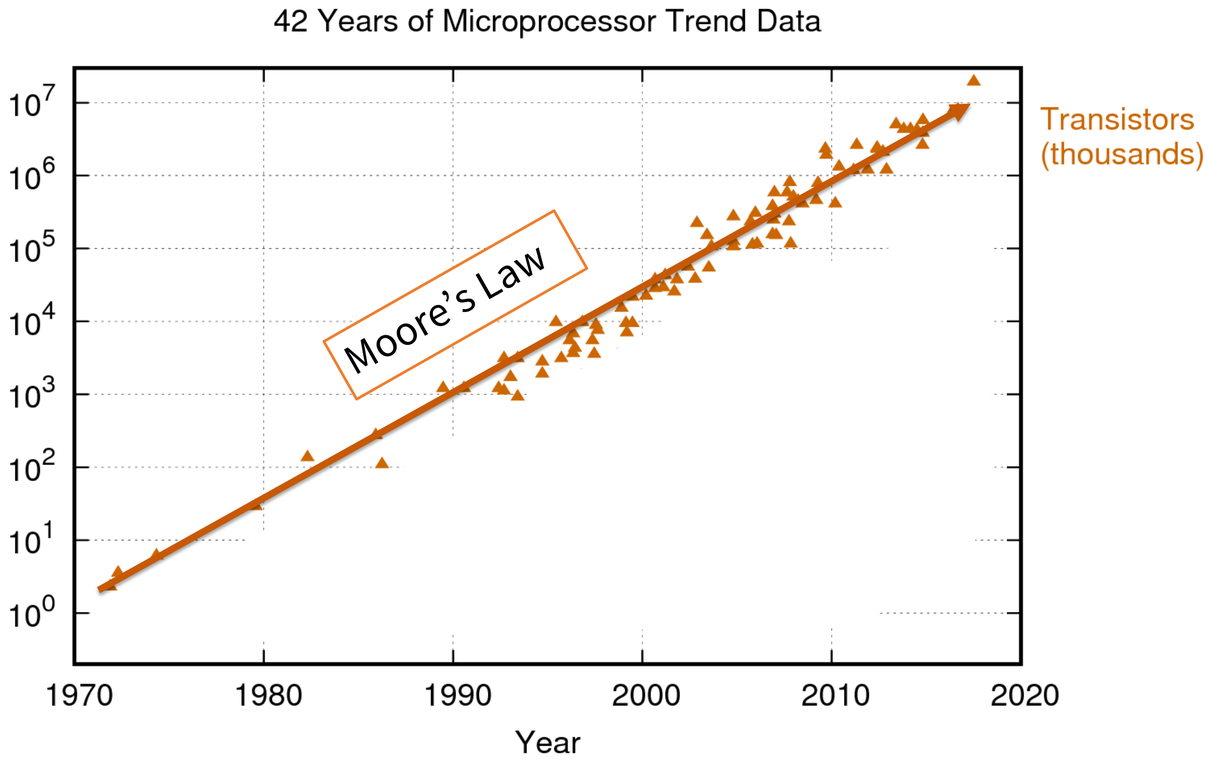


Start at the beginning…

Moore’s Law: A remarkable journey

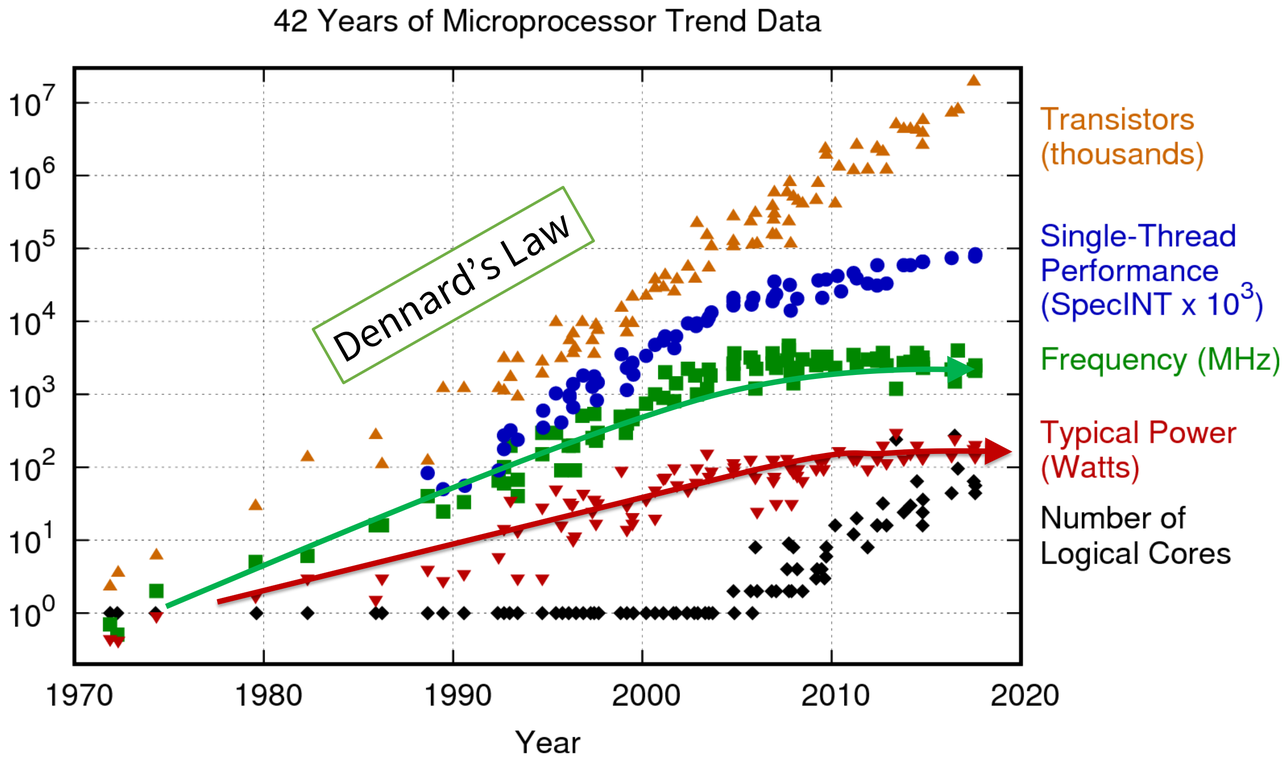


Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2017 by K. Rupp data source: https://goo.gl/bb6wZW

….remarkable journey is described by Moore’s Law, Intel co-founder Gordon Moore’s 1967 prediction that the number of transistors we can pack into a microchip would double every 18-24 months.

50 years of exponential growth!!

All exponentials must end…



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"…the nature of exponentials is that you push them out and eventually disaster happens"

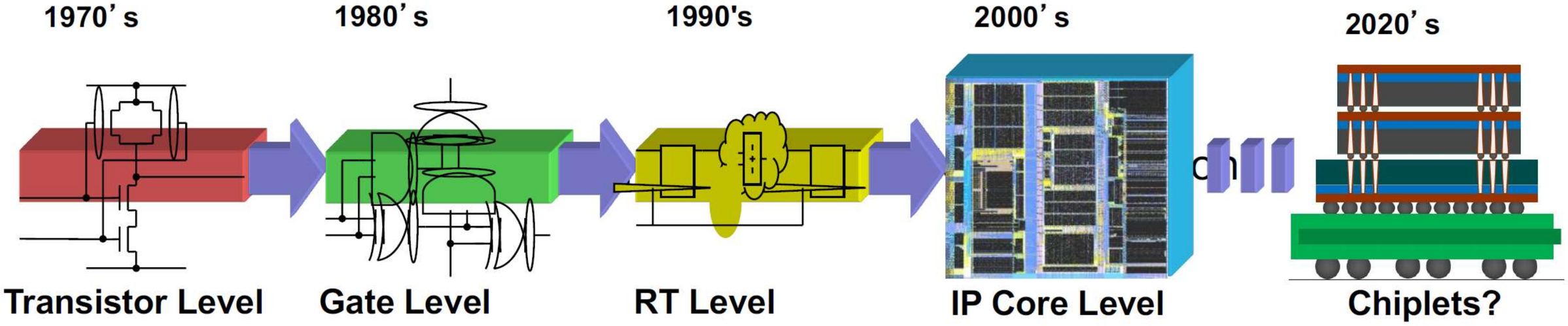
Some end sooner than others…Dennard's Law that says as transistors shrink, they get faster, use less power and get cheaper…ended about 10 years back!

Motivation

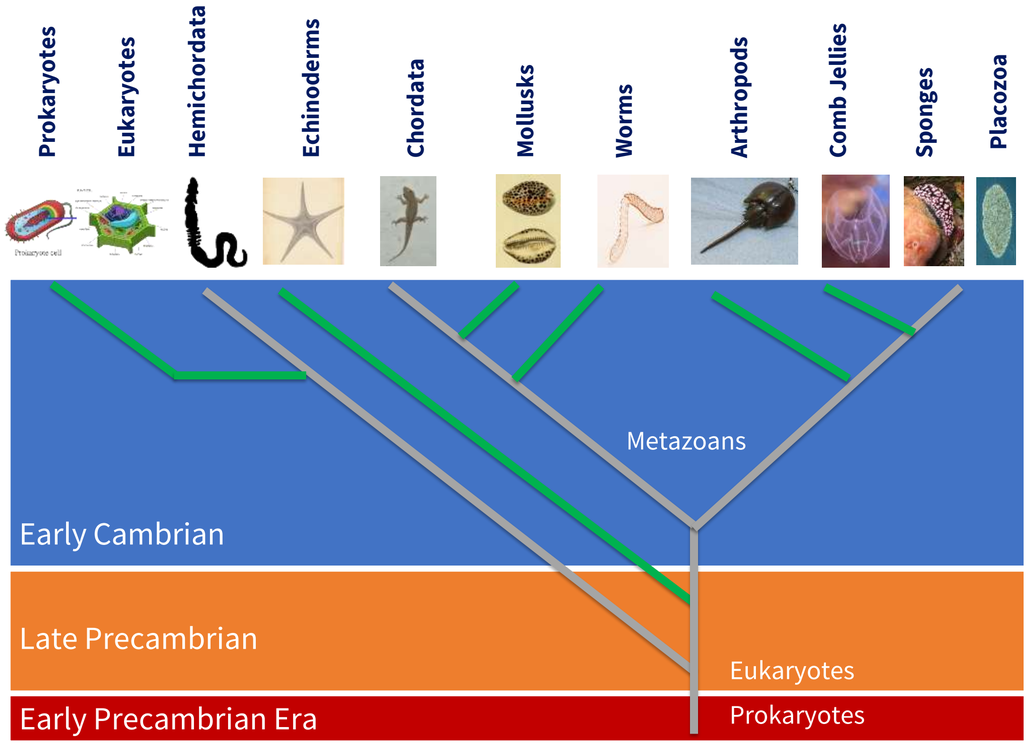
Gordon Moore also said…

“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.”

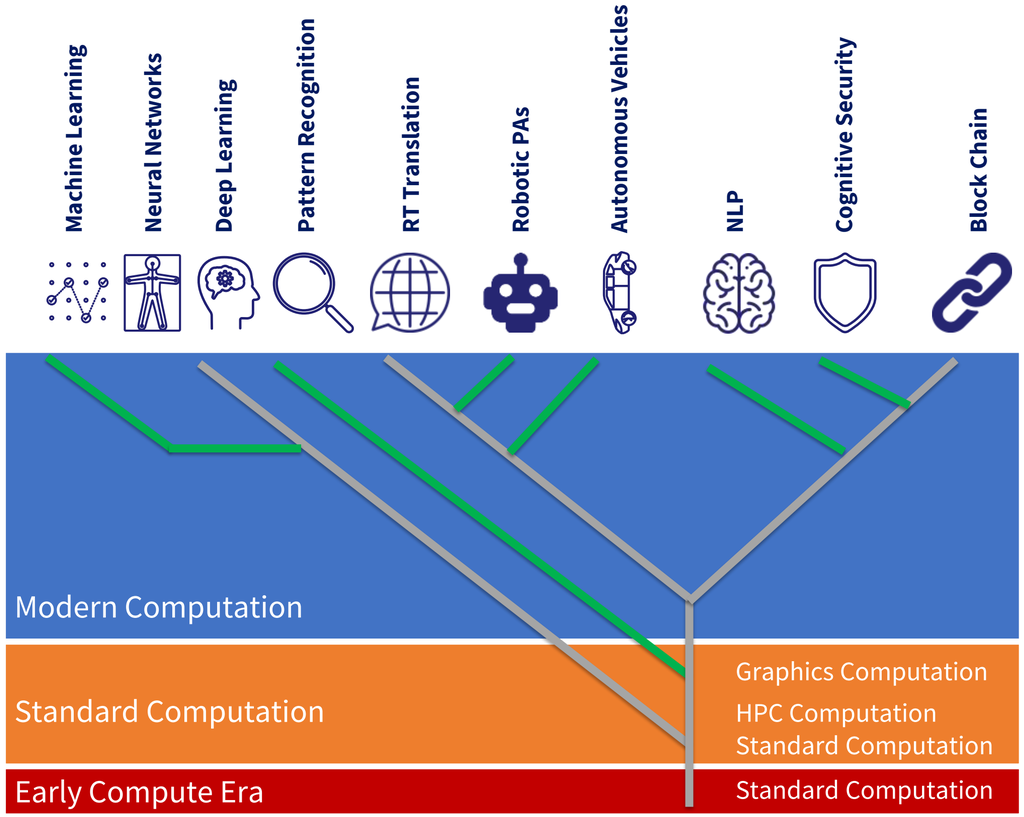
Electronics, volume 38, number 8, April 19, 1965



Cambrian Explosion of Workloads



Bio-Diversity Exploded from single cells into multi-cell organisms during the Cambrian explosion; all major phylla were established in this transition

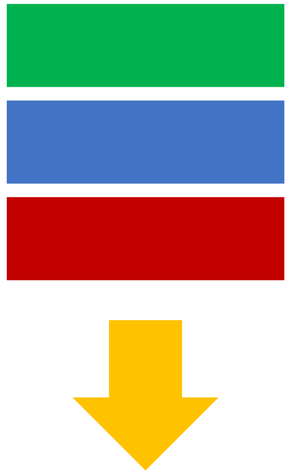


AI and Machine-learning and data-heavy workloads have exploded in past 5 years and will diversify as new applications are discovered constantly…

All images from Creative Commons

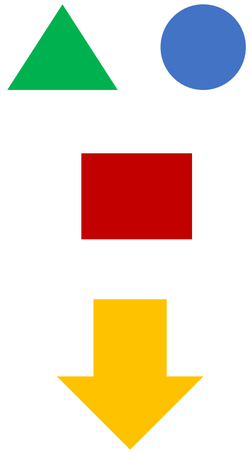
Domain-Specific Architectures

Logic Disaggregation



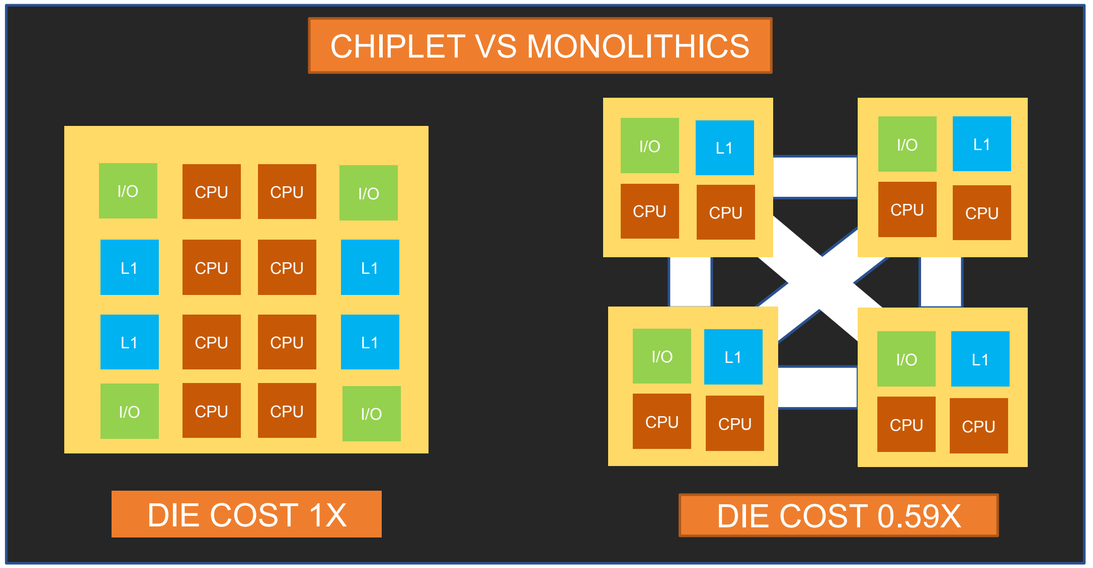
Improve yield and simplify/relax design requirements

IO Disaggregation



Right functionality in right silicon node

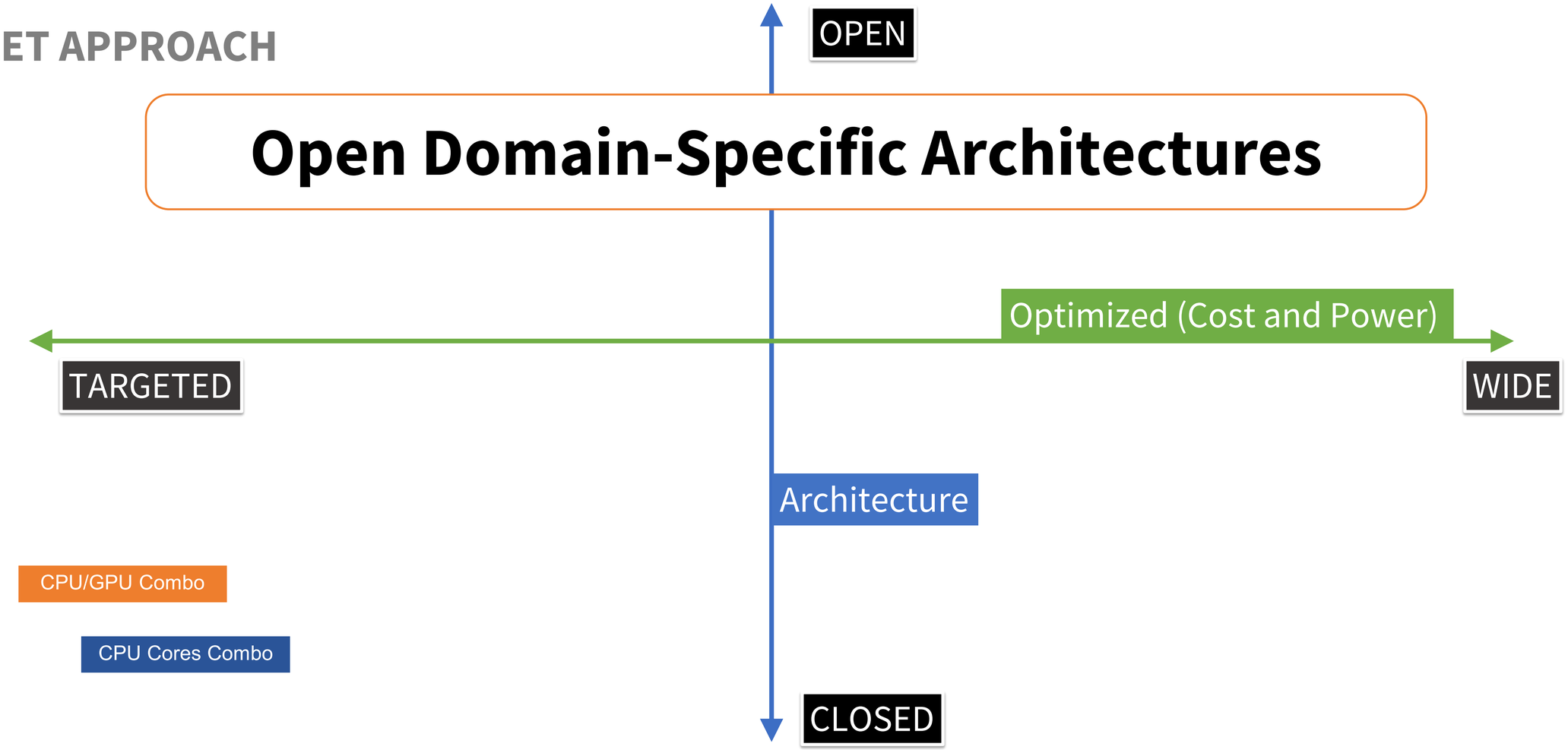
PROVEN EXISTING BUSINESS MODELS



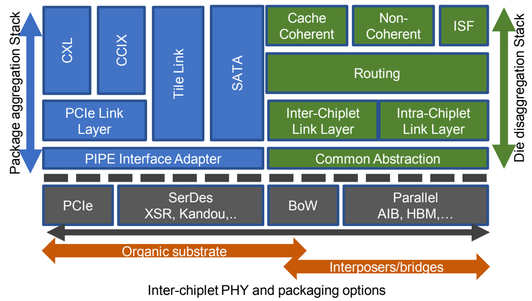
[L. Su, IEDM'17]

Open Domain-Specific Architecture (ODSA)

CHIPLET APPROACH

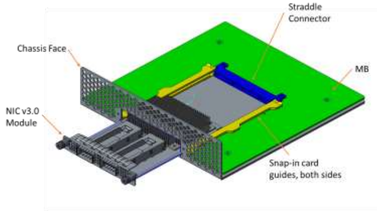


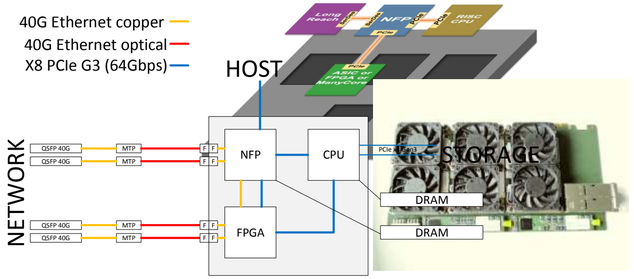
ODSA Goal: Chiplet Marketplace

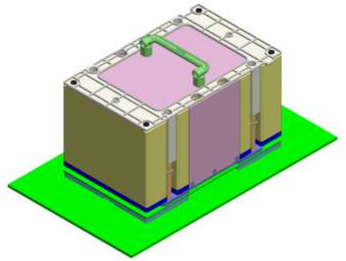


Inter-chiplet PHY and packaging options

Multi-technology
ODSA stack

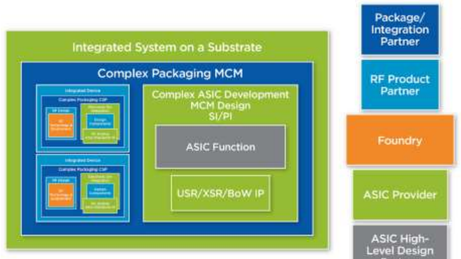






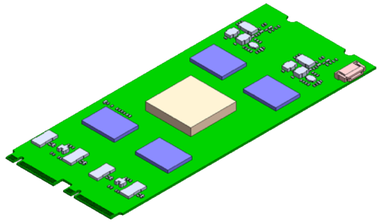
Chiplet
Marketplace

Reference architectures for:
Networking,
Storage,
Inferencing,
Training,
Video and Image processing



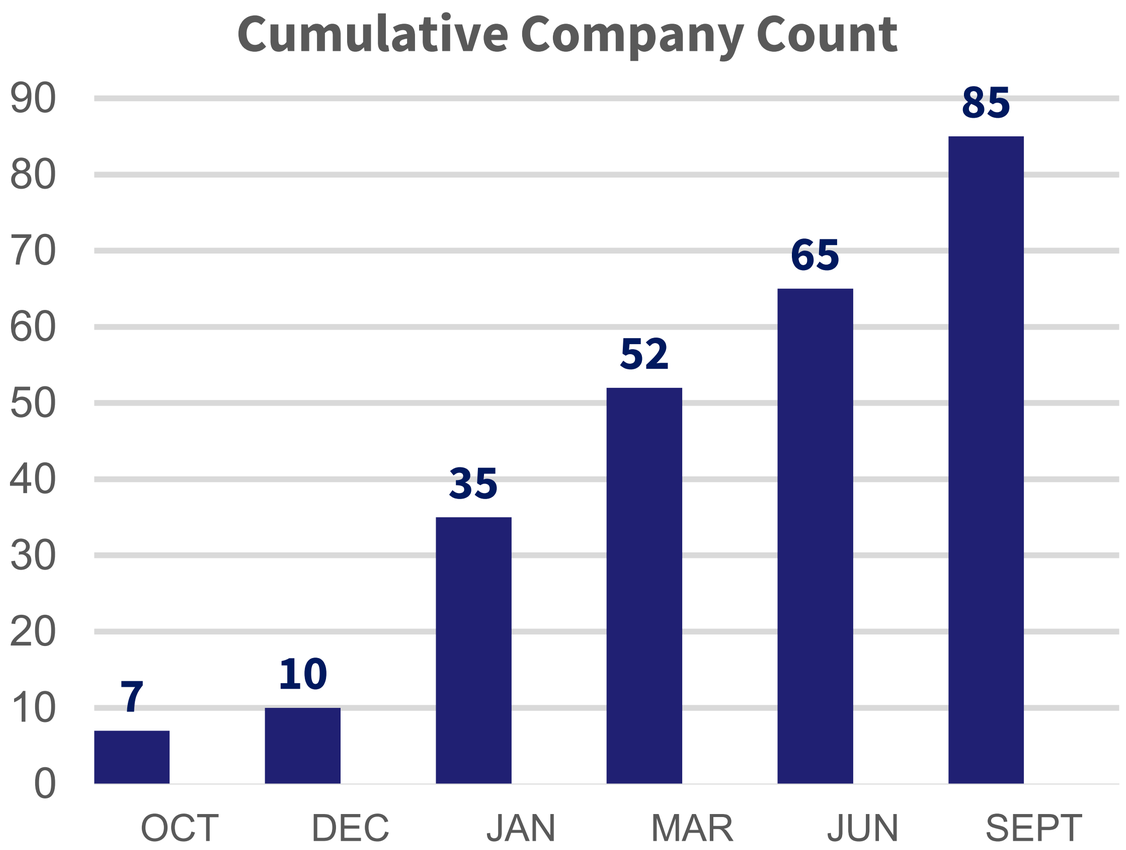
Business, Tools
Workflow to assemble
Product

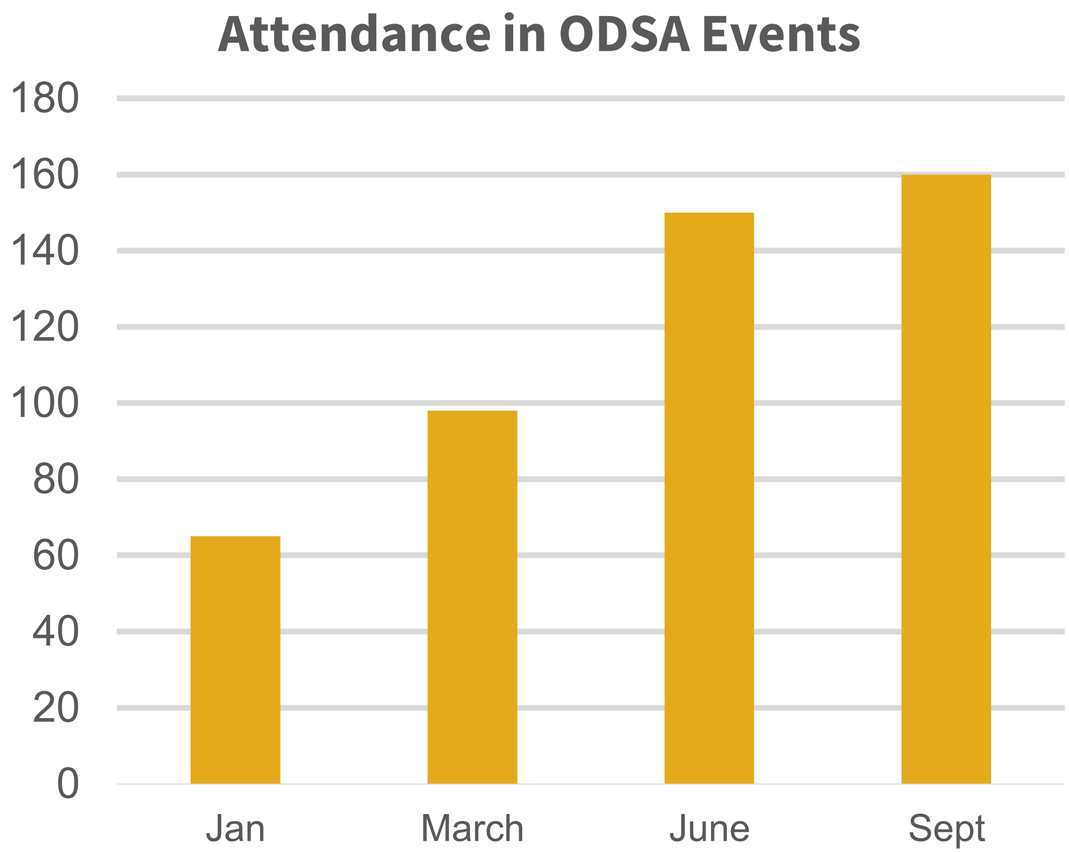
ODSA Activities



OCP Form Factors drive Power,I/O Footprint, Performance

Growth of ODSA





Source: OCP ODSA Survey

ODSA: A New Server Sub-Project

Extending Moore's Law:

- Domain-Specific Architectures: Programmable ASICs to accelerate high-intensity workloads (e.g. Tensorflow, Network Flow Processor, Antminer…
- Chiplets: Build complex ASICs from multiple die, instead of as monolithic devices, to reduce development time/costs and manufacturing costs.

Open Domain-Specific Architecture: An architecture to build domain-specific products

- Today: All multi-chiplet products are based on proprietary interfaces
- Tomorrow: Select best-of-breed chiplets from multiple vendors
- Incubating a new group, to define a new open interface, build a PoC

The Tip of the Spear “Opportunity”

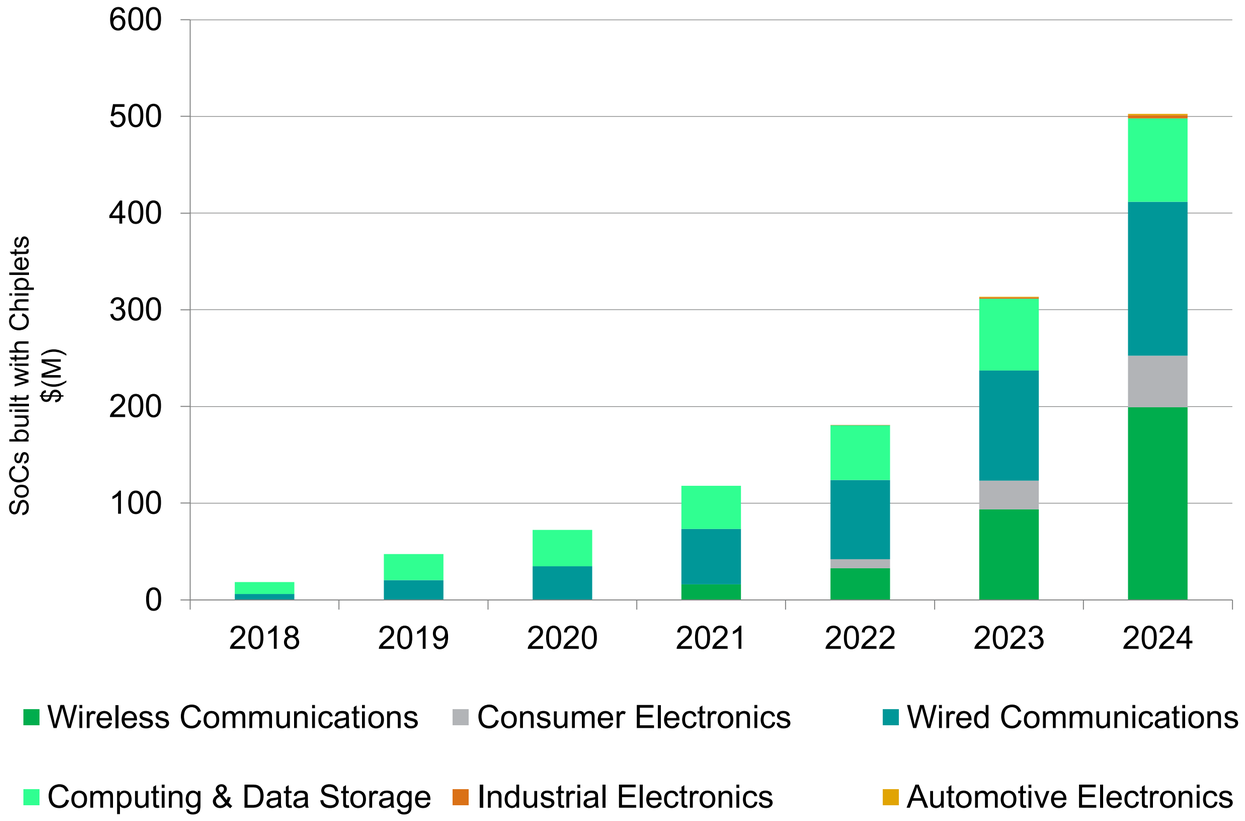
Independent research from IHS Markit

Four use cases for chiplets
SoCs
MPU
GPU
PLDs

Six Verticals (wireless, wireline, consumer, computing, industrial, automotive)

SoCs shown on the right. Immediate opportunity for an open interface – the tip of the spear.

SoC SAM by Market Segment



Excludes embedded x86 MPUs marketed as SoCs. Includes Configurable SoCs from PLD Vendors.
Source: IHS Markit

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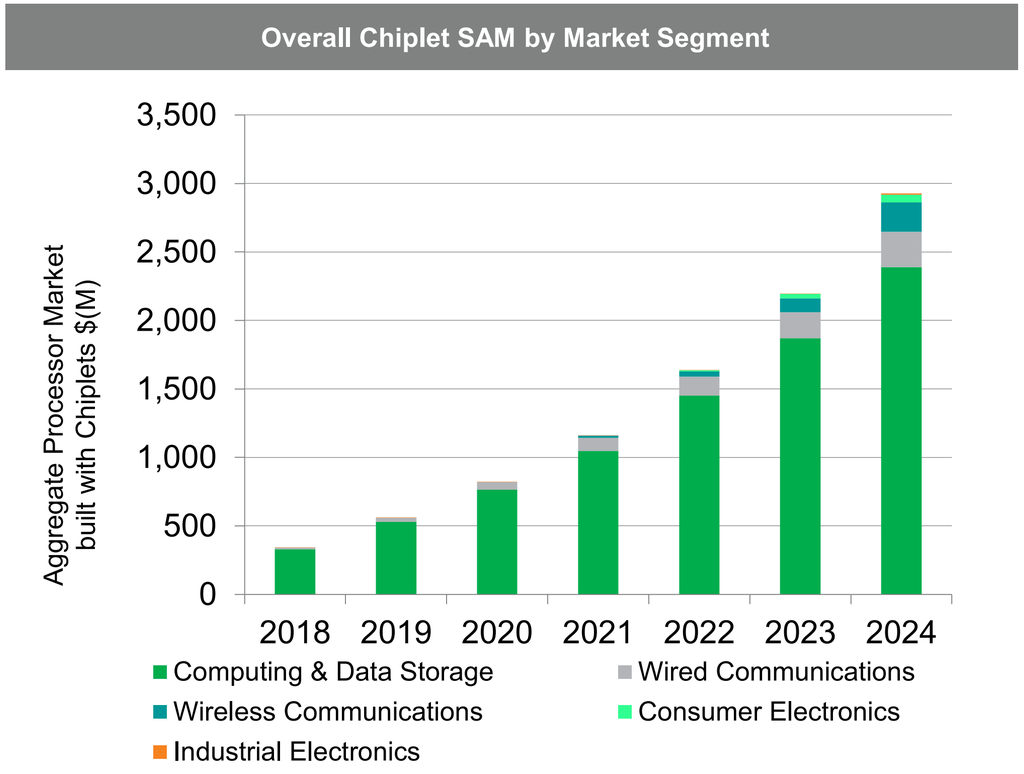
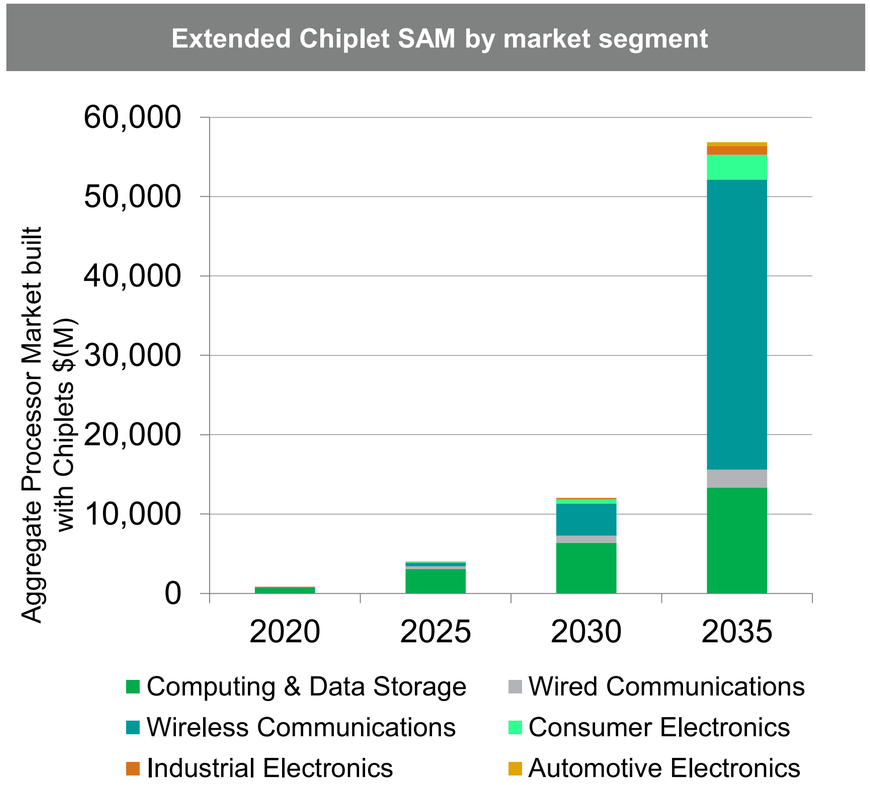
The End Game



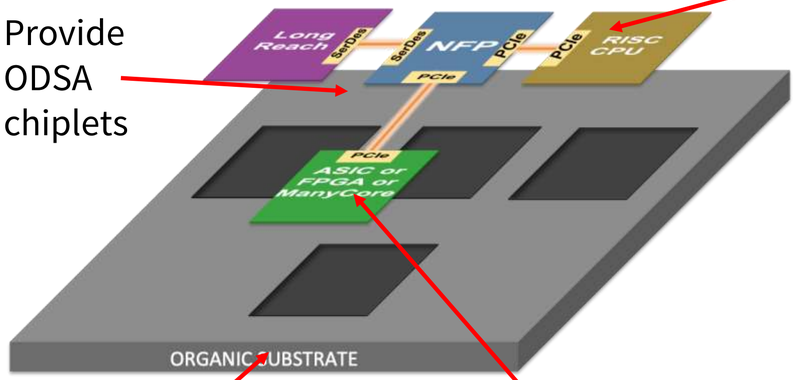


An open interface has a huge opportunity

Initially dominated by compute uses case, other market segments grow to dominate

Please Help! Join a Workstream

Join the PoC, Build fast:
(Quinn Jacobson/Jawad Nasrullah/ Jayaprakash Balachandran)



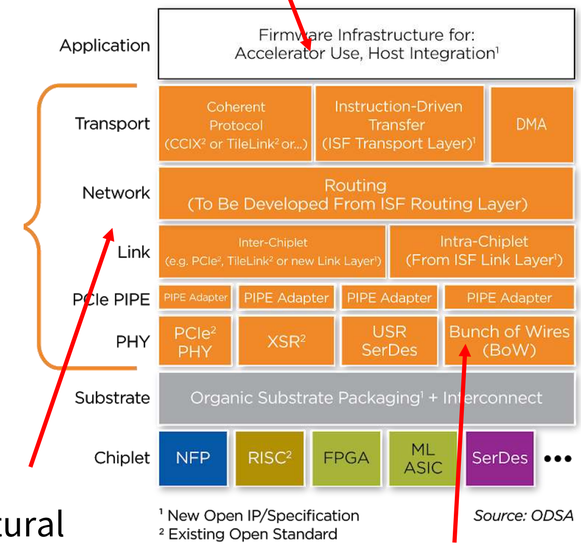
Provide ODSA chiplets

Develop Packaging + Socket, Dev Board

Provide FPGA IP

Join Interface/Standards:
(Mark Kuemerle/Ramin Farjad/ Robert Wang/David Kehlet)

Develop software

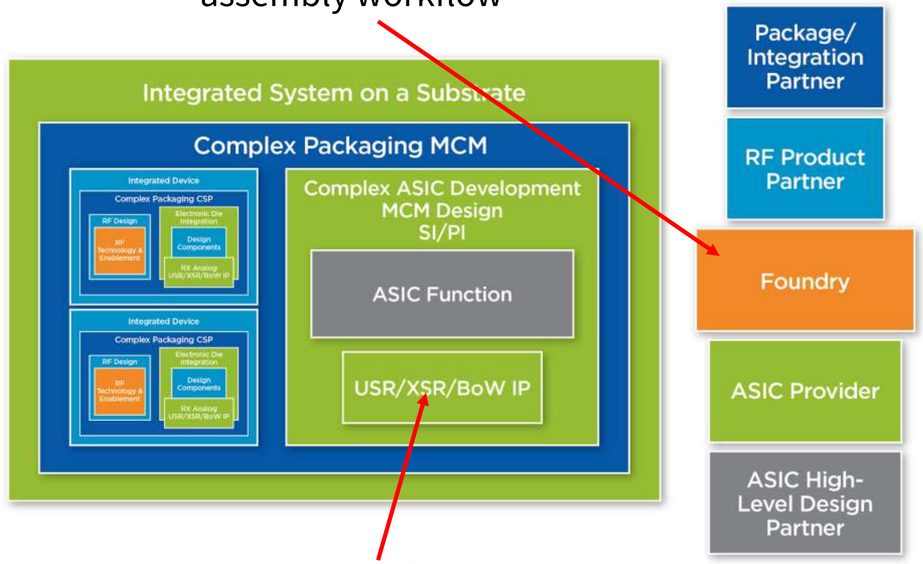


Define Architectural Interface

Provide PHY technology

Join Business, IP and workflow:
(Sam Fuller/Dharmesh Jani)

Define test and assembly workflow



Provide Chiplet IP

Workstream contact information at the ODSA wiki

Active Projects

Project	Objective	Organizations Participating	Recent Results	Upcoming Milestones	Needs
PHY Analysis	PHY requirements PHY analysis Cross-PHY abstraction (PIPE)	Alphawave, AnalogX, Aquantia, Avera Semi, Facebook, Intel, Kandou, Netronome, zGlue,	PHY Analysis paper (published at Hot Interconnect)	PIPE abstraction	
BoW Interface	No technology license fee, easy to port inter-chiplet interface spec	Aquantia, Avera Semi, Netronome	BoW Interface proposal (published at Hot Interconnect)	BoW specification 0.7 End September, 2019	Test chips, Chiplet library supporting interface
Prototype	product that integrates existing die from multiple companies into one package	Achronix, Cisco, Netronome, NXP, Samtec, Sarcina, zGlue, Macom, Facebook	Decomposable design flow.	Committed schedule	End user End user participation ~30% funding is open
Chiplet design exchange	Open chiplet physical description format.	Ayar, NXP, zGlue,	Draft spec	ZEF Exchange format draft specification	
Link and Network Layer	Interface and implementations – requirements and proposals	Achronix, Avera Semi, Intel, Netronome, NXP, Xilinx			
Multi-chiplet test	Test requirements for an open-chiplet interface				
Chiplet monitoring	Monitoring infrastructure for chiplet operation				
Business workflow	Formalize learnings from prototype effort				

Engineers from:
Achronix, AnalogX, ASE, Avera Semi, Ayar, Cisco, Facebook, Ferric, Intel, Kandou, Macom, Marvel, Netronome, NXP, On Semi, Samtec, Sarcina, Synopsys, Xilinx, zGlue

Wiki: https://www.opencompute.org/wiki/Server/ODSA, meet Fridays at 8 AM Pacific Time.
Please join us.

IF YOU WANT TO GO FAST, GO ALONE
IF YOU WANT TO GO FAR, GO TOGETHER

AFRICAN PROVERB

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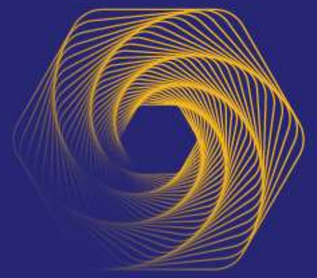
26–27, September, 2019