# DC-SCM 1.0 Reference Designs

## AMD Hawaii-V, Hawaii-H Cards w/Lanai PRoT Module

Ravi Bingi – Fellow, AMD <ravi.bingi@amd.com>
Greg Sellman – PMTS, AMD <gregory.sellman@amd.com>
Mahesh Prabhu – SMTS, AMD <Mahesh.prabhu@amd.com>

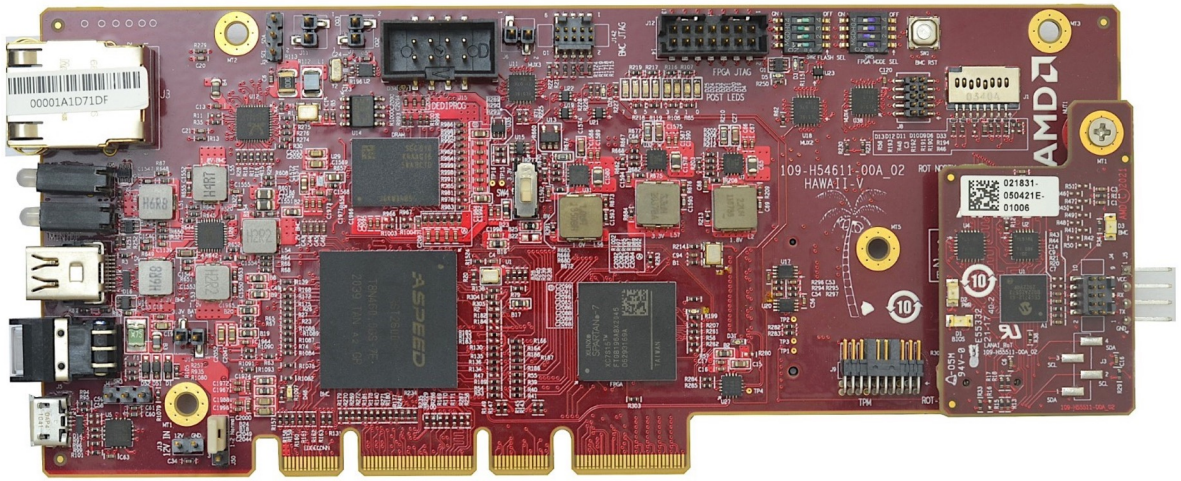
Connect. Collaborate. Accelerate.

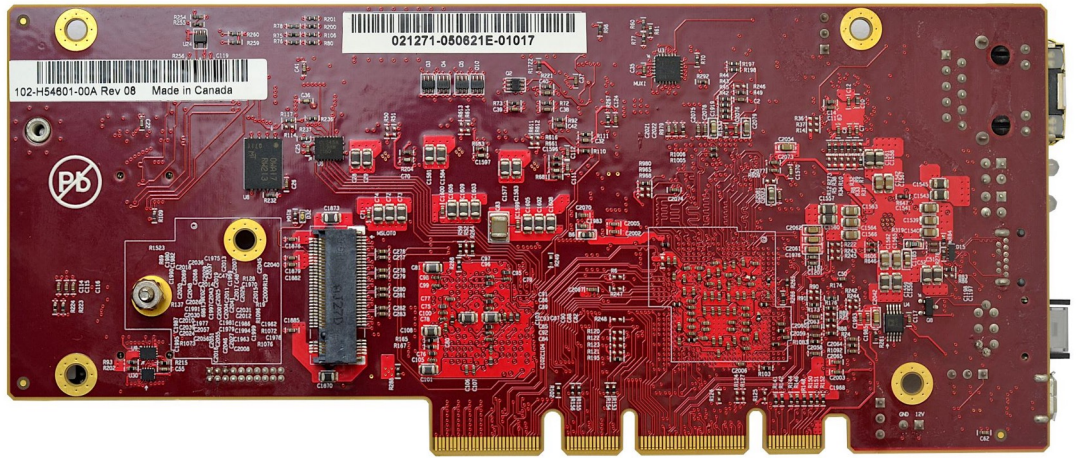
OPEN Compute Project®

# Outline

- Hawaii-V DC-SCM 1.0 Reference Design
- Hawaii-H DC-SCM 1.0 Reference Design
- Hawaii & Lanai Block Diagrams
- Hawaii-H & Hawaii-V Interface Details
- Hawaii & Lanai Reference Design Collateral
- Disclaimers

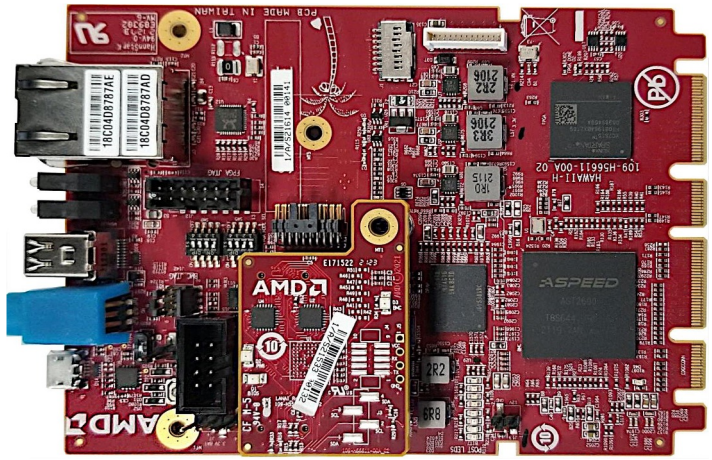
# "Hawaii-V" DC-SCM 1.0 Reference Design

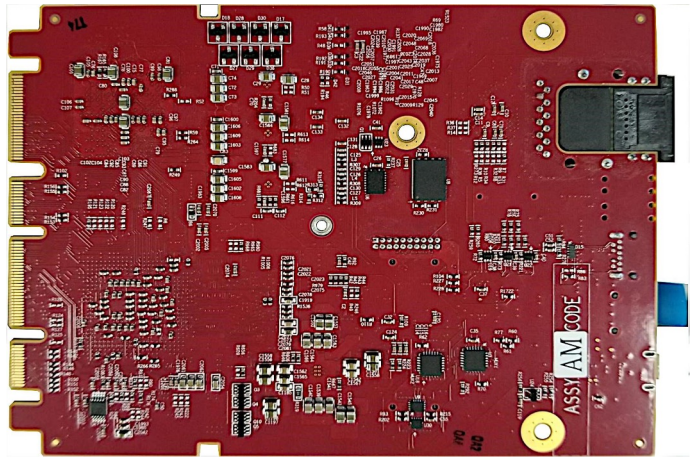



- Adheres to DC-SCM1.0 Vertical Form Factor (VFF1) Specification
- BMC subsystem based on ASPEED AST2600
- PRoT subsystem housed on a pluggable "Lanai" module
- Optional x4 PCIe M.2 Connector

# "Hawaii-H" DC-SCM 1.0 Reference Design

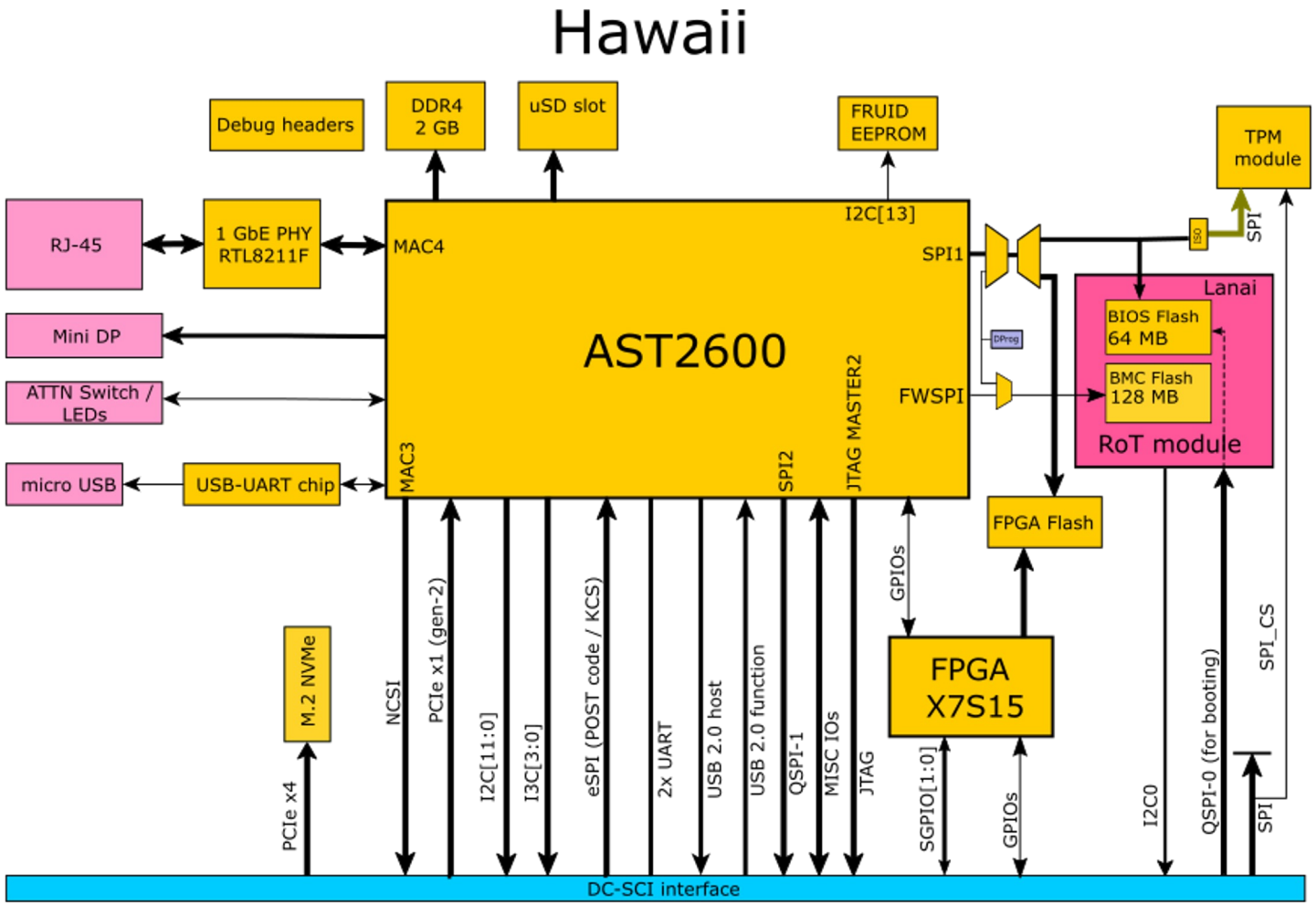


- Adheres to DC-SCM1.0 Horizontal Form Factor Specification
- BMC subsystem based on ASPEED AST2600
- PRoT subsystem housed on a pluggable "Lanai" module
- Optional x4 PCIe on DC-SCI interface not supported

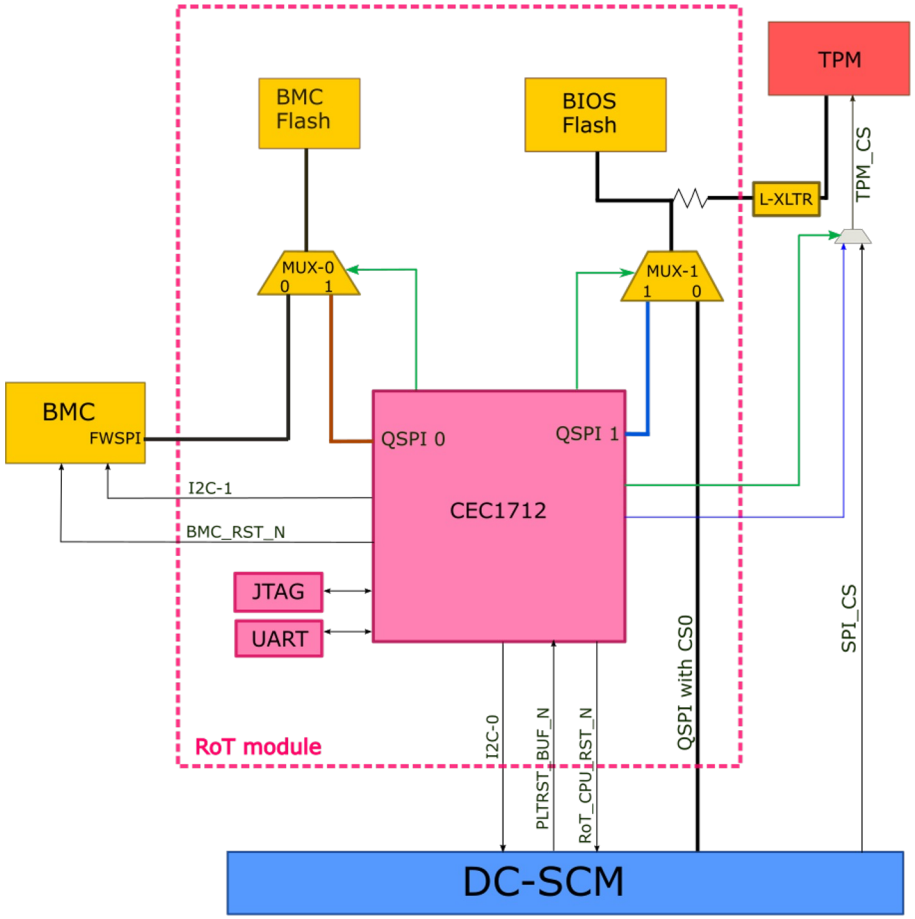
# "Hawaii" Block Diagram

- Adheres to DC-SCM 1.0 spec
- ASpeed AST-2600 BMC Subsystem
- Lanai, Platform RoT Module
- Specs:
  - 1Gb management port
    - NCSI connection to motherboard LOM
  - 12x I²C + 4x I³C Ports
  - SGPIO via XILINX Spartan7 FPGA
  - Remote FW update capability
  - KVM support over PCIe x1
  - Support for TPM
  - HW capability for BMC and Host FW authentication via

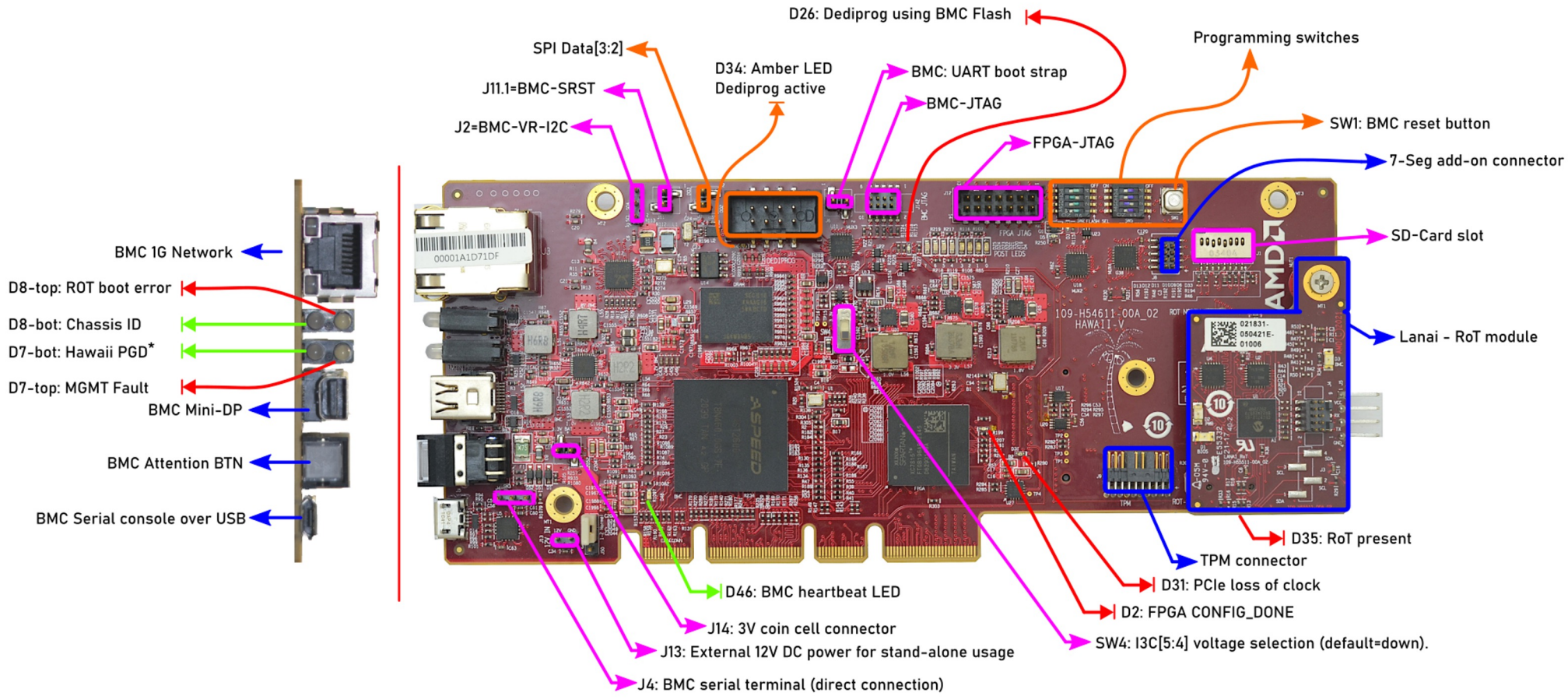


# "Lanai" Block Diagram

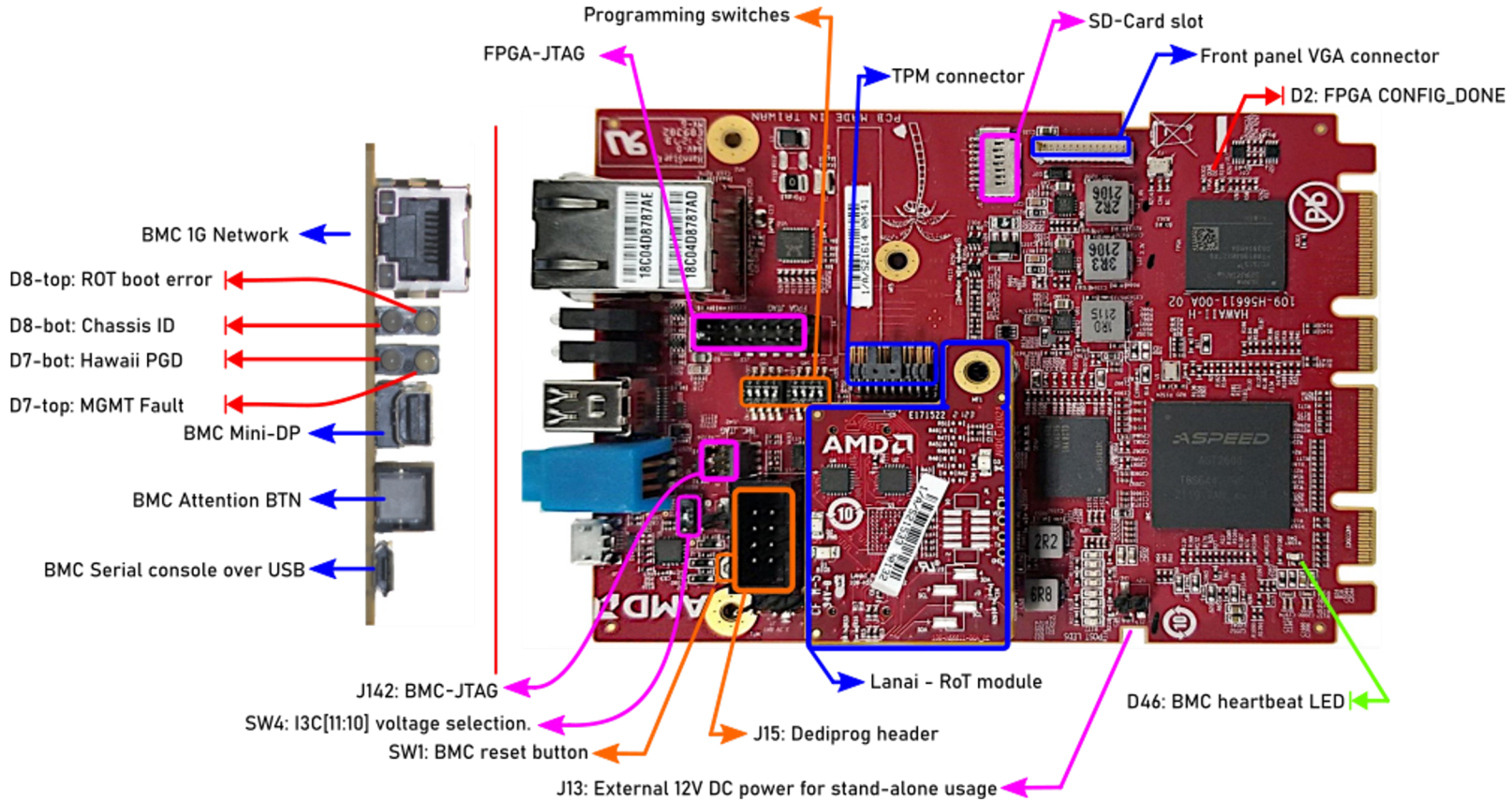
- Modular PRoT supports vendor independent implementation
- Contains BMC and Host BIOS flash ROMs
- Based on Microchip CEC1712 Secure Boot Controller
- Specs:
  - CEC1712
    - ARM Cortex-M4 CPU
    - Supports 2 code images in internal SPI flash
    - 1.8V or 3.3V operation, 84-pin WFBGA



# "Hawaii-V" Interface Details



# "Hawaii-H" Interface Details



# Hawaii & Lanai Design Collateral

| | Hawaii-V | Hawaii-H | Lanai |
|---|---|---|---|
| Schematic | Hawaii_V_database.zip | Hawaii_H_database.zip | Lanai_database.zip |
| BOM | Hawaii_V_BOM.xlsx | Hawaii_H_BOM.xlsx | Lanai_BOM.xlsx |
| Layout | Hawaii_V_brd.zip<br>Hawaii_V_gerbers.zip | Hawaii_H_brd.zip<br>Hawaii_H_gerbers.zip | Lanai_brd.zip<br>Lanai_gerbers.zip |
| Mechanical | Hawaii_V_STEP.zip | Hawaii_H_STEP.zip | Lanai _STEP.zip |
| FPGA firmware | Hawaii_FPGA_0p54_OCP.xpr.zip | | |
| BMC firmware | https://github.com/openbmc/openbmc | | |

# Disclaimers

The information contained herein is for informational purposes only, and is subject to change without notice. While every precaution has been taken in the preparation of this document, it may contain technical inaccuracies, omissions and typographical errors, and AMD is under no obligation to update or otherwise correct this information. Advanced Micro Devices, Inc. makes no representations or warranties with respect to the accuracy or completeness of the contents of this document, and assumes no liability of any kind, including the implied warranties of noninfringement, merchantability or fitness for particular purposes, with respect to the operation or use of AMD hardware, software or other products described herein. No license, including implied or arising by estoppel, to any intellectual property rights is granted by this document. Terms and limitations applicable to the purchase or use of AMD's products are as set forth in a signed agreement between the parties or in AMD's Standard Terms and Conditions of Sale.