BoW: A Die-to-Die Interface Solutions Specification Update

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High-level Targets for a Inter-Die Connectivity IP in MCM Packages

• Performance Targets:
  – Throughput Efficiency: ~1Tbps/mm (die edge)
  – Energy Efficiency: 1pJ/bit - 0.5pJ/bit

• Small silicon area per IO port for dense integration
  – Goal: IP silicon area not to limit IO density

• Minimal analog/complex circuitry to offer easy/fast process porting
  – Limit the maximum baud rate of the interface: ~10G-16Gbaud
  – Common clock to replace CDR with DLL, Digital PLL to generate clock, etc

• Single supply IP supporting wide Vdd range: 0.70V – 0.9V
  – To be compatible with most existing SoC/ASIC in popular/available process nodes

• Logical compatibility with AIB for ease of adoption
BoW (ODSA Proposal): Single-ended Signaling

- **BOW Base**
  - Unterminated lanes up to 5 Gbps/wire over 10m
  - Source Synchronous with clock alignment

- **BOW Fast**
  - Terminated lanes up to 16Gbps/wire over 50mm
  - DDR Source Synchronous with clock alignment

- **BOW Turbo**
  - Simultaneous Bidirectional in both directions
  - Terminated up to 2x16Gbps/wire= 32Gbps/wire over 50mm
  - Source Synchronous with clock alignment

Note: Baud rate limited to 16Gbaud for simplicity of design and ease of port
Top Level View: Bow Backward Compatibility

- A Bow-Fast can be configurable to be backward compatible to Bow-Base
  - By disconnecting the line terminations
- A Bow-Turbo can be configurable to be backward compatible to Bow-Base/Fast
  - Bow-Fast: By disabling Tx or Rx per lane
  - Bow-Base: By disabling Tx or Rx per lane and disconnecting terminations
BoW Slice (Building Block) Bump Map

- A common bump ordering to be used for BoW Slice Base/Fast/Turbo

- BoW Slice: 16 Data + 2 Clock ports
  - Configurable to be output clock or input clock pads when connected to non-Turbo Slices

- Vertical stacking of Bow Slices increases throughput per die edge

- BoW Slice Maximum Throughput
  - BoW Base: 16x4Gbps/pad = 64Gbps
  - BoW Fast: 16x16Gbps/pad= 256Gbps
  - BoW Turbo: 16x2x16Gbps/pad=512Gbps

- BoW Slice with same circuitry/layout but different RDL comes in 2 bump maps to create efficiency in building larger BoW modules
BoW 3-Deep Module Bump Map

- Stacking 3 (three) BoW Slices provides 48 data pads, with following throughputs:
  - **BoW Base**: 64x4Gbps/pad = 192Gbps Throughput/mm = ~164Gbps/mm
  - **BoW Fast**: 64x16Gbps/pad = 768Gbps Throughput/mm = ~656Gbps/mm
  - **BoW Turbo**: 64x2x16Gbps/pad = 1540Gbps Throughput/mm = ~1.32Tbps/mm
- Needs a package with 3-2-3 stack-up

Chip edge = 1170um (Bump Pitch=130um)
# BoW Slice Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Single Supply Voltage</strong></td>
<td>0.70V-0.90V (+/-5%)</td>
</tr>
<tr>
<td><strong>Max Throughput/mm (Combined Tx+Rx)</strong></td>
<td>Base: 55Gbps, Fast: 220Gbps, Turbo: 438Gbps ← 1x Stacked</td>
</tr>
<tr>
<td></td>
<td>Base: 110Gbps, Fast: 438Gbps, Turbo: 875Gbps ← 2x Stacked</td>
</tr>
<tr>
<td></td>
<td>Base: 164Gbps, Fast: 656Gbps, Turbo: 1320Gbps ← 3x Stacked</td>
</tr>
<tr>
<td><strong>BoW Slice Dimensions (Bump Pitch=130um)</strong></td>
<td>Chip Edge: 1170um, Height:320um</td>
</tr>
<tr>
<td><strong>Energy Efficiency (14nm)</strong></td>
<td>&lt; 0.7pJ/bit</td>
</tr>
<tr>
<td><strong>Trace length</strong></td>
<td>Base: 10mm, Fast: 50mm, Turbo: 50mm</td>
</tr>
<tr>
<td><strong>Latency</strong></td>
<td>&lt; 30/Gbaud ( &lt;3ns @10Gbaud)</td>
</tr>
<tr>
<td><strong>Slice Bump Allocation (excludes global AUX)</strong></td>
<td>16 Data, 2 Clock, 1 Mode, 4 Ground, 4 Power</td>
</tr>
<tr>
<td><strong>BER Target</strong></td>
<td>&lt;1E-15 (No ECC)</td>
</tr>
<tr>
<td><strong>ESD / CDM protection</strong></td>
<td>400V/100V</td>
</tr>
</tbody>
</table>
BoW Compatibility with AIB

- From logical viewpoint, BoW to use similar Interface Signals as AIB, with following differences:
  - Master Interface to also be the timing Master
  - Sideband Controls limited to 32 registers for both Master and Slave
- AUX signals are not duplicated like AIB and are independently hardwired
- BoW to provide Dual mode Master and Slave option
- 16 bit bus vs. 20+ bit bus
SDR & DDR Clocking

SDR

- TX (single-rate)
- RX (single-rate)
- Clock
- data_out (single-rate)
- fs_fwd_clk
- Data (at output pad)
- Forwarded clock (at output pad)

DDR

- TX (double-rate)
- RX (double-rate)
- Clock
- data_out[0] (single-rate)
- data_out[1] (single-rate)
- fs_fwd_clk
- Data (at output pad)
- Forwarded clock (at output pad)
Receive SDR and DDR I/O Mapping

- Clock signal hs_clk is fed to BoW IO block from a clock generator (e.g. PLL)
- In Bow Basic mode, fwd_clk, hs_clk, and mac_clk all run at the same speed
- In BoW Fast and Turbo, fwd_clk and hs_clk run 4x faster than mac_clk
- Mux/Demux ratios will be different between BoW Basic (2:1/1:2) and Fast/Turbo (8:1/1:8)
Transmit SDR and DDR I/O Mapping

• Clock signal mac_clk is always sent from BoW IO block to the MAC block, regardless of the block being a receive or transmit IO
• Clock signal hs_clk is fed to BoW IO block from a clock generator (e.g. PLL)
**BoW Sideband Control Signals**

<table>
<thead>
<tr>
<th>Signal name</th>
<th>Signal function</th>
<th>Bits</th>
<th>Signal origin (far-side or MAC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ms_osc_transfer_en</td>
<td>Oscillator calibration complete</td>
<td>1</td>
<td>FS</td>
</tr>
<tr>
<td>sl_osc_transfer_en</td>
<td>TX DCC calibration complete</td>
<td>1</td>
<td>FS</td>
</tr>
<tr>
<td>ms_tx_dcc_cal_done</td>
<td>RX calibration complete</td>
<td>1</td>
<td>FS</td>
</tr>
<tr>
<td>sl_tx_dcc_cal_done</td>
<td>Start RX calibration</td>
<td>1</td>
<td>MAC</td>
</tr>
<tr>
<td>ms_rx_dcc_lock_req</td>
<td>RX DLL locked</td>
<td>1</td>
<td>FS</td>
</tr>
<tr>
<td>sl_rx_dcc_lock_req</td>
<td>TX calibration complete</td>
<td>1</td>
<td>FS</td>
</tr>
<tr>
<td>ms_tx_transfer_en</td>
<td>Start TX calibration</td>
<td>1</td>
<td>MAC</td>
</tr>
<tr>
<td>sl_tx_transfer_en</td>
<td></td>
<td></td>
<td></td>
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<td>ms_rx_dcc_lock_req</td>
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- BoW uses the same 7 fixed Sideband Controls as AIB, 16 external controls for both Master & Slave, and 9 Reserved controls

- Limit sideband clock to 200M-400MHz
  - Fewer controls bits relaxes clock frequency

- The functions of the fixed sideband controls are the same as AIB with same source:
  - Far-side (link-partner)
  - MAC (local)

<table>
<thead>
<tr>
<th>User Defined</th>
<th></th>
<th></th>
</tr>
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<tbody>
<tr>
<td>External Control</td>
<td>Defined by protocol or application</td>
<td>MS: 8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Other</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved</td>
<td>MS/SL:9</td>
</tr>
</tbody>
</table>
Test & Calibration Options

- 1149.1 Legacy/1149.6 High-speed (JTAG scan)
- IEEE 1500 (HBM type systems)

- At-Speed Self Test
  - Serial At-Speed PRBS Self Loopback: Tx(Port-N_Chiplet-A) to Rx(Port-N_Chiplet-A)
  - High-Coverage Wafer Test Screen (pre-package) loopback traces on ATE load board

- At-Speed System Test/Compliance
  - External PRBS Loopback: Tx(Port-N_Chiplet-A) to Rx(Port-M_Chiplet-B)
  - Eye Monitor for At-Speed Test/Compliance: Tx(Port-N_Chiplet-A) to Rx(Port-M_Chiplet-B)
    • Per data bump: Measure Errors Rate for each phase and voltage threshold

- Calibrations
  - PLL/DLL Lock
  - Rx Phase Lock
  - DCC Calibration (optional)
Summary

• Concept proven in 14nm Silicon (Hybrid easy to port to other nodes)
• Over 1Tbps/mm chip edge over 50mm organic substrate (pitch= 130um)
  • Full-duplex Throughput/bump up to 32Gbps (2x16Gbps)
• Small area per port of <0.02mm²
• Less than 0.7pJ/bit in 14nm (<0.5pJ/bit estimate in 7nm)
• Single power supply 0.7V-0.9V: Compatible with synthesized logic circuits
• Easy and quick to port into other process nodes (16G NRZ vs 112G PAM4)
• Backward compatibility
  • A Chiplet with Bow Turbo interoperates with other BoW interfaces
• High Wafer-level test coverage per Chiplet to improve final product yield
Target Specification Milestone

• We Are Targeting:
  • Spec Draft V0.5 by Hot Interconnect Workshop in August
  • Spec Draft V0.9 by next ODSA Workshop in September
  • Spec Draft V1.0 by ODSA Workshop in November
Why BoW Specification Makes Sense

- There are multiple versions of die-die interfaces being built by multiple companies today
  - Open standard makes sense to converge design points
- A common and simple parallel interface at relatively low data rate enables chips in older nodes to be integrated into the system
  - Example: Critical for RF component integration
- Master/Slave mode simplifies clock generation requirements
  - Also helpful for legacy technology implementations
- Expandability of the same pins in higher data rates with BoW Fast and Turbo allows for chiplets to meet multiple applications
  - Example: Streaming data with several RF chips
    Same die switching accelerator data with NIC, FPGA
How You Can Help

Seeking volunteer(s) for

• Foundries to support implementation of BoW PHY IP in their high-end process nodes (esp Finfet)

• Development of the BoW PHY IP in multiple process nodes (28nm to 7nm and even 5nm)
  – Availability of the BoW in wide range of process nodes will encourage larger and faster adoption

• Development of PHY Interface to different Standards and Protocols
  – BoW PHY needs a separate dedicated interface layer developed for each transmission standard having different coding and partitioning
    • Example: PCIe/CXL, Ethernet, etc
BACK UP
AQLink Demo Silicon in GF

LR: M1 ↔ S2  MR: M2 ↔ S1  SR: M3 ↔ S0

| 2mm | 10mm | 25mm |

2mm

10mm

25mm

traces on test chip
AQlink Internal Eye for Bidirectional 28Gbps (>1E11 bits per point)

2mm: SR Channel

10mm: MR Channel

25mm: LR Channel