RunBMC
The Hardware Interface for BMC

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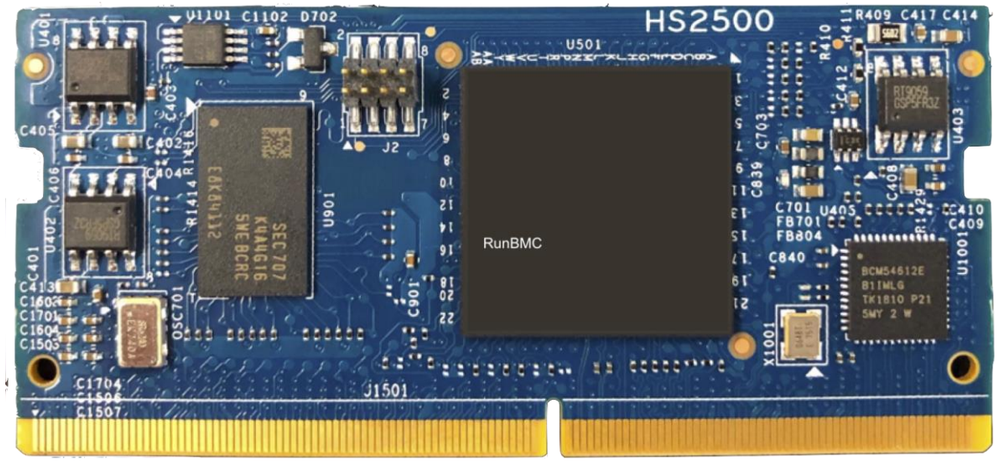
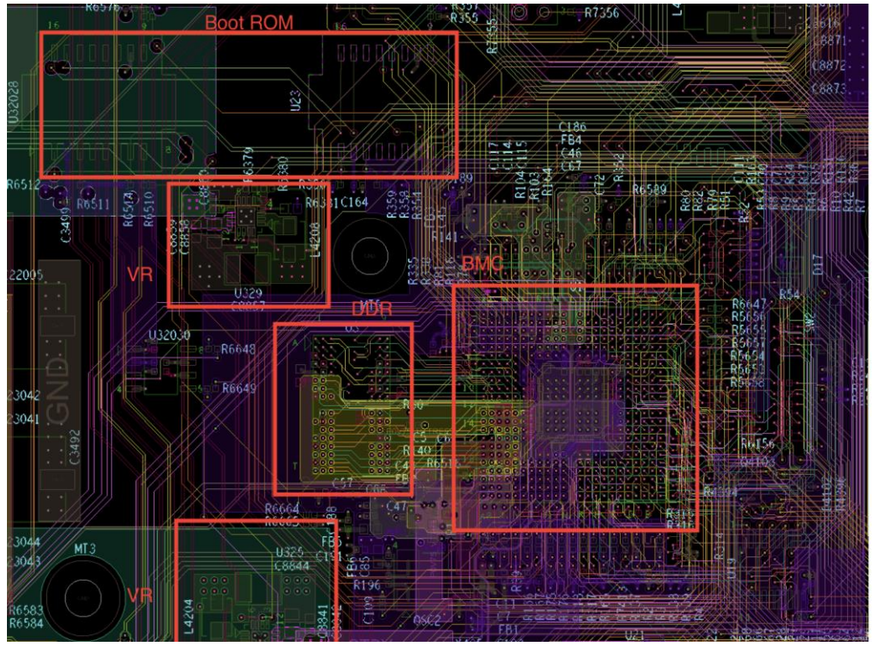
Overview

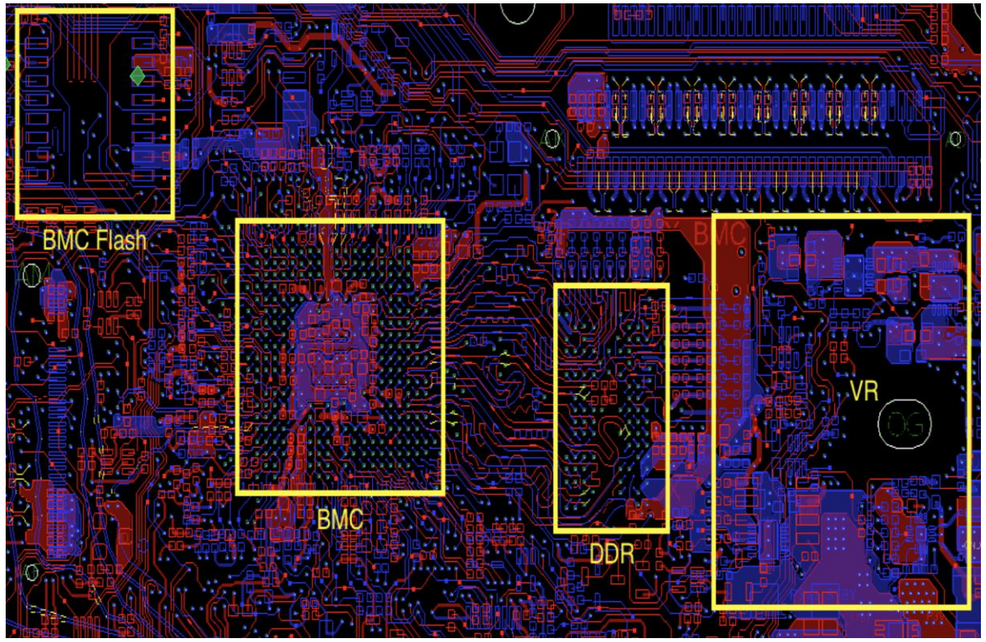
- “RunBMC specification defines the interface between the Baseboard Management Controller(BMC) subsystem and OCP hardware platforms, such as network or compute motherboards.”



Platform Analysis

2018-2019: In-depth analysis of currently available OCP server platforms to compare BMC implementations

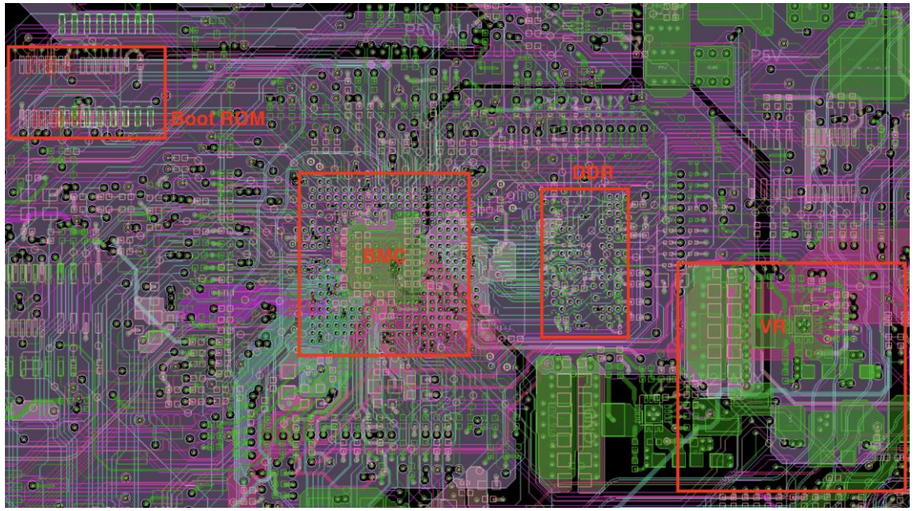




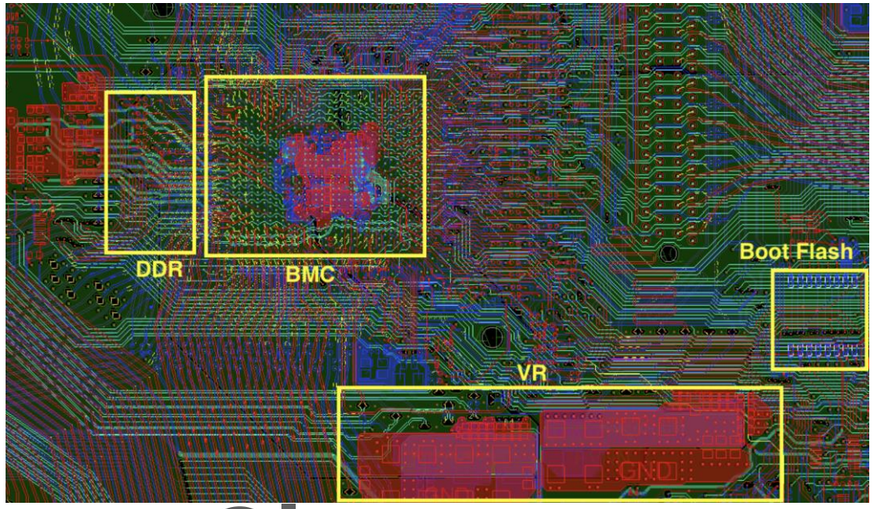
- **Wedge (100G switch)**
  - Standard DDR3 layout, redesigned
  - Unique voltage regulation for BMC
  - Boot ROM reused
  - Uses SGMII for BMC network

- **Tioga Pass**
  - Standard DDR4 chip, custom layout
  - Unique voltage regulation for BMC
  - Placement requirement for Flash (may be a crowded design)
  - Routing RMII to Intel I210 (not shown)

Platform Analysis….Cont’d



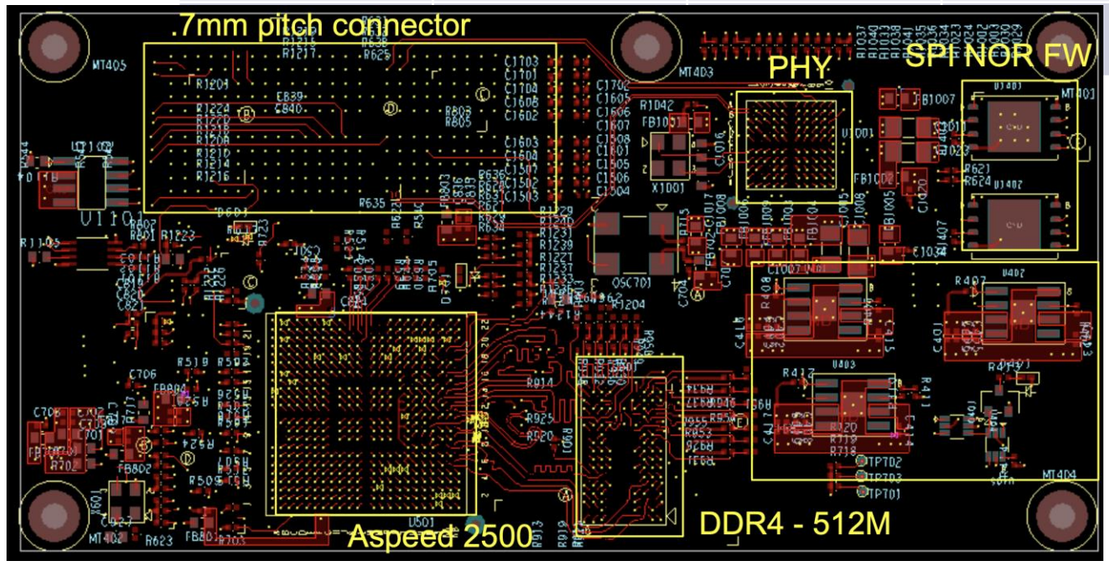
- **Zaius**
  - DDR4 layout effort
  - Unique voltage regulation for BMC
  - RGMII to PHY (for dedicated BMC connection)



- **Olympus**
  - DDR3 layout effort
  - Same design as Wedge with minimal changes
  - RGMII to PHY (for dedicated BMC connection)

Platform Analysis Summary & prototype

	GPIO (Resets etc..)	IRQ or Error	Total (GPIO/IRQ/others)	I2C (busses)	UART
Tioga Pass	58	32	103	13	3
Zaius	71	20	98	15	1
				10	2

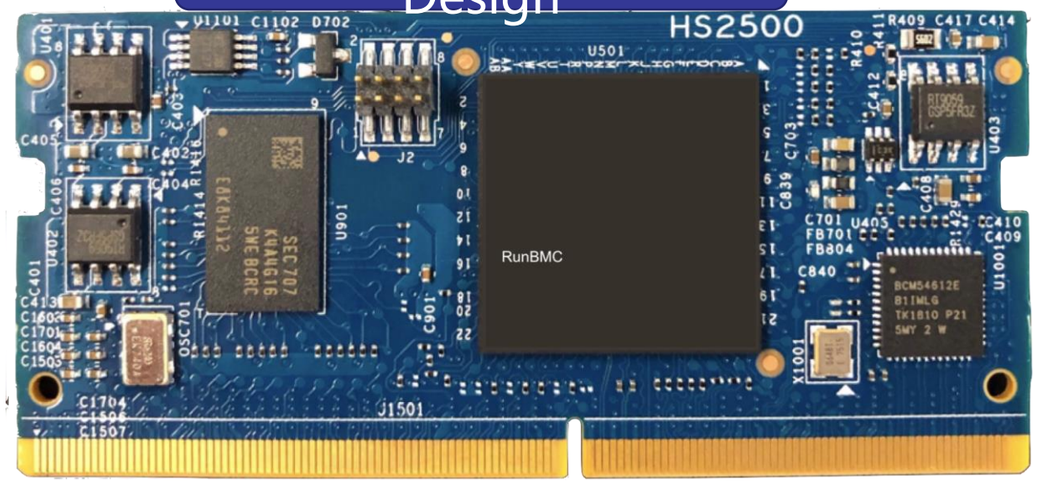


- **RunBMC 2018 Prototype**
  - 300 Pins
  - Board to Board Connector
  - Specification ??

Fast Forward to 2019

- RunBMC specification & more collaboration
- More reference boards & more prototypes

AST2500 Reference Design



- **SOC**: ASPEED AST2500 SOC
  - ARM11 32-bit, 800Mhz
- **SPI**: 2x 32MB
- **DDR4**: 512MB
- **PHY**: 1GbT, BCM54612e

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Nuvoton Poleg reference design

- **SOC**: Nuvoton Poleg SOC
  - Dual Cortex A9 32-bit, 800Mhz
- **SPI**: 2x 64MB
- **eMCC**: 8GB or None (Two SKUs)
- **DDR4**: 1GB
- **PHY**: 1GbT

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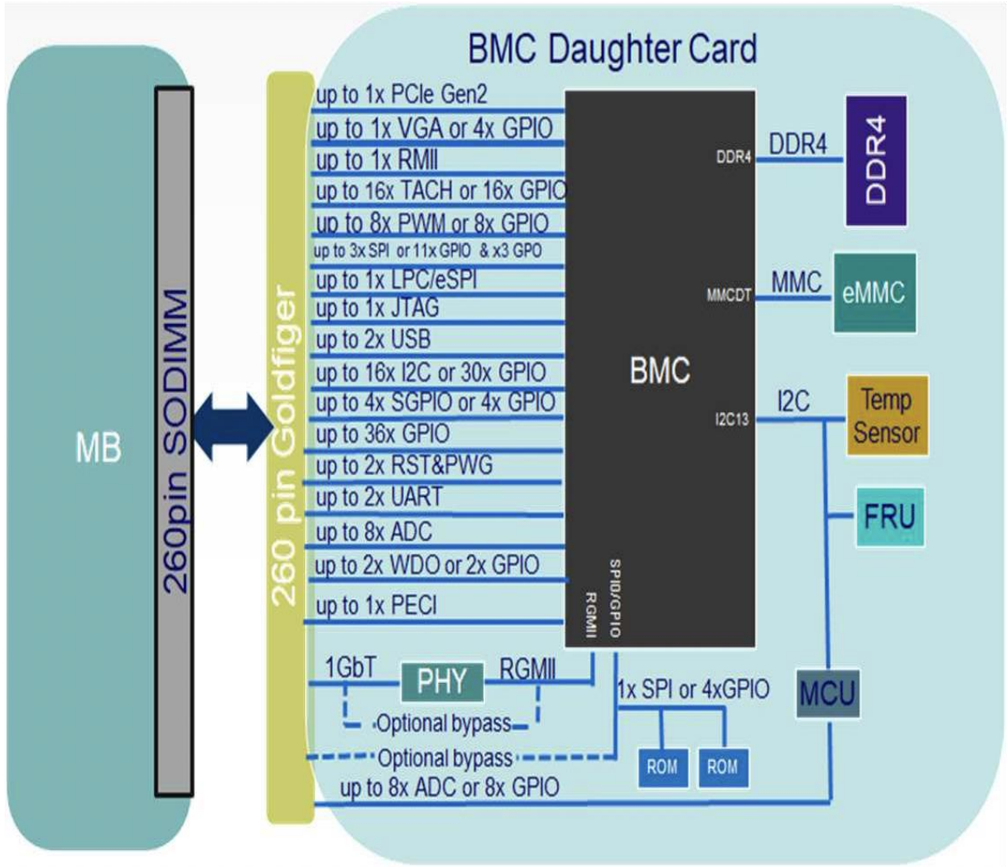
High Level Spec

Overview	
Overview	RunBMC specification defines the interface between the Baseboard Management Controller(BMC) subsystem and OCP hardware platforms
Connector and Form Factor	
Connector/ FF	260pin DDR4 SO-DIMM Connector. MO-310C JEDEC registration in two different heights. Standard (32mm) and Large (50mm) allowed. Right Angle and Vertical Supported
I/O Connectivity	
I/O	1x PCIe Gen2, 1x VGA, 1xRMII, 16x TACH, 8x PWM, 3x SPI, 1x LPC/ESPI, 1x JTAG, 2x USB, 16x I2C, 4x SGPIO, 36x GPIO, 2x RST/PWRGD, 2x UART, 8x ADC, 2x WDO, 1x PECI, 1GbT/RGMII, 8x ADC
Flexible Functionality	
Flexible	Dual Functions for majority of the I/O is supported via multiplexing. Provides system flexibility



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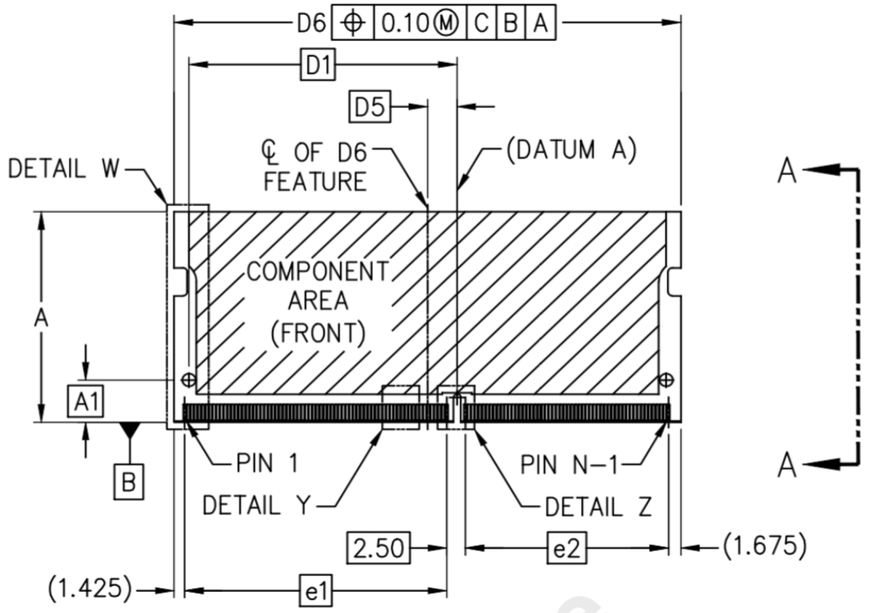
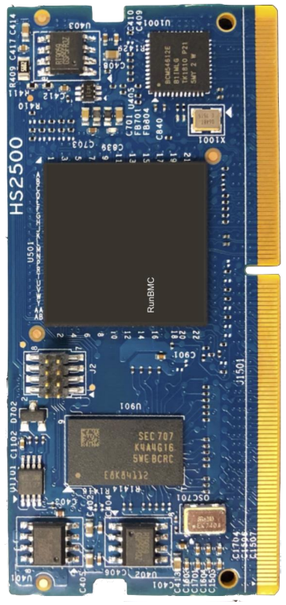
Mechanical Form Factor

- **Connector**
  - 260 Pins (from 300 Pins) DDR4 SODIMM, .50mm Pitch DIMM Registration
  - Form factor, defined by MO-310C
  - Exception is height and component keepout

Card Types	"A" height denoted in Figure below
Standard	32mm
Large	50mm





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Connector Overview

Function	Signal Count for Interface	Number of Interfaces	Number of used pins	Total Signals
Power 3.3V			5	5
VDD_RGMII_REF			1	1
LPC 3.3v or ESPI 1.8v			1	1
Power 12 V			1	1
Ground			38	38
ADC	1	8	8	8
GPI/ADC	1	8	8	8
PCIe	7	1	7	7
RGMII/1GT PHY	14	1	14	14
VGA / GPIOs	7	1	7	7
RMII/NC-SI	10	1	10	10
Master JTAG/GPIO	6	1	6	6
USB host	4	1	4	4
USB device	3	1	3	3
SPI1: SPI for host - quad capable	7	1	7	7
SPI2: SPI for host	5	1	5	5
FWSPI: SPI for Boot - quad capable	7	1	7	7
SYSSPI: System SPI	4	1	4	4
LPC/eSPI	8	1	8	8
I2C / GPIOs	2	12	24	24
GPIOs / I2C	2	3	6	6
I2C	2	1	2	2
UARTs (TxD, RxD)	2	4	8	8
CONSOLE (Tx, Rx)	2	1	2	2
PWM	1	8	8	8
Tacho/GPIOs	1	16	16	16
PECI	2	1	2	2
GPIOs	1	37	37	37
GPIO/GPIO Expanders (Serial GPIO)	4	1	4	4
Reset and Power Good	1	2	2	2
Watchdogs/GPIO	1	2	2	2
BOOT_IND# / GPIO	1	1	1	1
RESERVED/KLUDGE	1	2	2	2

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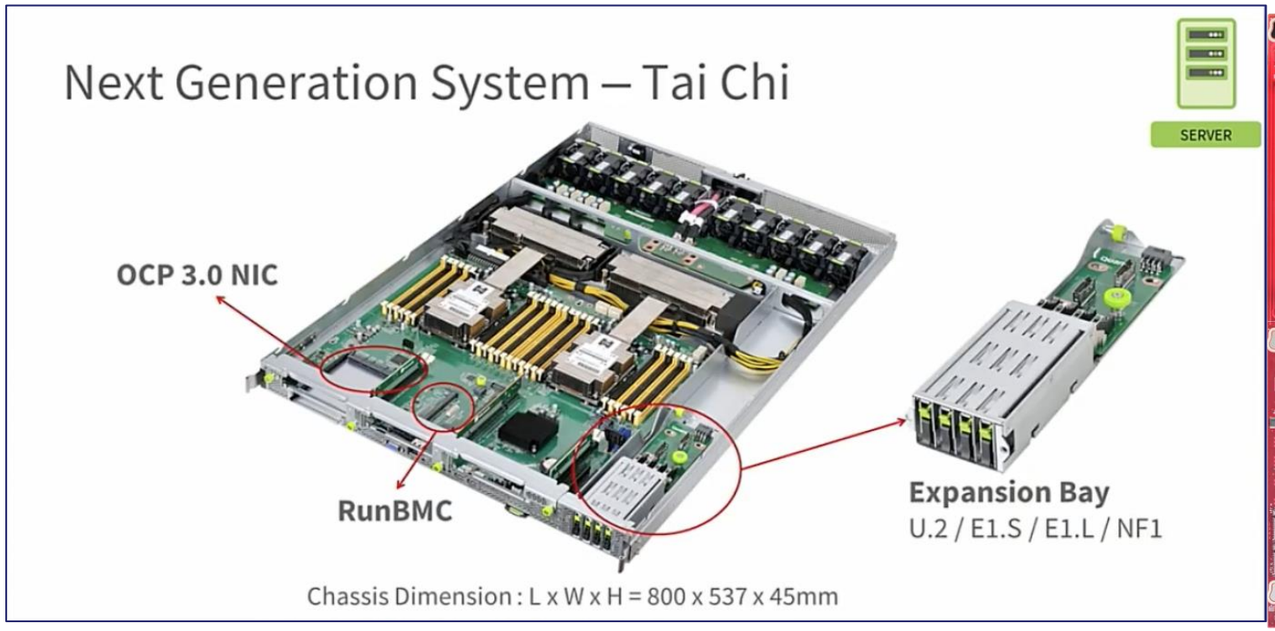
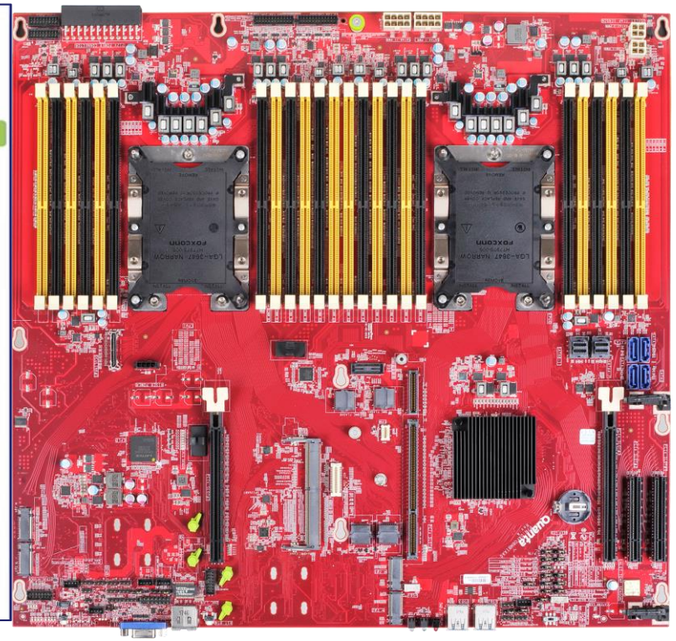
Benefits

- **Improved Security**
  - Hardened modular BMC acts as Root of Trust. Design is more stable, slower cadence cycle then server
  - Physically easier to control fabrication
- **Supply Chain**
  - Pick your own BMC to fit server needs
- **Manageability**
  - Managing the platform code
  - Consistent interfaces drive consistent code
- **Agile**
  - Move fast to market – Don’t redesign your BMC

Big Thanks to..

- **Hyve, QCT, Nuvoton, Microsoft, Google, Facebook, Aspeed & Twitter**





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Next Steps

- **BMC Standardization**
  - Specification for BMC server connections
  - A firmware stack that would comply to a standard, e.g. a “X PWM goes to X Fan” so that the system is intelligently “wired” and easier to control in terms of consistency.

- **Subgroup**

MANAGEMENT

Roadmap / Next Steps

- **AST2600 Reference Module**
  - Aspeed AST2600 is next gen SoC for upcoming server platforms
  - We will design from the specification to create a reference module based on this SoC
  - High Level: AST2600, 2 GB of DDR4 RAM, 1 GB of SPI NOR Serial Flash, 1 Gbps PHY on-board, pin compatible module that can replace any RunBMC AST2500 or RunBMC Poleg module (drop-in)

Thanks!

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