intel foundry services

Chiplets Open the World of Collaboration

Bob Brennan

VP, Customer Solutions Engineering, Intel Foundry Services

With technical contributions from:

Tak Abe, Bruce Fleming, Mark Gardner, Tanay Karnik, David Kehlet, Rob Munoz, Peter Onufryk, Edi Roytman, Debendra Das Sharma

Legal Notices and Disclaimers

Statements in this document that refer to future plans or expectations are forward-looking statements. These statements are based on current expectations and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in such statements. For more information on the factors that could cause actual results to differ materially, see our most recent earnings release and SEC filings at www.intc.com.

All product plans and roadmaps are subject to change without notice. Any forecasts of goods and services needed for Intel's operations are provided for discussion purposes only. Intel will have no liability to make any purchase in connection with forecasts published in this document. Code names are often used by Intel to identify products, technologies, or services that are in development and usage may change over time. No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

 This document contains information on products and/or processes in development.

intel foundry services

Outline

- Industry Vision
- Technical Challenges
- Technology Needed
- Commercial Case Studies

intel foundry services

Moore's Predicted "Day of Reckoning"

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected[1]."

-Gordon E. Moore

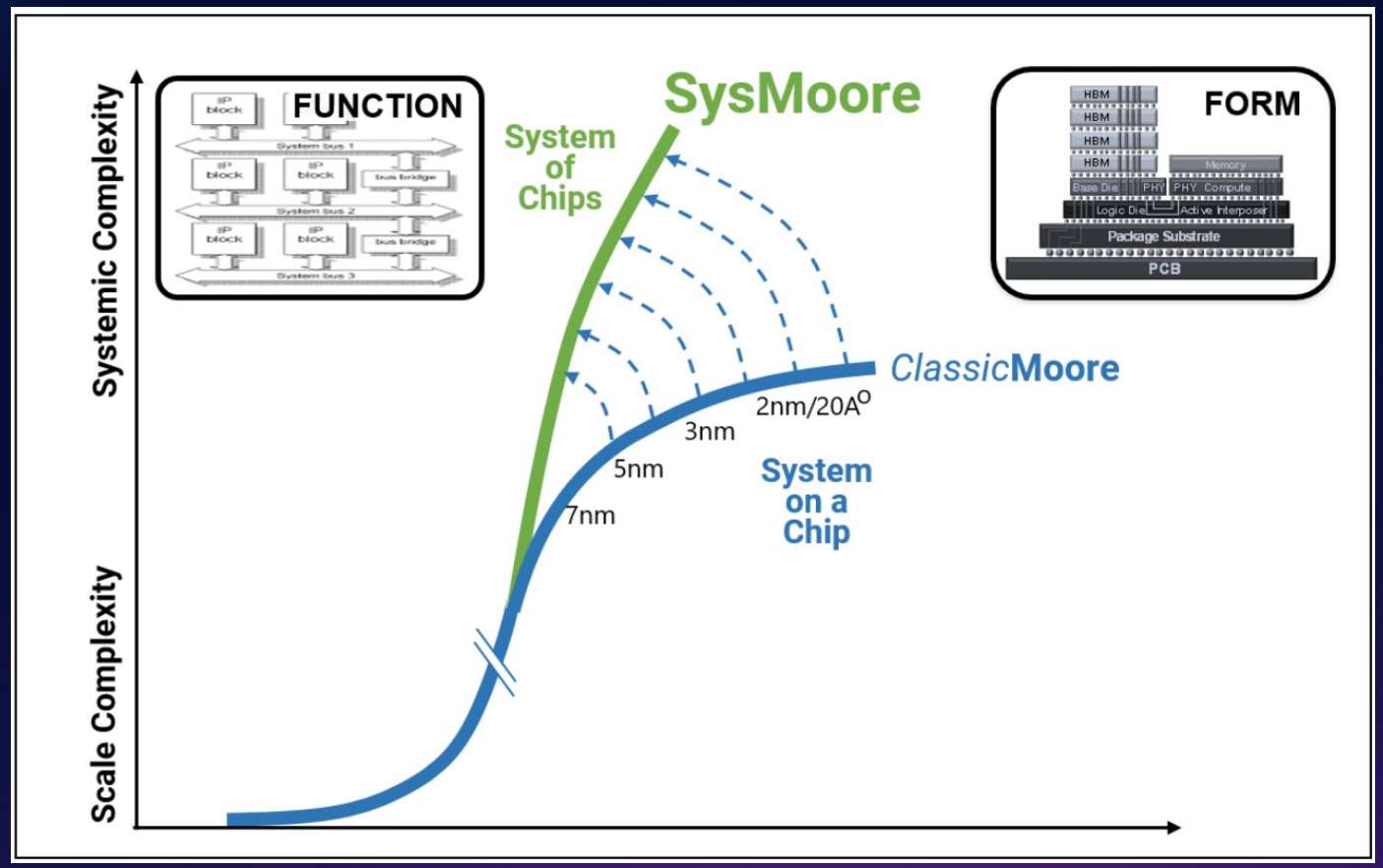
Image: Intel

[1]: "**Cramming more components onto integrated circuits**", Electronics, Volume 38, Number 8, April 19, 1965

intel foundry services

System on Chip -> System of Chips

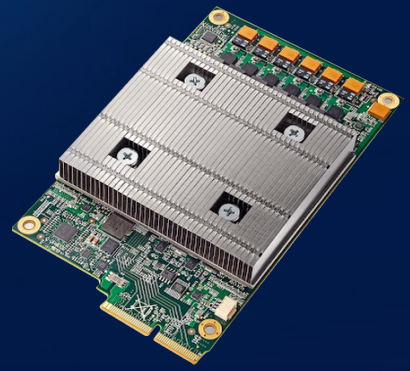
"Catalyzing the Impossible: Silicon, Software, and Smarts for the SysMoore Era" – Dr. Aart de Geus



Source: Synopsys, https://www.synopsys.com/glossary/what-is-sysmoore.html

Google Cloud Blog*: A Chiplet Innovation Ecosystem for a New Era of Custom Silicon

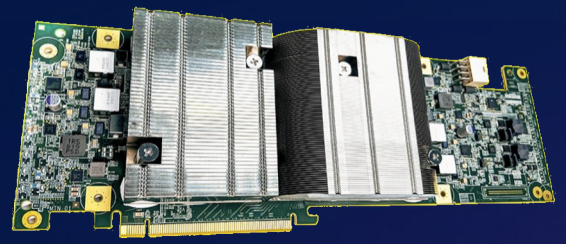
Growing Demand for AI



Google Tensor Processing Unit

Growing Demand for Video

(YouTube, Live Streaming)



Google Video Coding Unit

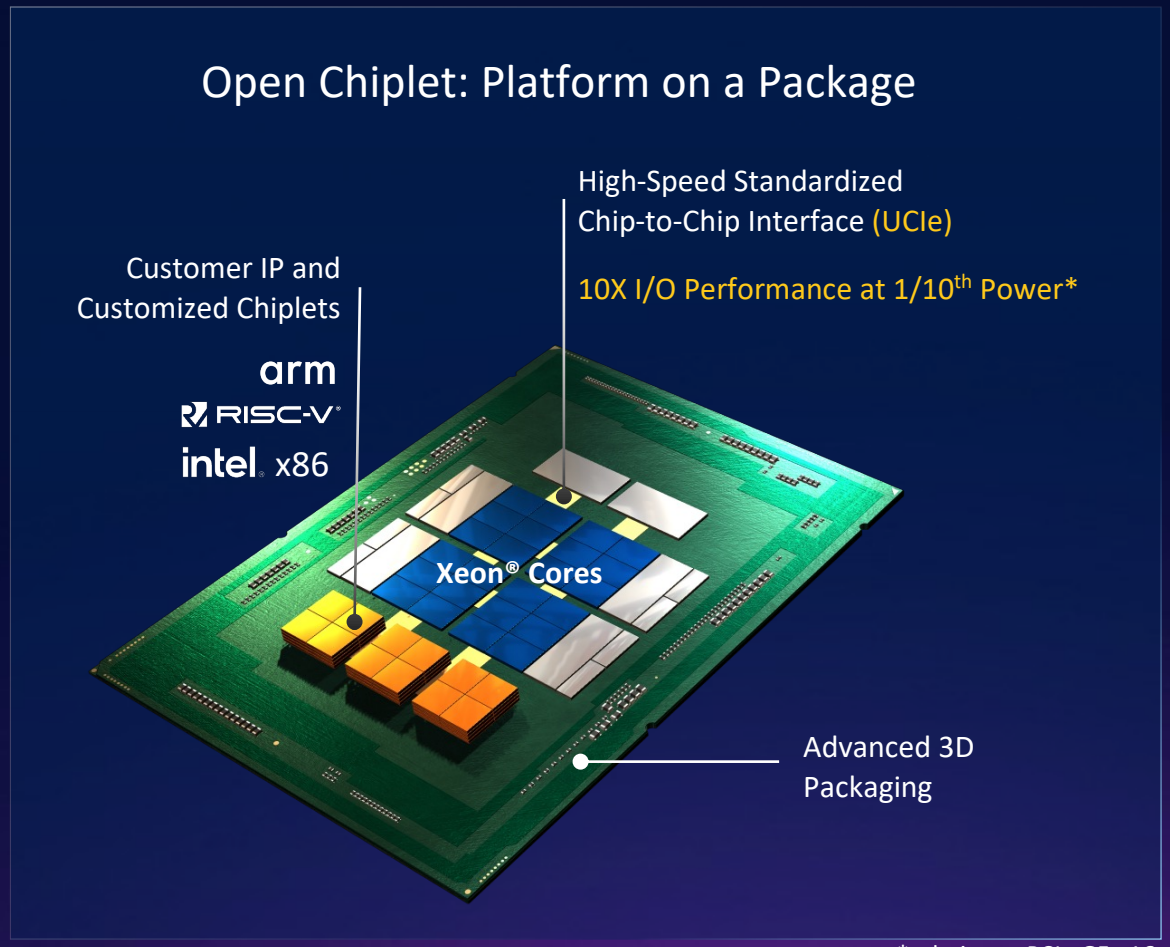
Image credit: Google

What's needed:

- Modularity
- Optimized Silicon and Package
- Open Standards, examples:
  - IO
  - Protocols
  - Security
  - Management

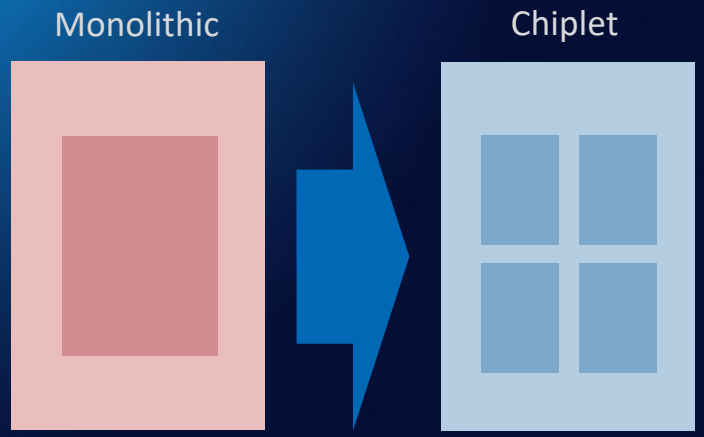
*https://cloud.google.com/blog/topics/systems/open-chiplet-ecosystem-powering-next-era-of-custom-silicon

Intel Vision : The “Chiplet Revolution”



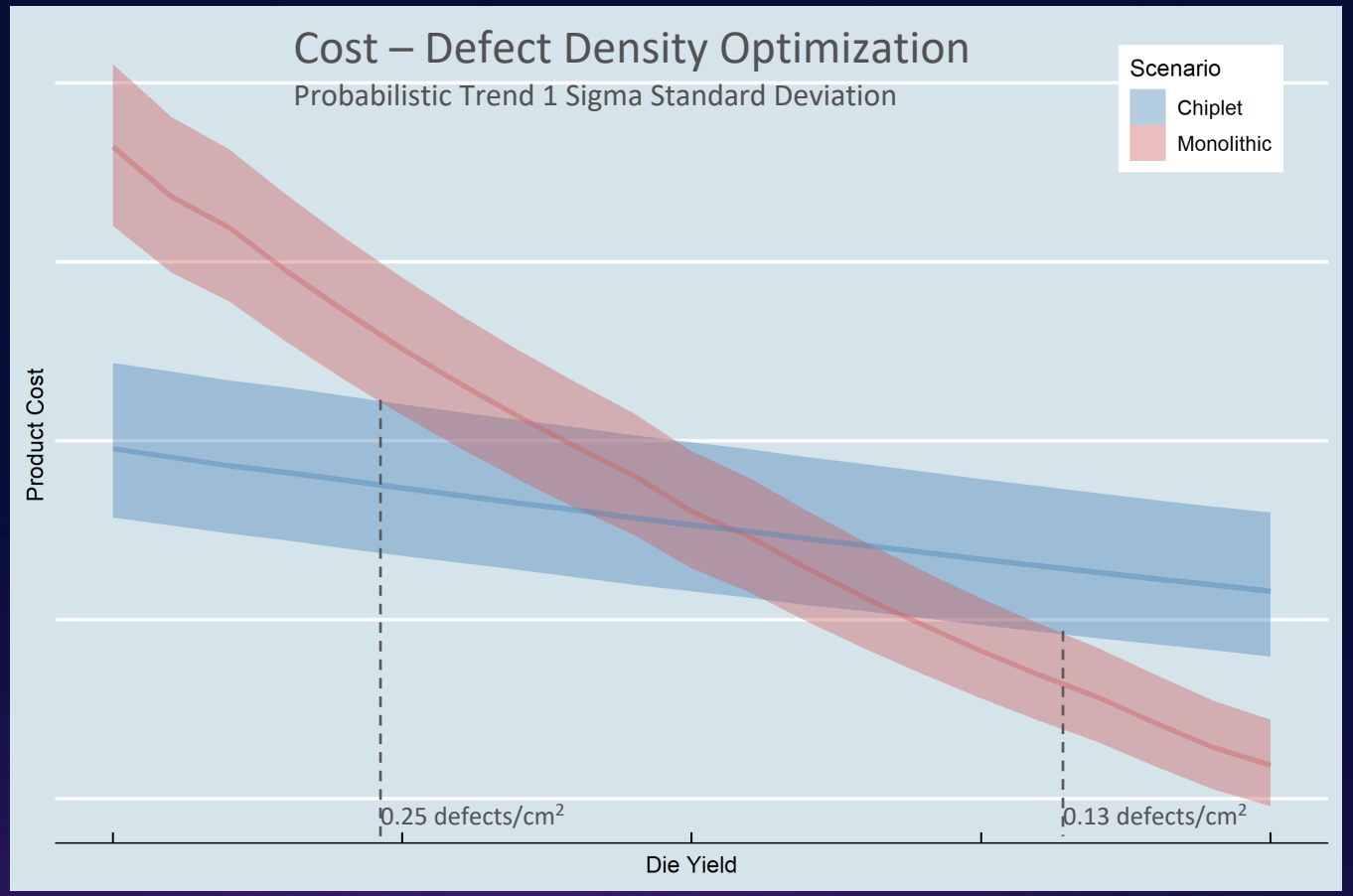
*relative to PCIe G5 x16

Motivation : Cost & Manufacturing Optimization



Input Variables:

- Die Area
- # of Chiplets
- Wafer Cost
- Defect Density
- Package/Assembly/Test
- Known Good Die
- Die Area Tax & Overhead

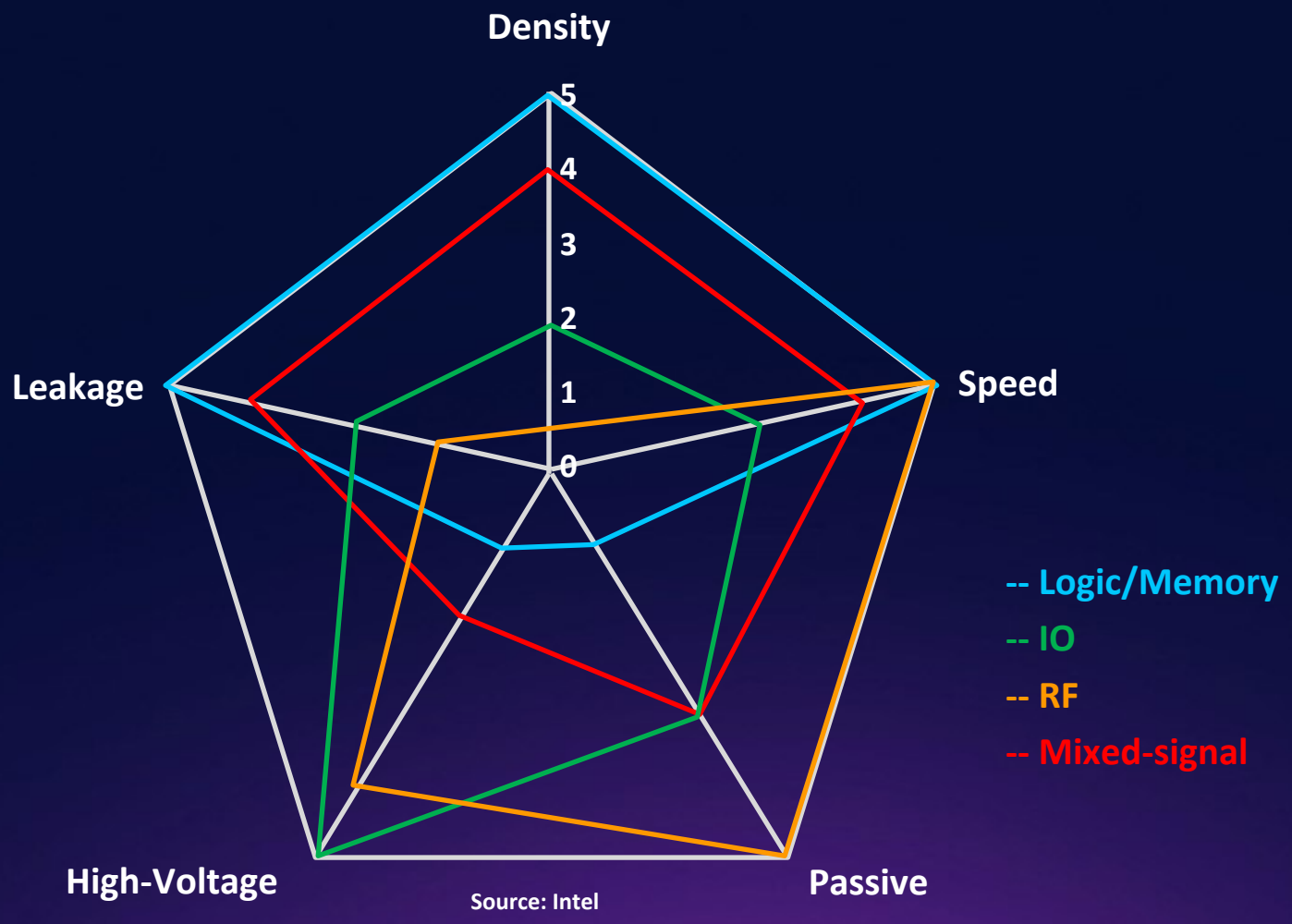


*Probabilistic trend by 1std dev

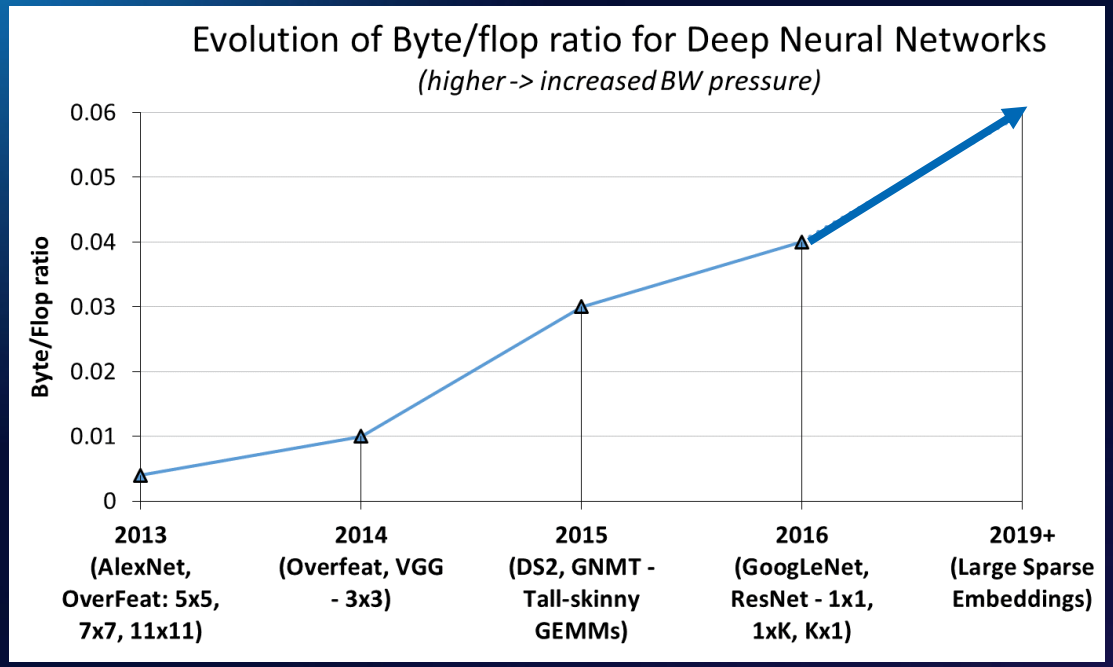
Source: Intel Model

Reference: https://ieeexplore.ieee.org/document/9758914
"Heterogeneous Integration of Chiplets: Cost and Yield Tradeoff Analysis"

Motivation : Process Technology Optimization

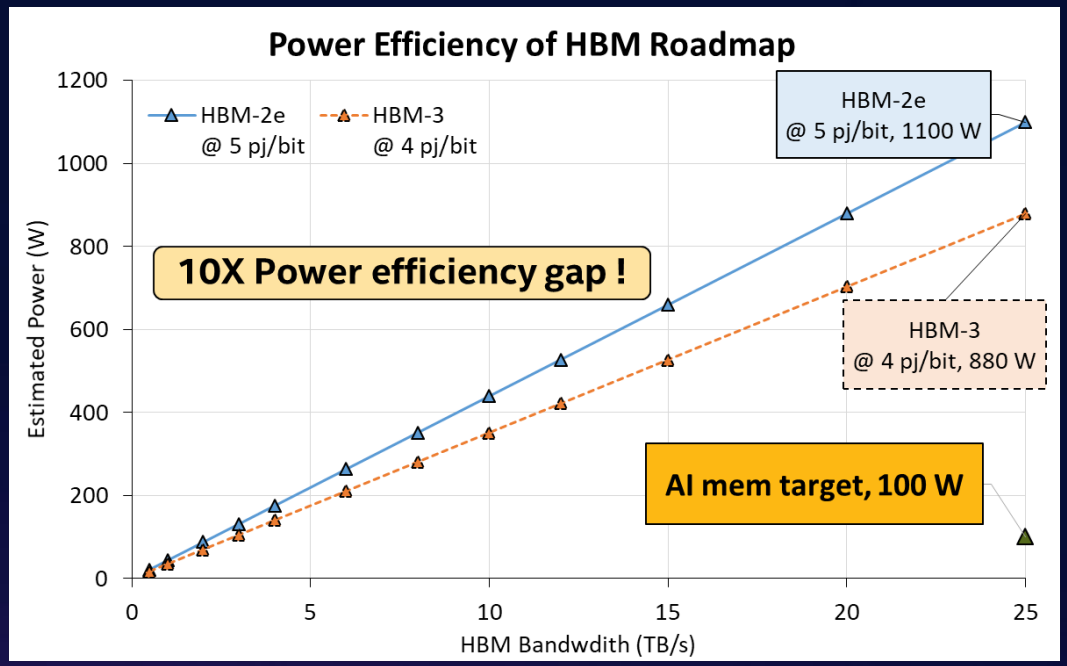


Motivation : AI Memory BW/Power Gap



2020 AI Compute ~ 400 Tops
0.06 B/F → 25 TB/s

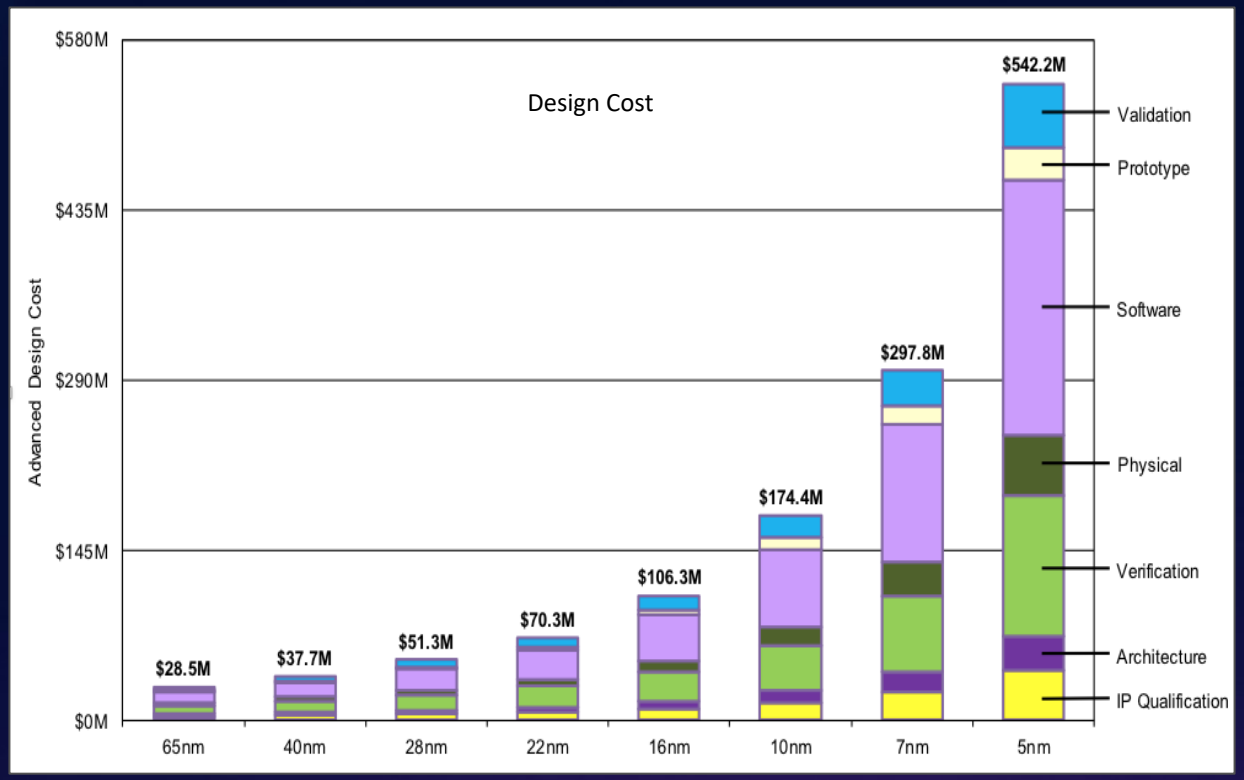
Source: Intel



Source: Intel

- Insatiable Memory Bandwidth
- The energy efficiency gap is getting bigger

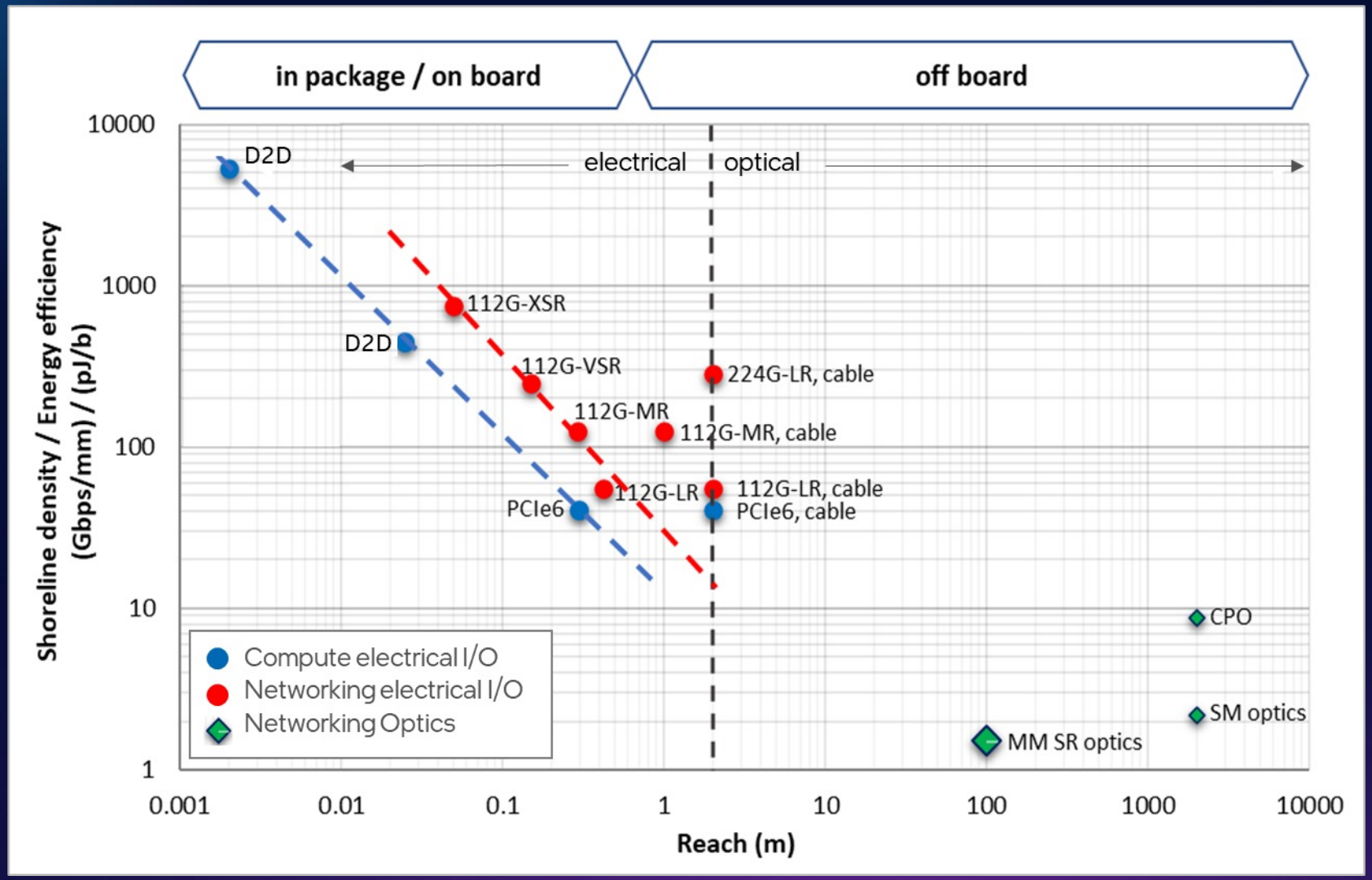
Motivation: R&D Cost and Product Velocity



Source: Lapadeus, M., "Big Trouble At 3nm", Semiconductor Engineering, June 21, 2018
cited in IEEE Heterogeneous Integration Roadmap
https://eps.ieee.org/images/files/HIR_2020/ch02_hpc_1.pdf

Move from Exponential -> Linear with modularity and reuse

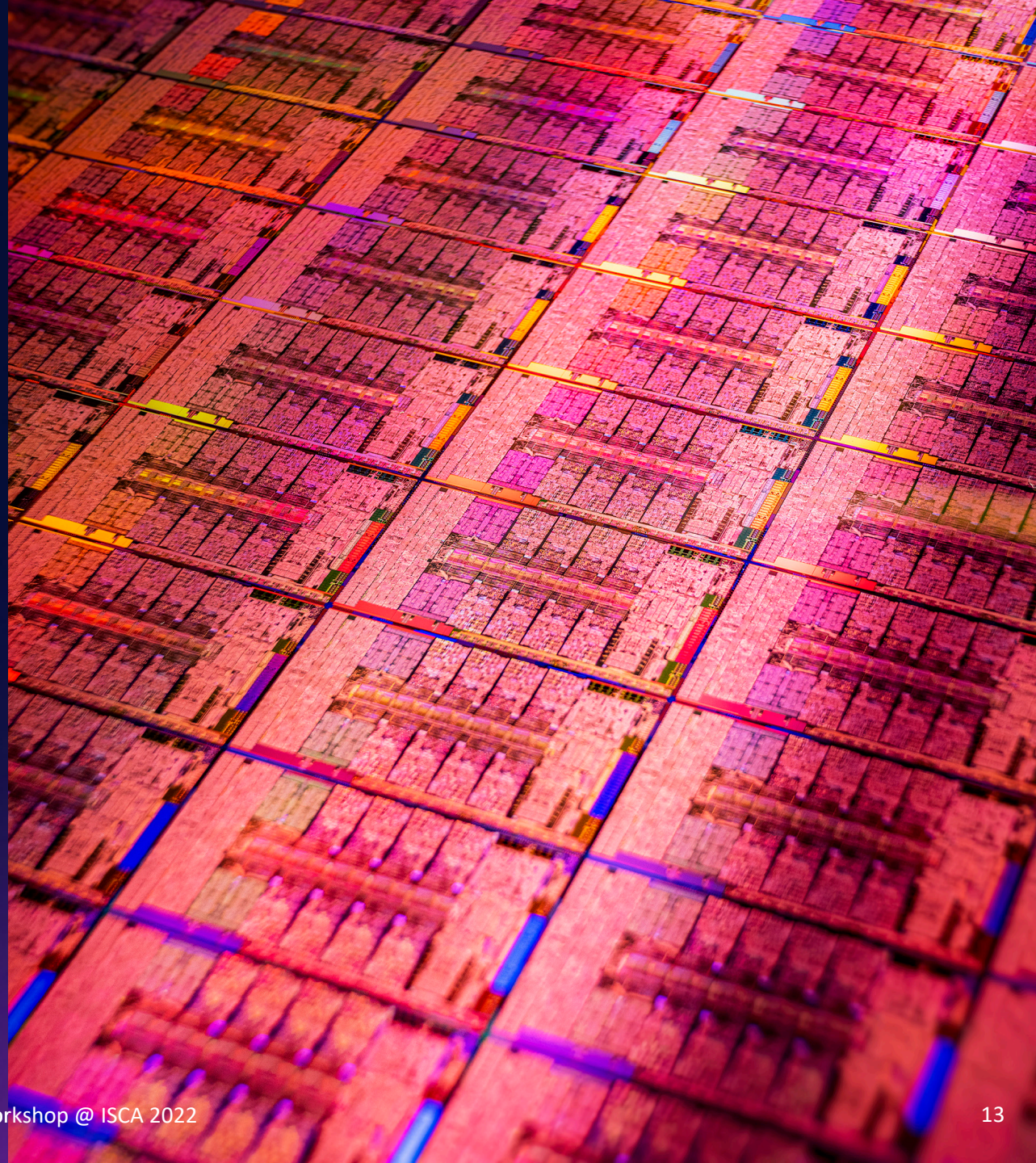
Motivation: Optimize System Level High Speed IO



Source: Intel

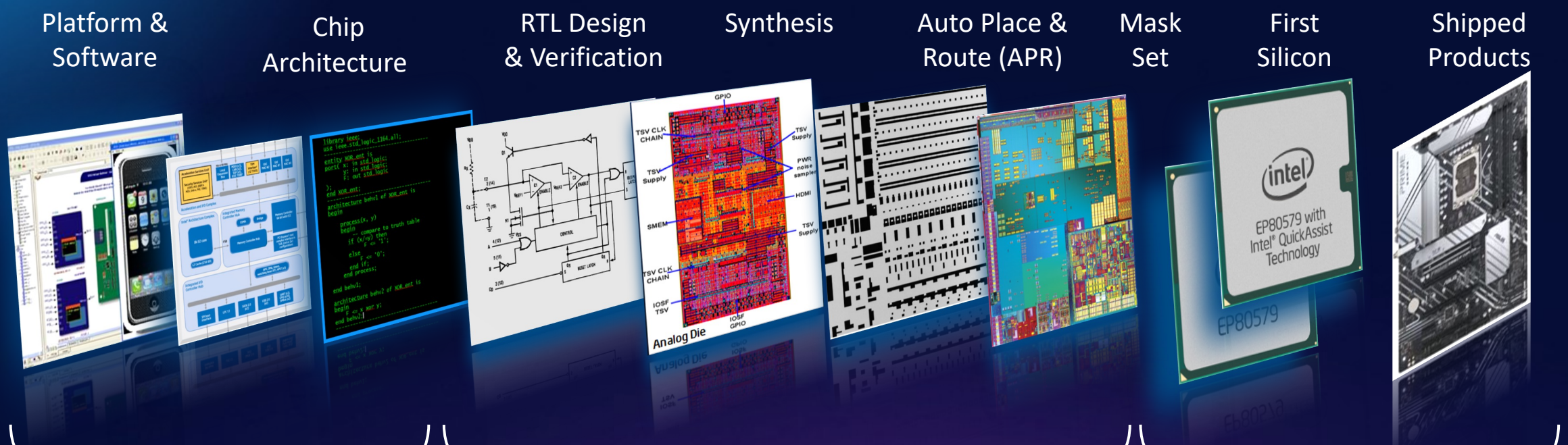
Technology Needed

Open Ecosystem



intel foundry services

New Development Model : System on Chip -> System of Chips



UCIe Open Interconnect & Packaging

UCIe Universal Chiplet Interconnect Express

Standard Specifications

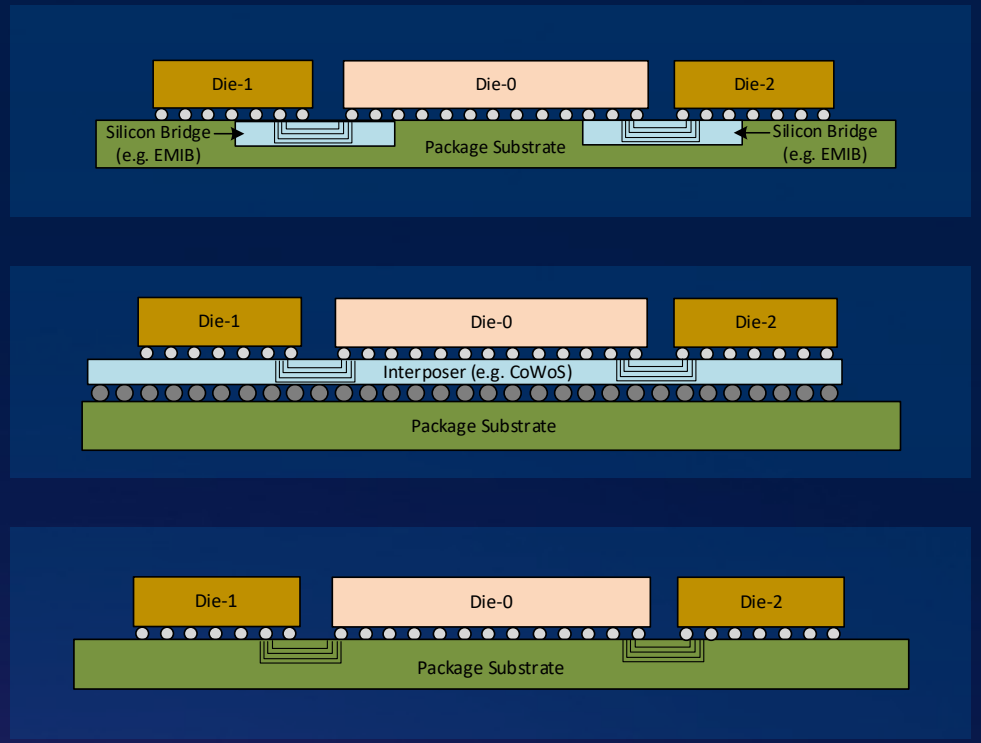
Physical Layers	Protocols	Form Factors	Management
Initial D2D I/O	CXL™/PCIe®		

INITIAL FOCUS

- Physical Layer: Die-to-Die I/O with industry leading KPIs
- Protocol: CXL/PCIe for near-term volume attach
- Well-defined specification: ensure interoperability & evolution

FUTURE GOALS

- Additional protocols (ex. CHI)
- Advanced chiplet form-factors
- Chiplet management
- Security
- And much more!

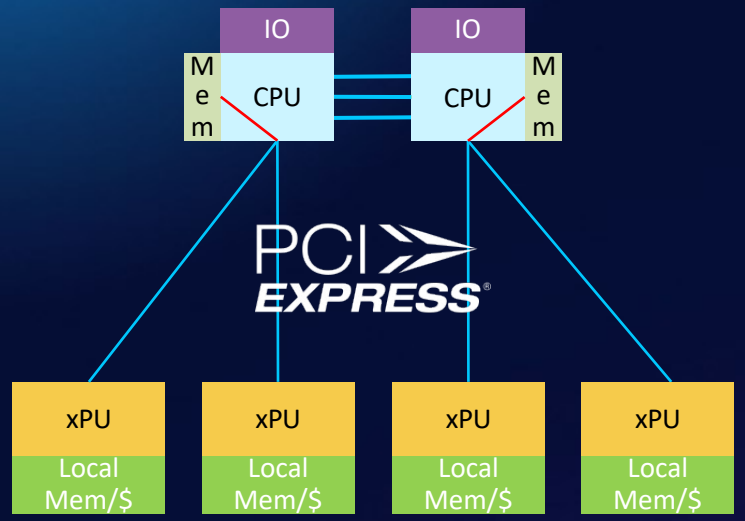


Different flavors of packaging options supported to build an open ecosystem

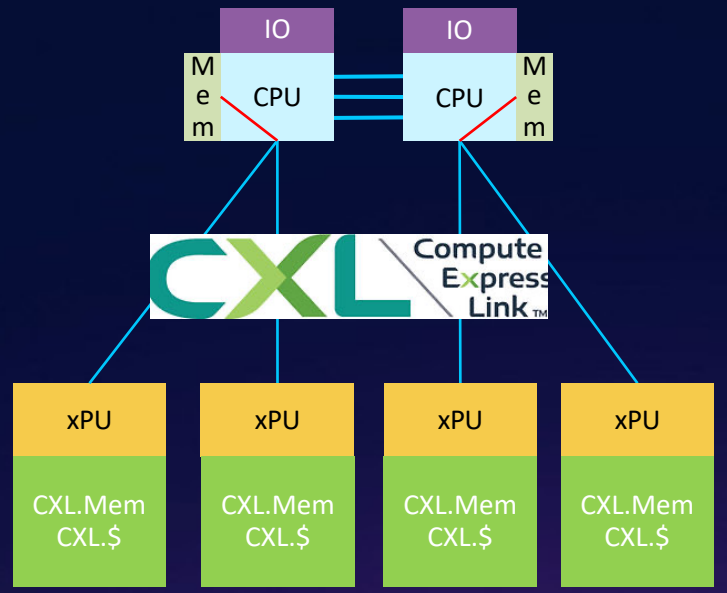
intel foundry services

Open Protocols for xPU

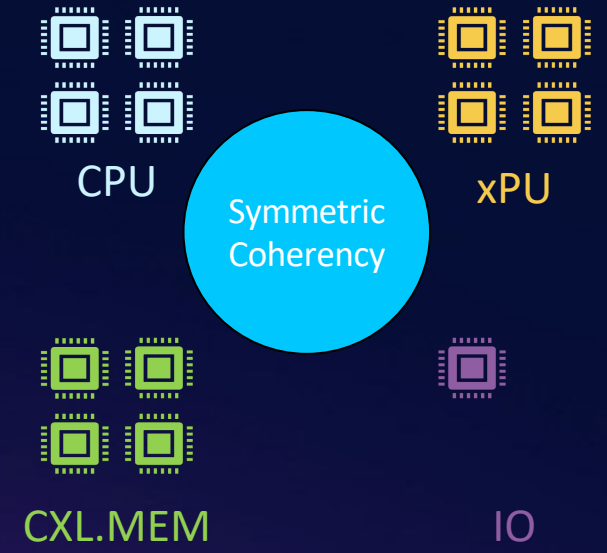
DMA Only



Asymmetric Coherency (CXL.$)

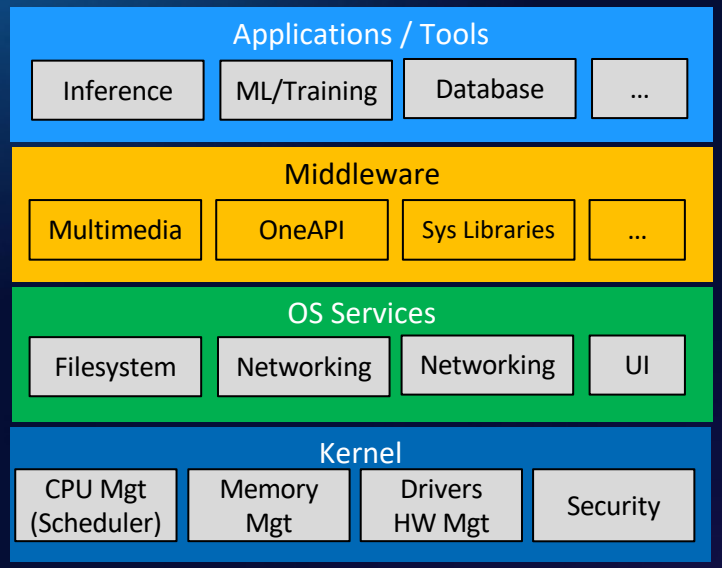


(Hypothetical) Symmetric Coherency



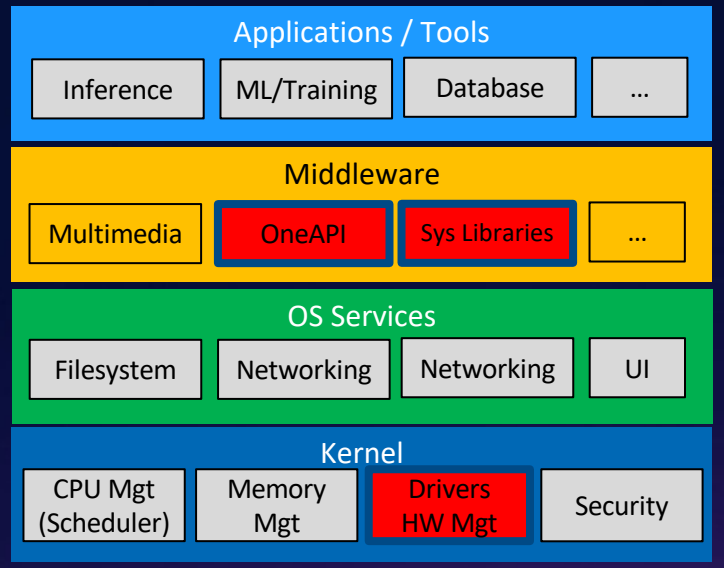
New Open Software Stack for Heterogenous Computing

DMA Only



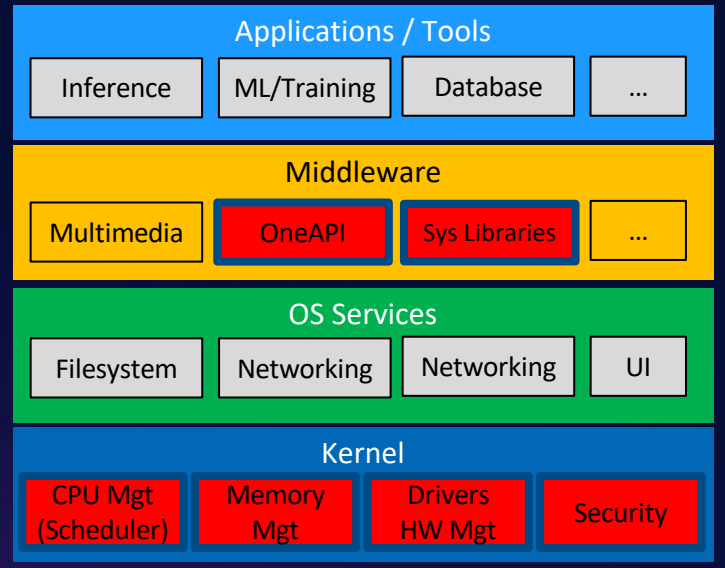
Device Driver Model

Asymmetric Coherency (CXL.$)



Middleware -> Device

(Hypothetical) Symmetric Coherency



Peer-Peer Graphed Execution

intel foundry services

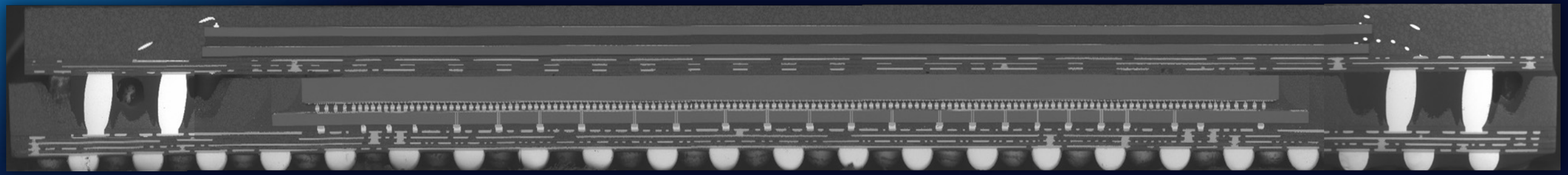
Chiplets

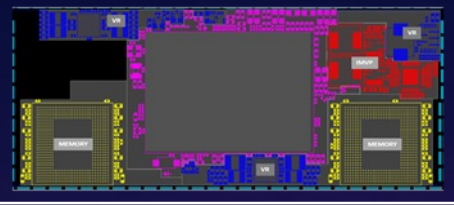
Industry Case Studies & Representative Applications

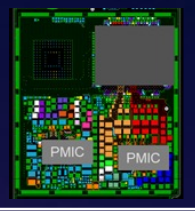
intel foundry services

Case Study: Intel Client, Lakefield 3D Foveros

ex. Market Segmentation (GFX, Memory), Process Optimization





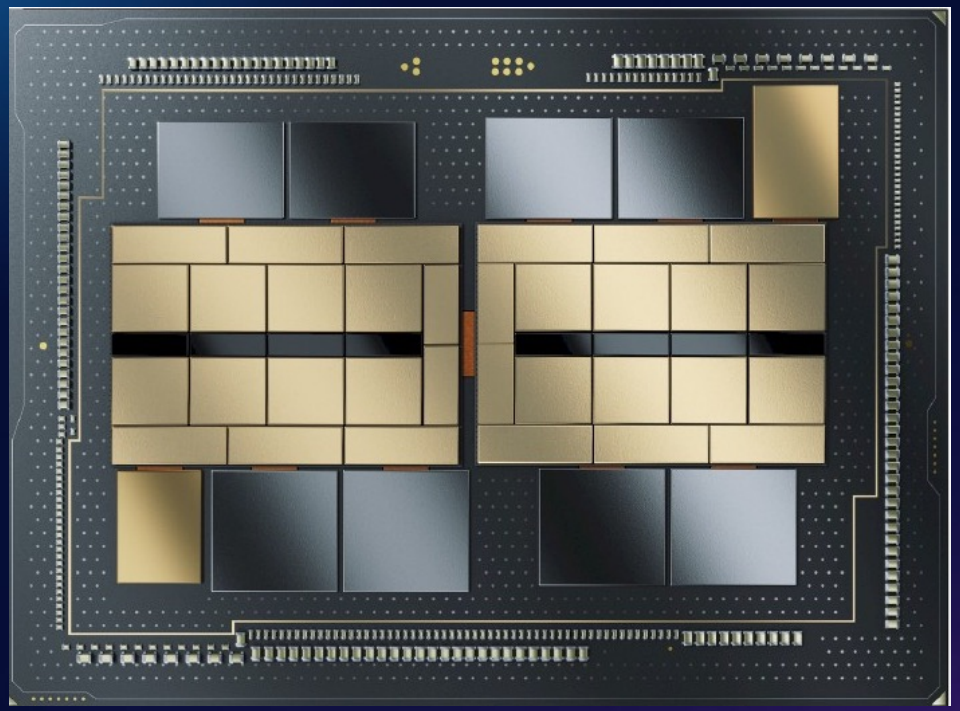


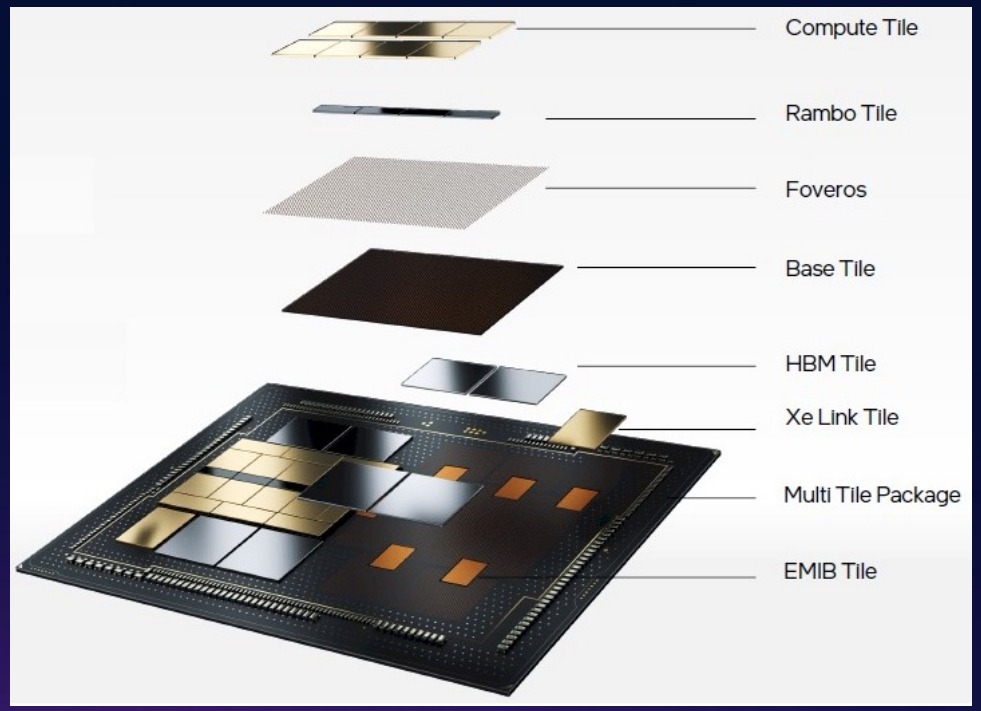
	Y SKU Gen-1	Y SKU	LKF
Package	20.5x16.5	26.5x18.5	12x12
Memory	LP3 11x11.5	LP4-4x 12.5x12.5	LP4-4x POP

intel foundry services

Case Study : Intel HPC - Ponte Vecchio

ex. Complexity Management, Process Optimization

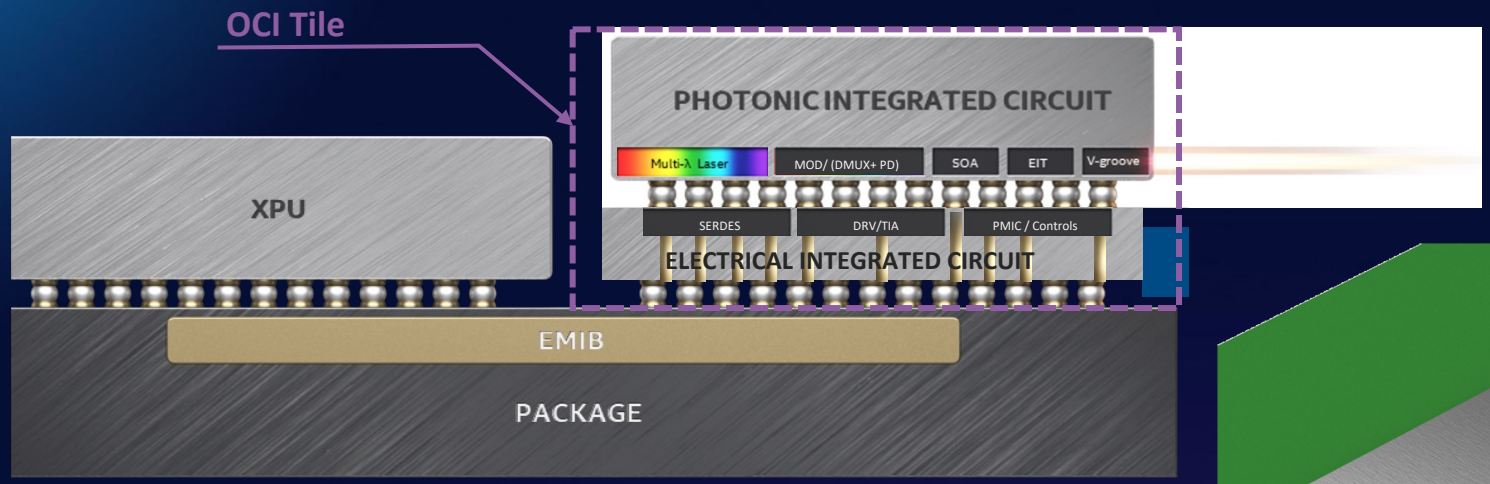


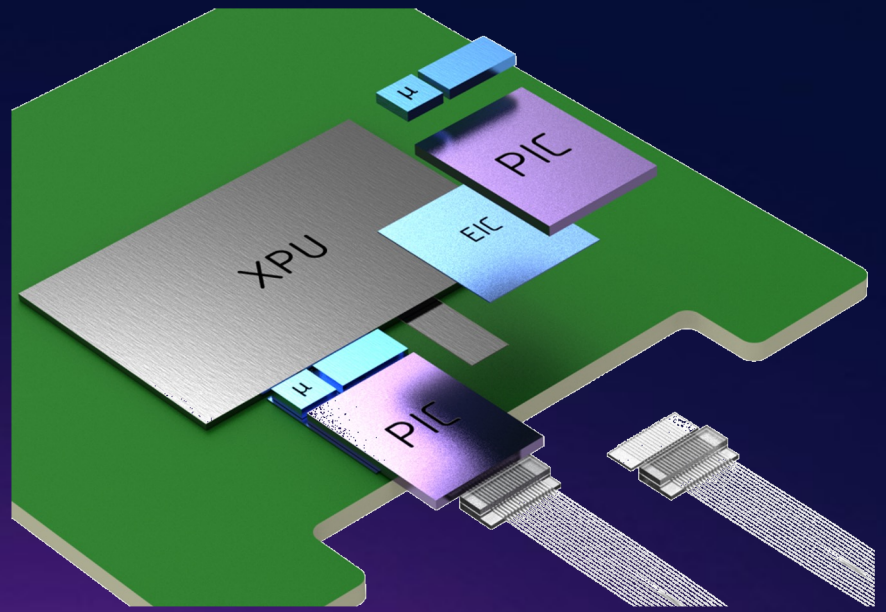


intel foundry services

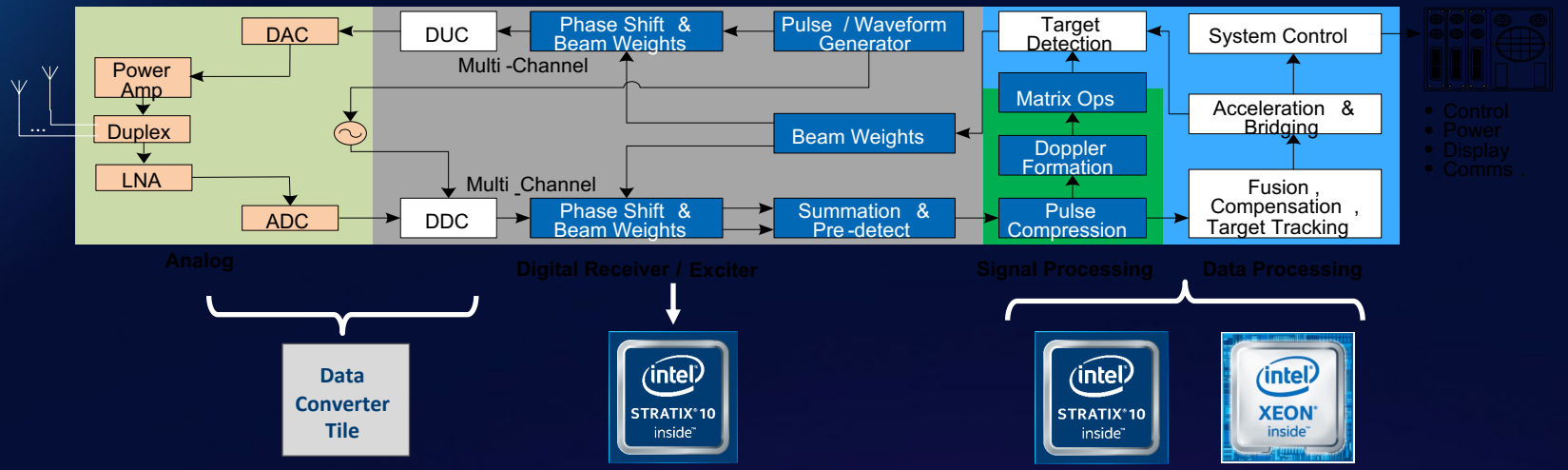
IO Optimization: Intel Optical

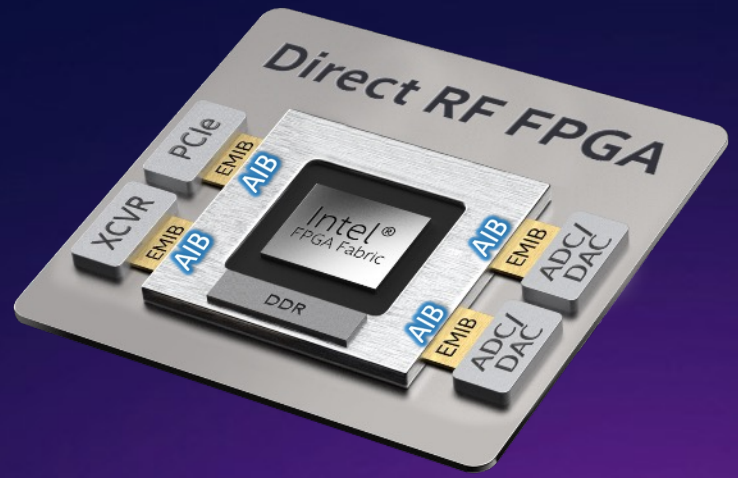
ex. Network Optimization through Modularity





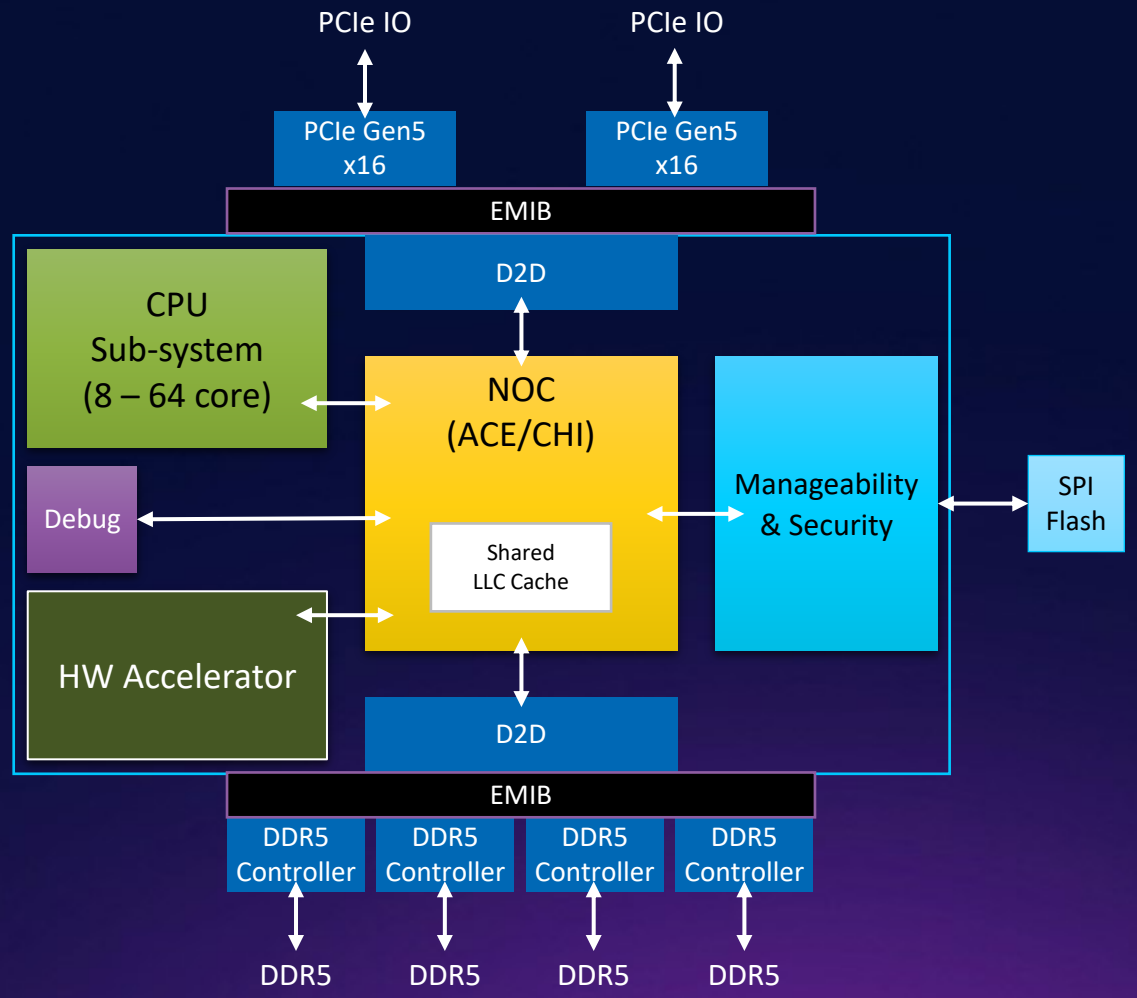
Sensor Case Study: Radar Beamforming Application





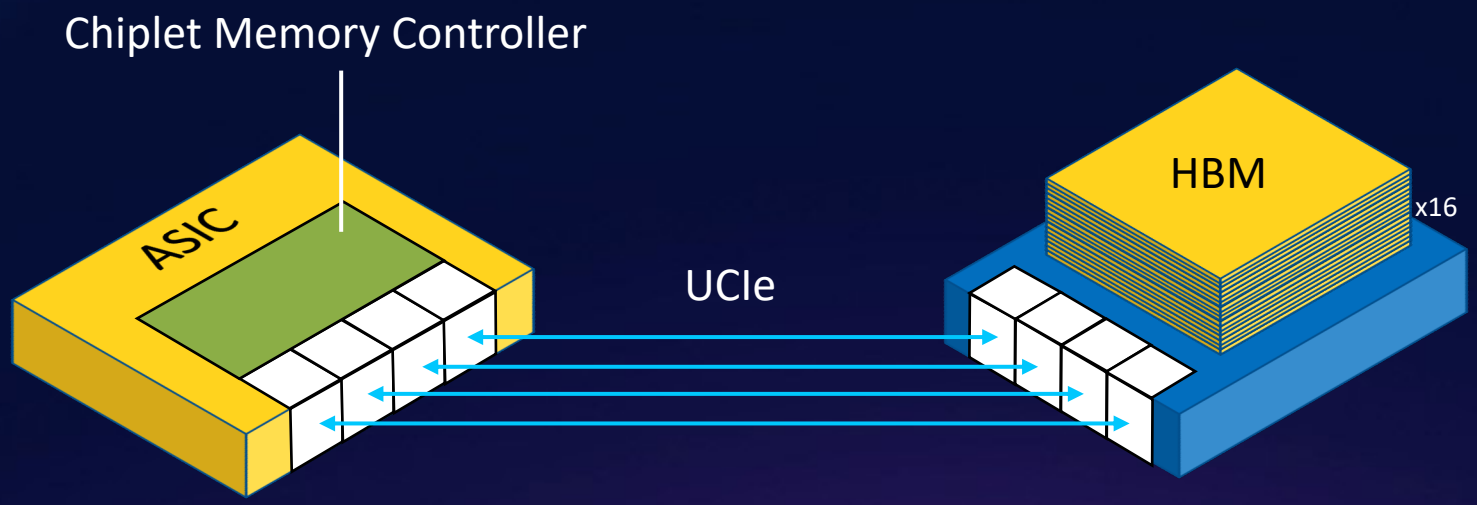
IO Case Study: Disaggregated PCIe & Memory

ex. Optimization of Process (ex. Analog), Supply Chain



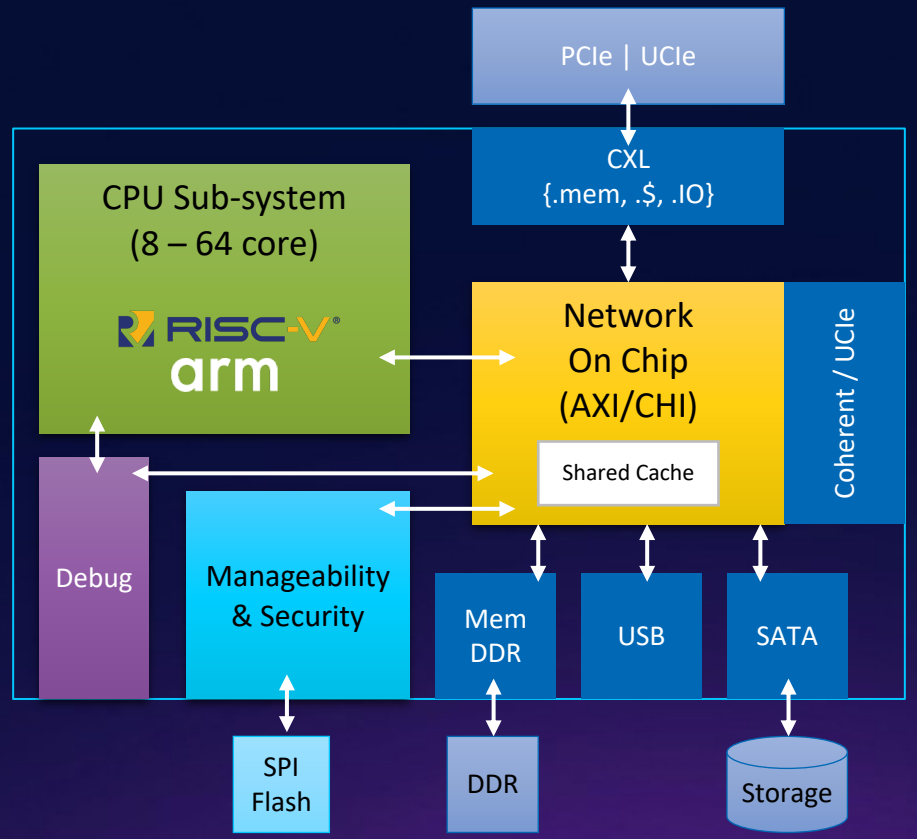
IO Case Study: Possible HBM Architecture

Optimize : AI Bandwidth/Power Density, AI Thermals



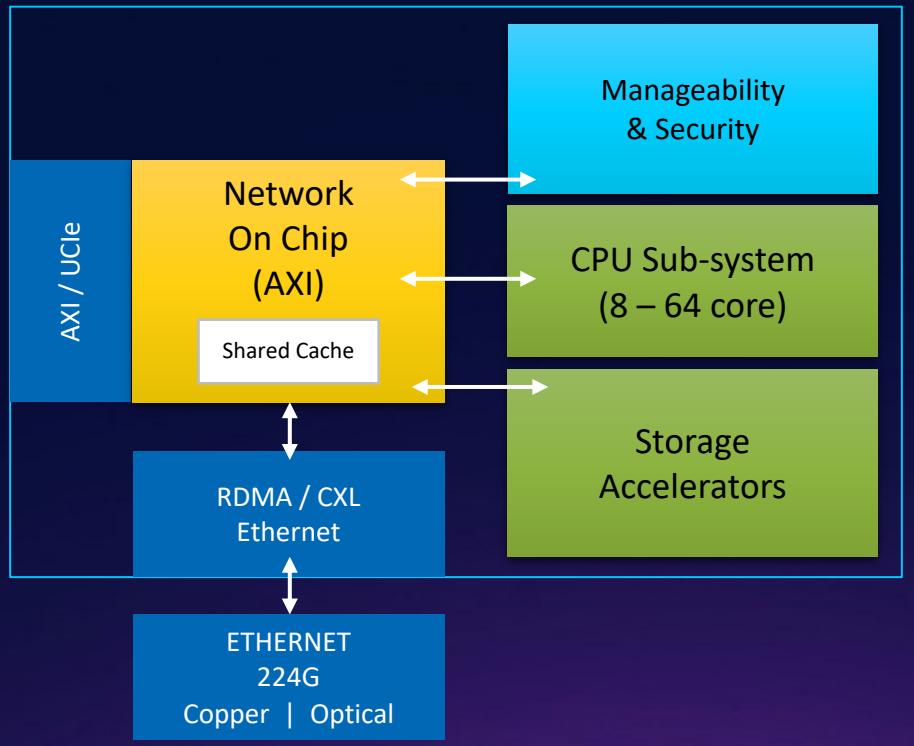
Server Case Study: Multi-core uServer

Ex. Multi-Protocol Architecture : CXL/UCIe and CHI/UCIe



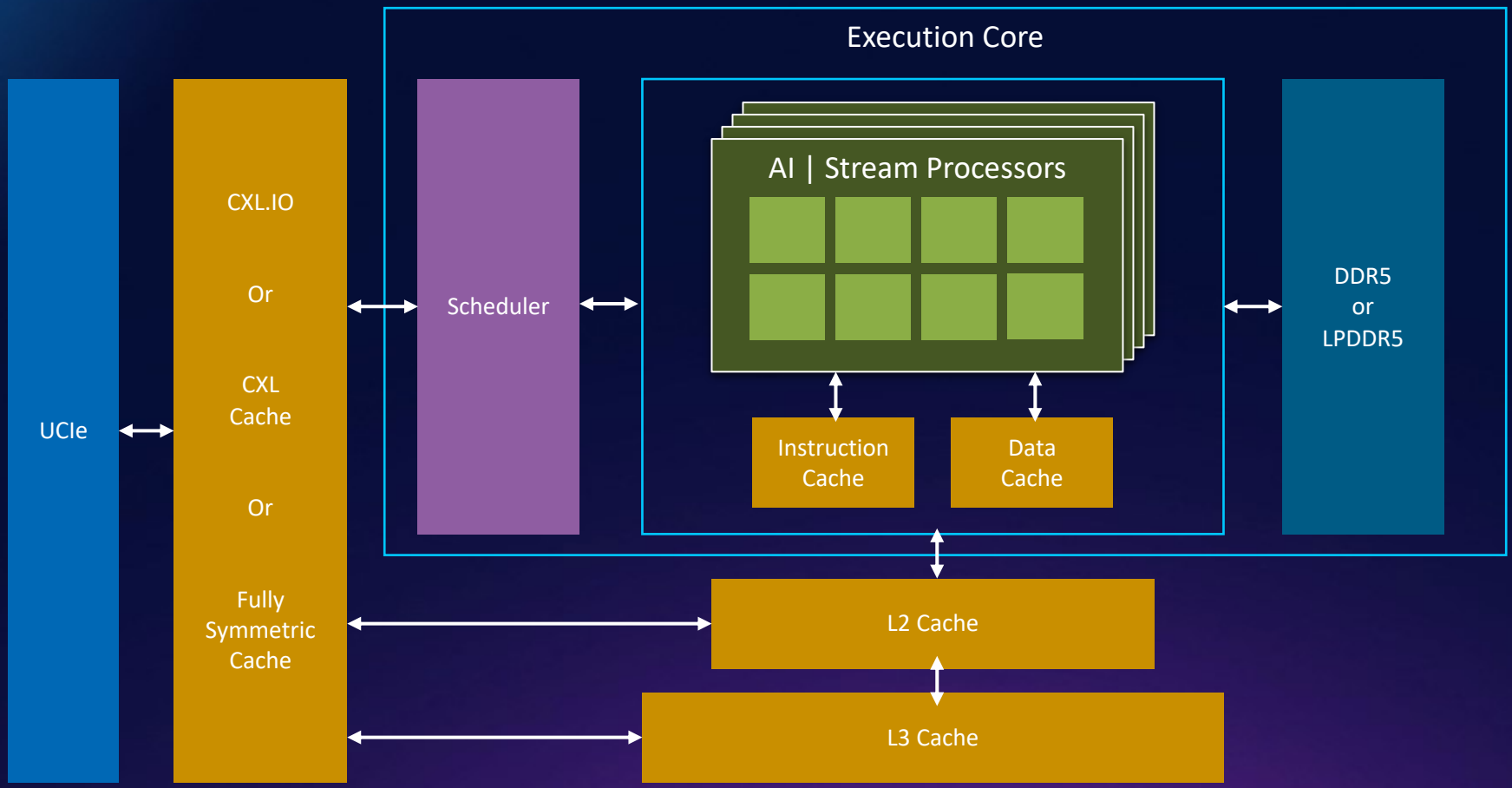
Networking/Storage Case Study: IPU/DPU

Ex. Multi-Protocol Architecture : AXI/UCIe ; Networking Modularity



AI Case Study: Caching Inference Architecture

Ex. DMA, Asymmetric Coherence, Symmetric Coherence



Summary

- Industry Vision – we are at an inflection point
- Technical Challenges – die size, process, IO, and R&D $ optimization
- Technology Needed – CAD tools, Distributed Coherency, Software, Interconnect, Packaging
- Commercial Case Studies – many new emerging architectures, it’s just the beginning, let’s collaborate!

intel foundry services

Thank you