Chiplets Open the World of Collaboration

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Outline

- Industry Vision
- Technical Challenges
- Technology Needed
- Commercial Case Studies
Moore’s Predicted “Day of Reckoning”

“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected¹.”

-Gordon E. Moore

¹: “Cramming more components onto integrated circuits”, Electronics, Volume 38, Number 8, April 19, 1965
System on Chip -> System of Chips

“Catalyzing the Impossible: Silicon, Software, and Smarts for the SysMoore Era” – Dr. Aart de Geus

Google Cloud Blog*: A Chiplet Innovation Ecosystem for a New Era of Custom Silicon

Growing Demand for AI

What’s needed:

• Modularity
• Optimized Silicon and Package
• Open Standards, examples:
  ▪ IO
  ▪ Protocols
  ▪ Security
  ▪ Management

Growing Demand for Video

(YouTube, Live Streaming)

*https://cloud.google.com/blog/topics/systems/open-chiplet-ecosystem-powering-next-era-of-custom-silicon

Image credit: Google

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Google Tensor Processing Unit

Google Video Coding Unit

Image credit: Google
Intel Vision: The “Chiplet Revolution”

Open Chiplet: Platform on a Package

- Customer IP and Customized Chiplets
- High-Speed Standardized Chip-to-Chip Interface (UCle)
- 10X I/O Performance at 1/10th Power*
- Advanced 3D Packaging

*relative to PCIe G5 x16
Motivation: Cost & Manufacturing Optimization

Input Variables:
- Die Area
- # of Chiplets
- Wafer Cost
- Defect Density
- Package/Assembly/Test
- Known Good Die
- Die Area Tax & Overhead

"Heterogeneous Integration of Chiplets: Cost and Yield Tradeoff Analysis"

Source: Intel Model
Motivation: Process Technology Optimization

Density

Leakage

High-Voltage

Passive

Source: Intel

-- Logic/Memory
-- IO
-- RF
-- Mixed-signal

Source: Intel
Motivation: AI Memory BW/Power Gap

- Insatiable Memory Bandwidth
- The energy efficiency gap is getting bigger
Motivation: R&D Cost and Product Velocity

Move from Exponential -> Linear with modularity and reuse
Motivation: Optimize System Level High Speed IO

Source: Intel
Technology Needed
Open Ecosystem
New Development Model: System on Chip -> System of Chips
UCle Open Interconnect & Packaging

**INITIAL FOCUS**
- Physical Layer: Die-to-Die I/O with industry leading KPIs
- Protocol: CXL/PCIe for near-term volume attach
- Well-defined specification: ensure interoperability & evolution

**FUTURE GOALS**
- Additional protocols (ex. CHI)
- Advanced chiplet form-factors
- Chiplet management
- Security
- And much more!

Different flavors of packaging options supported to build an open ecosystem
Open Protocols for xPU

DMA Only

Asymmetric Coherency (CXL.$)

(Hypothetical) Symmetric Coherency

CPU

Symmetric Coherency

xPU

CXL.MEM

IO
New Open Software Stack for Heterogenous Computing

**Device Driver Model**

**Asymmetric Coherency (CXL.$)**

**(Hypothetical) Symmetric Coherency**

- DMA Only
- Asymmetric Coherency (CXL.$)
- (Hypothetical) Symmetric Coherency

**Applications / Tools**
- Inference
- ML/Training
- Database
- ...

**Middleware**
- Multimedia
- OneAPI
- Sys Libraries
- ...

**OS Services**
- Filesystem
- Networking
- Networking
- UI

**Kernel**
- CPU Mgt (Scheduler)
- Memory Mgt
- Drivers HW Mgt
- Security

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**Device Driver Model**

**Middleware -> Device**

**Peer-Peer Graphed Execution**
Chiplets
Industry Case Studies & Representative Applications
Case Study: Intel Client, Lakefield 3D Foveros

ex. Market Segmentation (GFX, Memory), Process Optimization

<table>
<thead>
<tr>
<th></th>
<th>Y SKU Gen-1</th>
<th>Y SKU</th>
<th>LKF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>20.5x16.5</td>
<td>26.5x18.5</td>
<td>12x12</td>
</tr>
<tr>
<td>Memory</td>
<td>LP3 11x11.5</td>
<td>LP4-4x 12.5x12.5</td>
<td>LP4-4x POP</td>
</tr>
</tbody>
</table>
Case Study: Intel HPC - Ponte Vecchio

ex. Complexity Management, Process Optimization
IO Optimization: Intel Optical

ex. Network Optimization through Modularity
Sensor Case Study: Radar Beamforming Application

- **Digital Receiver / Exciter**
  - ADC
  - DAC
  - LNA
  - Duplex
  - Power Amp

- **Signal Processing**
  - DDC
  - DUC
  - Phase Shift & Beam Weights
  - Pulse / Waveform Generator

- **Data Processing**
  - Summation & Pre-detect
  - Beam Weights
  - Target Detection
  - Fusion, Compensation, Target Tracking

- **System Control**
  - System Control
  - Acceleration & Bridging

- **Multi-Channel**
  - Multi-Channel

- **Analog**
  - Data Converter Tile

- **Direct RF FPGA**
  - Intel® Stratix® 10
  - Intel® Xeon®

- **Applications**
  - Control
  - Power
  - Display
  - Comms

HiPChips Chiplet Workshop @ ISCA 2022
IO Case Study: Disaggregated PCIe & Memory

ex. Optimization of Process (ex. Analog), Supply Chain
IO Case Study: Possible HBM Architecture

Optimize: AI Bandwidth/Power Density, AI Thermals
Server Case Study: Multi-core uServer

Ex. Multi-Protocol Architecture: CXL/UCIe and CHI/UCIe
Networking/Storage Case Study: IPU/DPU

Ex. Multi-Protocol Architecture: AXI/UCle; Networking Modularity
AI Case Study: Caching Inference Architecture

Ex. DMA, Asymmetric Coherence, Symmetric Coherence

- Ex. DMA, Asymmetric Coherence, Symmetric Coherence
Summary

• Industry Vision – we are at an inflection point
• Technical Challenges – die size, process, IO, and R&D $ optimization
• Technology Needed – CAD tools, Distributed Coherency, Software, Interconnect, Packaging
• Commercial Case Studies – many new emerging architectures, it’s just the beginning, let’s collaborate!
Thank you