OPEN Compute Project[®]

OCP – ODSA Project

Commercialization Use Case



Fourth Generation SmartNIC Architectural Imperatives

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Community Led



Why ODSA at Corigine & NETRONCME

Motivation to use OCP/ODSA philosophy and standards

- Netronome and Corigine are building <u>Fourth Generation SmartNICs</u> which have several specific requirements including..
 - Flexibility ability to integrate specialized subsystems components from different vendors e.g. I/O chiplet, datapath processors, management plane processors, crypto, ML/AI cores
 - **Composability** heterogeneous elements from 3rd parties and different foundry nodes
 - □ Open standards not just interface standards, but also open instruction set (RiscV)
 - Scalability link speeds scaling from 25G to nX100Gbps, processing and bandwidth to assure line rate without blocking or dropped packets (including very large packets)



- Power-Performance-Area Denard Scaling and Moore's Law dictate that a chiplet based implementation is vastly superior to a monolithic implementation from PPA, yield and cost perspectives
- Netronome has been involved with ODSA
 - Since inception in 2019
 - □ Early evangelists / proselytizers



ODSA Use Case at Corigine & NETRONCME

Product intersection with ODSA specifications

1. Implementing multiple interfaces using D2D controller with BOW phy supporting non-blocking line rate up to 20 X 100Gbps serdes

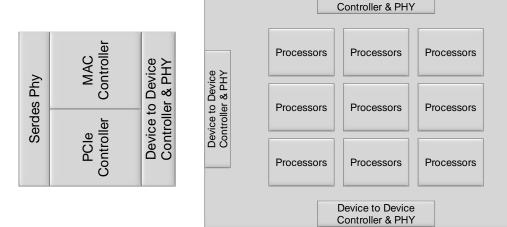
2. Scalable datapath processors (>1000+ core MIMD configurations)

3. Target process is advanced TSMC node/ product availability 2023; early access on Corigine MIMIC[™] emulation platform



DDR interface

DDR interface

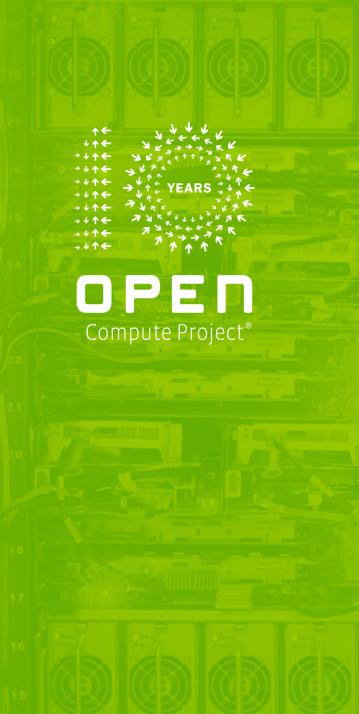




What is Next for ODSA at Corigine & NETRONCME

- Roadmap using (truly) open standards to offer a range of SmartNICs from 2x25G to 800Gbps
 - Propagate chiplet methodology to adjacent markets e.g. SDWAN etc.
- Composable Architecture that enables the integration of 3rd party chiplets with domain specific capabilities e.g. ML, photonic I/O chiplet etc.
- Demonstrable solutions based on heterogeneous technology (different process nodes, different foundries, different vendors)
- Early Ecosystem enablement through MIMIC[™] emulation platform of different chiplets
- Practical establishment of a chiplet marketplace through pragmatic demonstrable implementations (substrate modelling, packaging, test etc.)
- Provide Technical Leadership for the APAC ecosystem, establishing a regional chapter under the auspices of the OCP/ODSA leadership





Questions