OPEN Compute Project®

Community Led Hyperscale Open Innovation

OCP – ODSA Project

Commercialization Session

Bapi Vinnakota

Sub-Project Lead

The ODSA Sub-Project

- **Built from the ground up to address die disaggregation and IP reuse**
  - Available today and integrated in real designs.
  - Optimized for low latency, power, and manufacturing cost.
- **Our layered, non-prescriptive approach enables the widest range of products, price points, and applications for economies of scale**
- **We support truly open development**
  - Players of any size can readily contribute or even lead

Attendees and Participants:

Attendance and/or participation do not imply corporate endorsement

Semi Vendors
IP providers, EDA
Service providers

Tools, Manufacture, Design,
Test,
Integration

Systems vendors,
End users, ISVs, Service
Providers

OCP GLOBAL SUMMIT

ODSA Community

Workstream	Leader	Value	Output
ODSA	Bapi Vinnakota	First vertical protocol+PHY D2D stack	Specifications, 15+ refereed technical papers
Bunch of Wires	Elad Alon	First cross-technology scalable clock-forwarded PHY	BoW Draft Spec
Business	Ravi Agarwal	Largest ever OCP workshop Chiplet cost model	Chiplet cost model
CDX	David Ratchkov	First cross-industry open workflow models	Design flow white paper
Cross-PHY	Shahab Ardalan	Industry-standard objective metrics to compare D2D PHYs	Cross-PHY spreadsheet
End User	Dharmesh Jani	Structured flow of requirements	HipChips Conference
Link Layer	Open	Lightweight cross-protocol cross-PHY	DiPort controller
OpenHBI	Kenneth Ma	Leverage most popular chiplet technology	OpenHBI specification
Prototyping	JP Balachandran	Fully collaborative open, community-funded effort	BoW Test Chip ODSA Board Prototype

Estimating Production Readiness

Interop Issue	Status	Source
Chiplets with open interfaces sourced internally		
D2D PHY	BoW, Open HBI specifications maturing [18]	ODSA
	Channel models in flight (BoW test chip)	
D2D Transaction protocol	AXI, PCIe protocol adapters definitions available [21]	
Software development	Multi-company PoC platform (CPU, NIC available) [3]	
Chiplets sourced externally by a business arrangement		
Model data	Model catalog for behavior, power, mechanical, thermal, signal/power integrity, DRC/LVS. [3]	Various (IEEE, Commercial)
Test and validation	Access: IEEE 1848 [19]	IEEE
	Interconnect redundancy - die specific	
	Cross-die self-test	Open
Interop verification	Certifying compliance	
Chiplets sourced externally from a marketplace		
Business models	In flight with ODSA business workstream [3]	ODSA
Initialization, management & monitoring	Initialization	Open
	Management: Open, build off DMTF Redfish [24]	DMTF
	Monitoring	Open
Chiplet integrity and Security	Physical provenance, SEMI device traceability [25]	SEMI
	Logical integrity- open	IEEE
	Root of trust [24]	DMTF

2022 Plans

- **Support all efforts to advance an open chiplet ecosystem**
  - Collaborate with UCIe –
    - e.g., align the second generation of our work - OpenHBI, BoW, DiPort, Link Layer…
    - Some ODSA work is entirely complementary - CDX, Chiplet business model, KGD model
  - Continue to collaborate with the IEEE, Chips Alliance,…
- **Continue the great work we have been doing!**
  - ODSA solutions are the only game in town optimized for die disaggregation
  - ODSA solutions are geared for all use cases and not just compute centric
- **Multiple chips/test-chips are in flight, and an ecosystem is already forming – today's session**