3D Test: Problem Statement

- Address both pre- and post-bond die testing
- Address both partial and full stack testing
- Modular tests to cover
  - die internals
  - die to die interconnect
  - die to board/package connections
- Leverage existing (and emerging) standards: 1149.1/6, 1500, 1687, 1838, Jedec
Die-level DFT Infrastructure

- Embedded Scan
- JTAG (1149.1/6)
- PTAM (Power Test Access Management)
- OPCG / OCC
- MBIST
- LBIST
- Compression
- Process Monitors

Example Die with 1149.1
3D Stack DFT Architecture - Concept

- Die-level wrapper - 1500 / 1149.1
- Die has dedicated probe pads for pre-bond test
- Die has a few dedicated TSVs for post-bond test
3D Test Mode Set-up Example

Building On Existing Standards

- **IEEE 1149.1 (aka JTAG)**
  - 5 pin Test Access Port (TAP)
  - Used for isolation and access at the board
- **IEEE 1500**
  - Wrapper for cores
  - Used for isolation and access at the SoC
- **JEDEC standards:**
  - JESD229- Wide I/O Single Data Rate,
  - JESD229-2 Wide I/O 2
  - JESD235B High Bandwidth Memory DRAM
- **IEEE 1839**
  - Serial control mechanism
  - Die wrapper register (DWR)
  - Flexible parallel port (FPP)