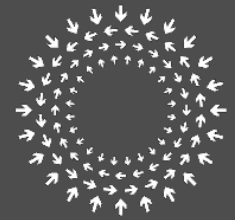

ODSA: Proof OF Concept (POC)

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Jayaprakash Balachandran, Cisco
Jawad Nasrullah, zGlue Inc

ODSA Project Workshop

June 10, 2019

Consume. Collaborate. Contribute.

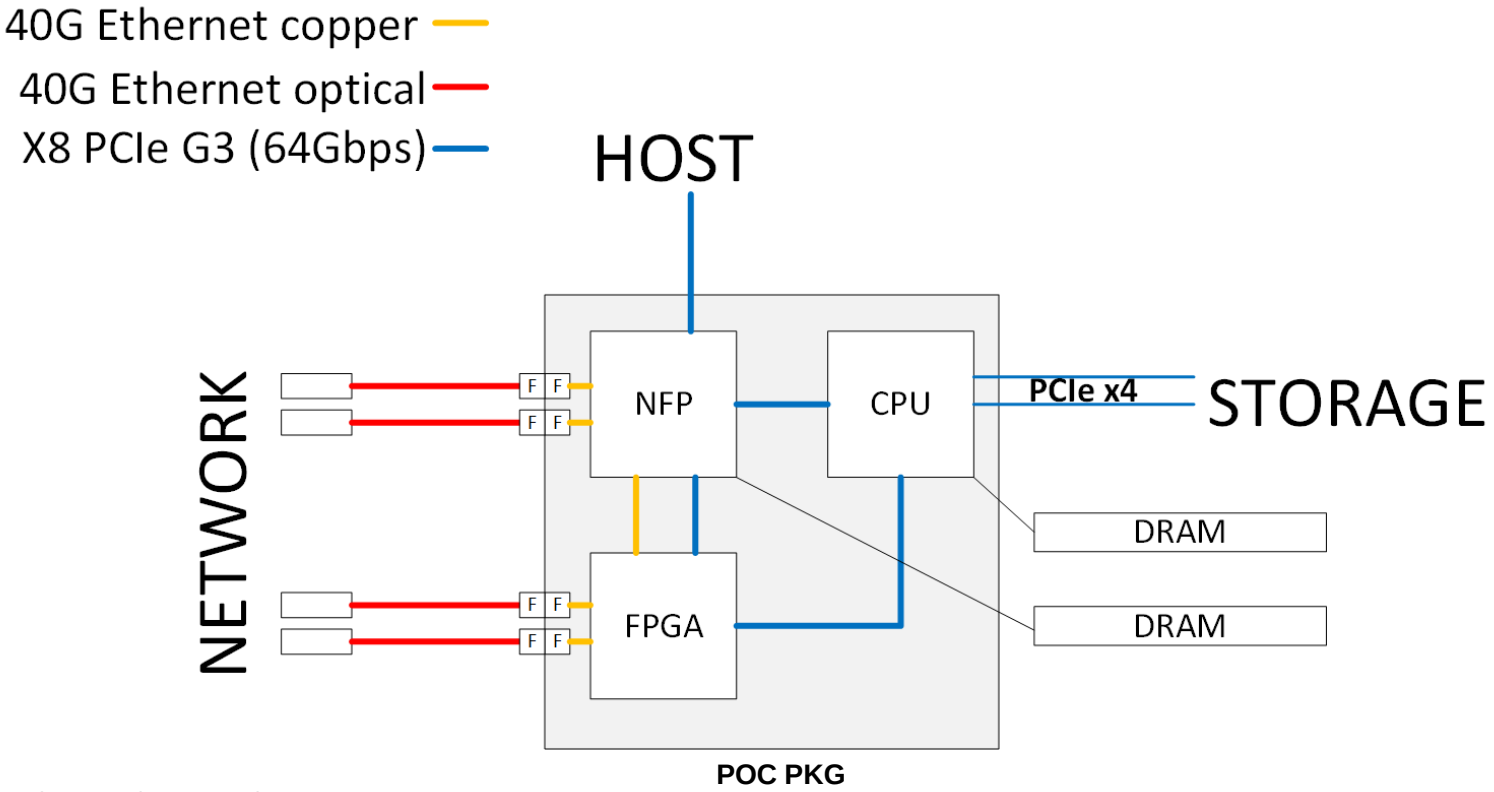
Why do a Proof-of-Concept

- Learn
- Reduce Risk
- Convince Skeptics

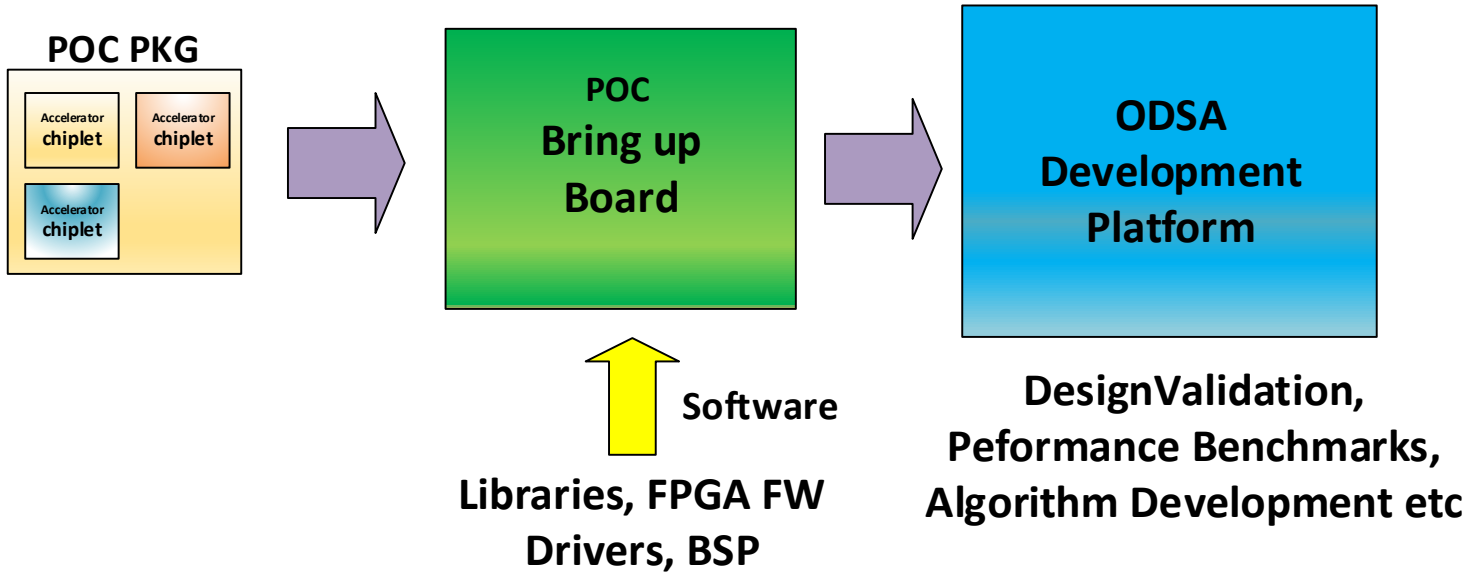
Multiple dimensions of POC

- Architectural
  - Validate interfaces protocols
  - Evaluate performance issues
  - **Develop software programming models**
- Physical
  - Explore chiplet integration and packaging
  - Validate power distribution
  - Develop high-speed I/O solutions
- Business
  - Force information sharing at a bare die-level
  - Exposing issues of sharing sensitive business metrics
  - Validate risk and value sharing models

POC Architecture



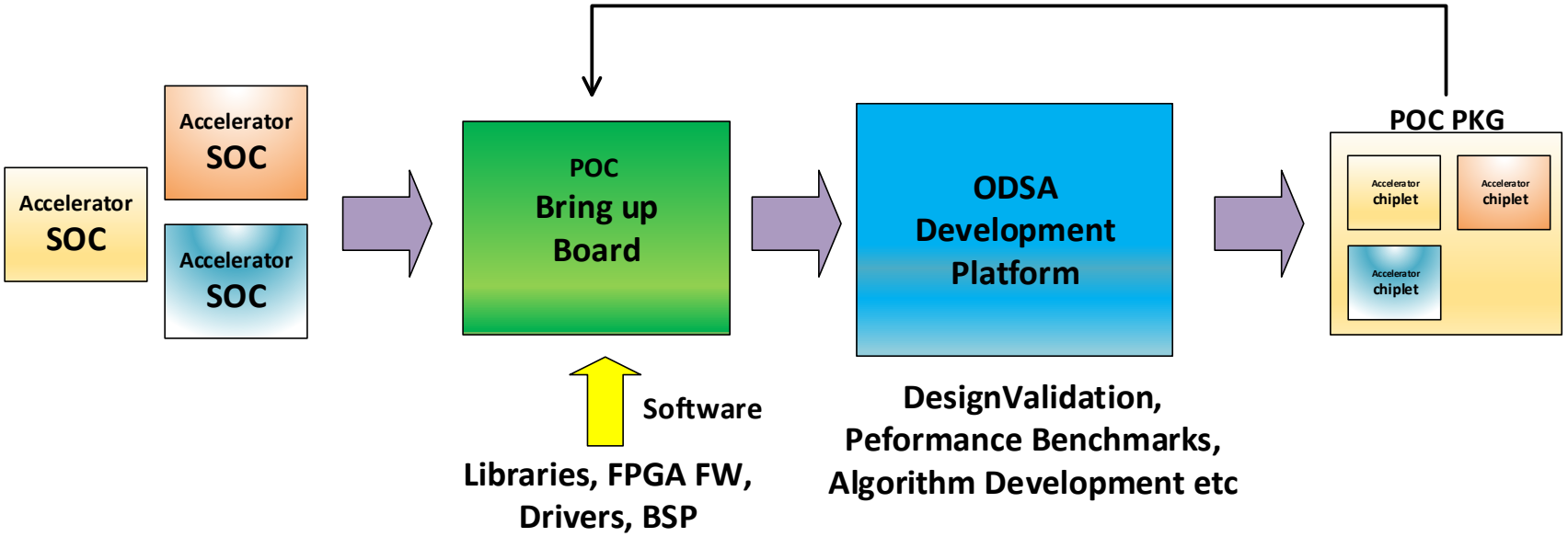
ODSA POC Platform Development Flow



PoC Package Design Challenges

- Package Fabrication, Assembly and Test is Expensive
- Package design is challenging with 3 Large multivendor chiplets
  - Prone to Errors
  - Limited resources
- Evolving Architecture
  - Need to Test drive before commit

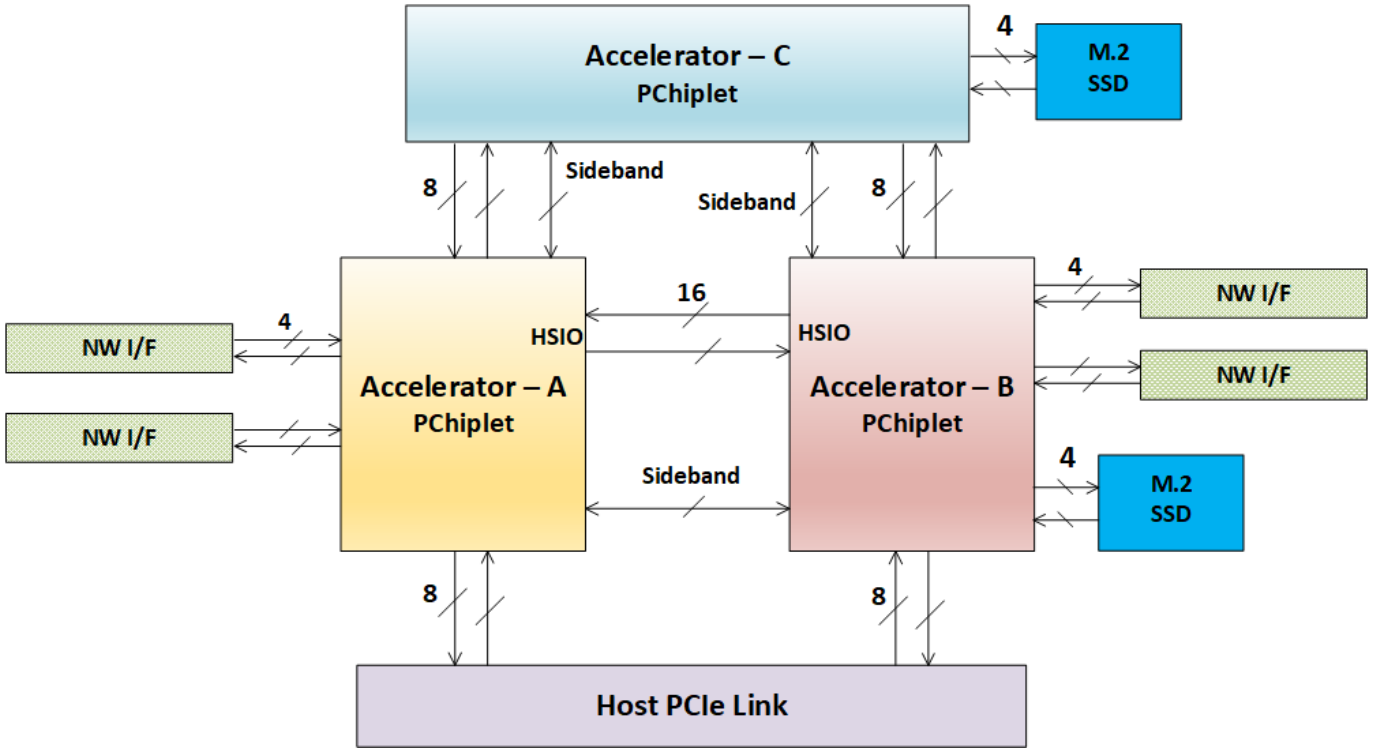
ODSA POC Platform Development Flow to Mitigate Package Design Risks



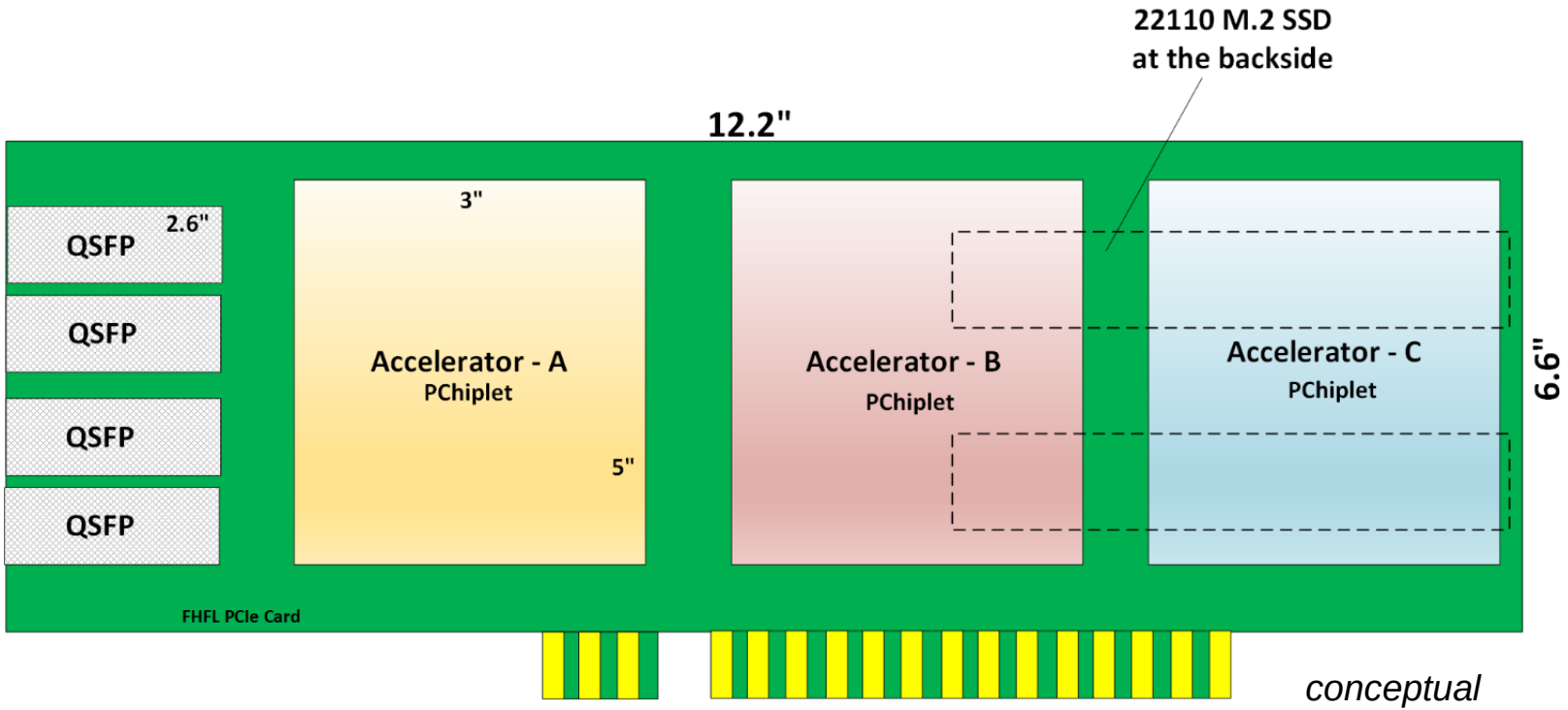
POC Bringup Platform Requirements

- Disaggregated Architecture enabling independent design and test of Accelerator SOCs
  - Ease of Component Upgrades & Debug
  - Enable Different Architecture Evaluation
- Support various Domain Specific Acceleration Use Cases
- Flexible Form Factor
  - Attached directly to server host
  - Standalone operation

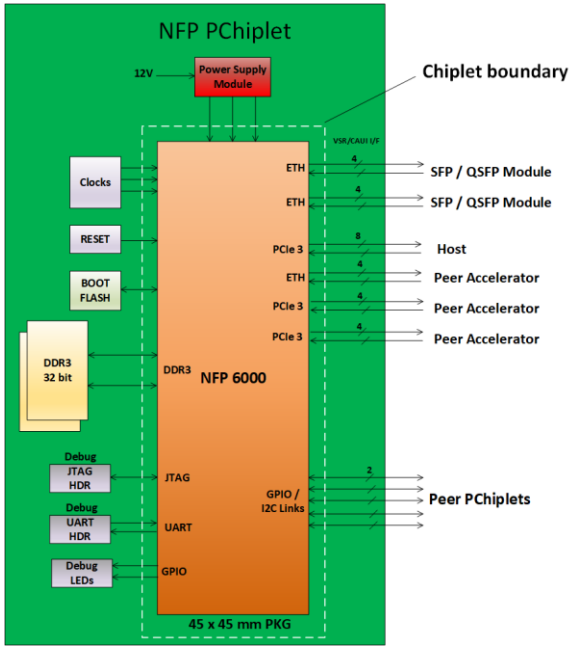
POC Bring up Platform Architecture

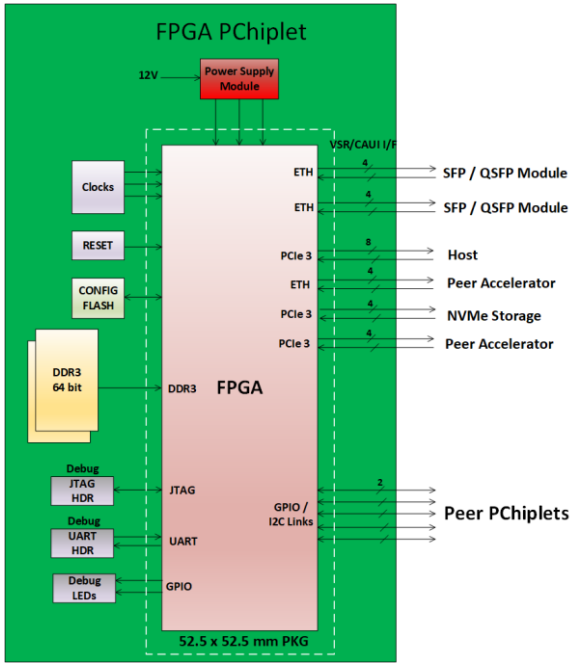


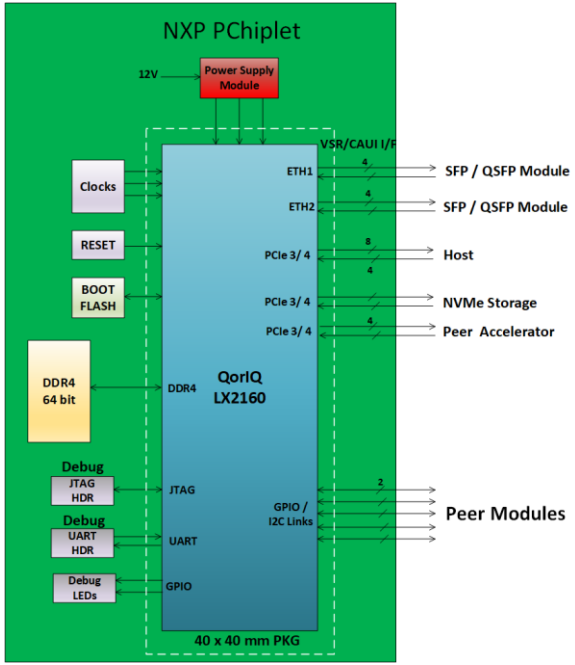
POC Bringup Platform Physical Implementation



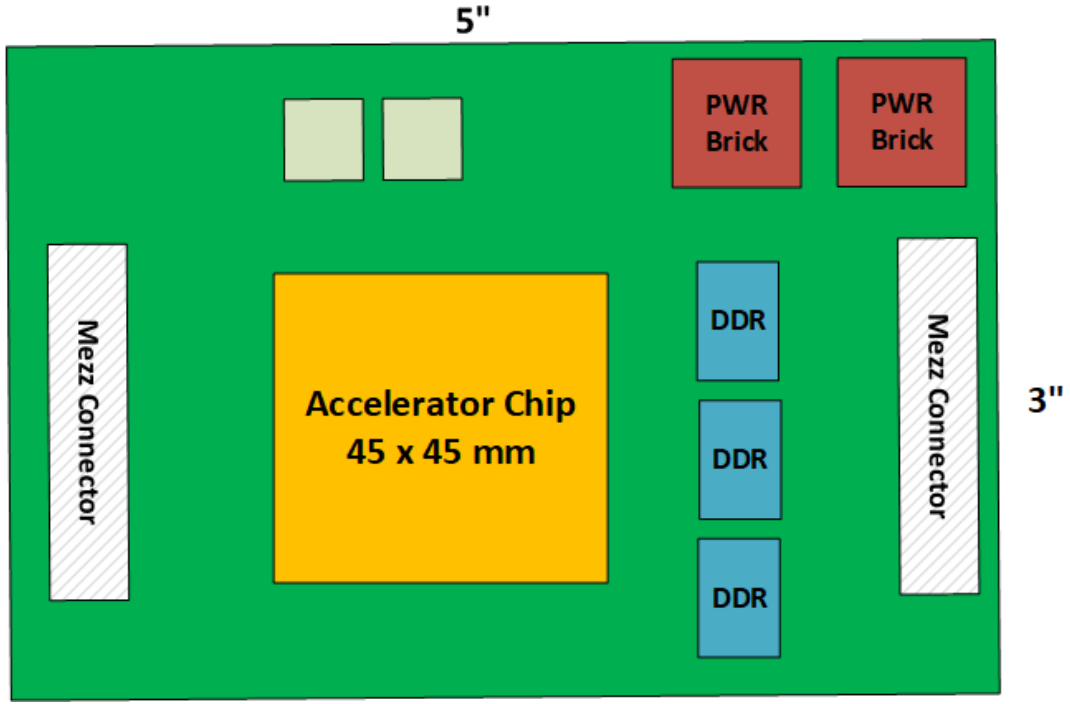
PChiplet Architectures







PChiplet Physical Implementation

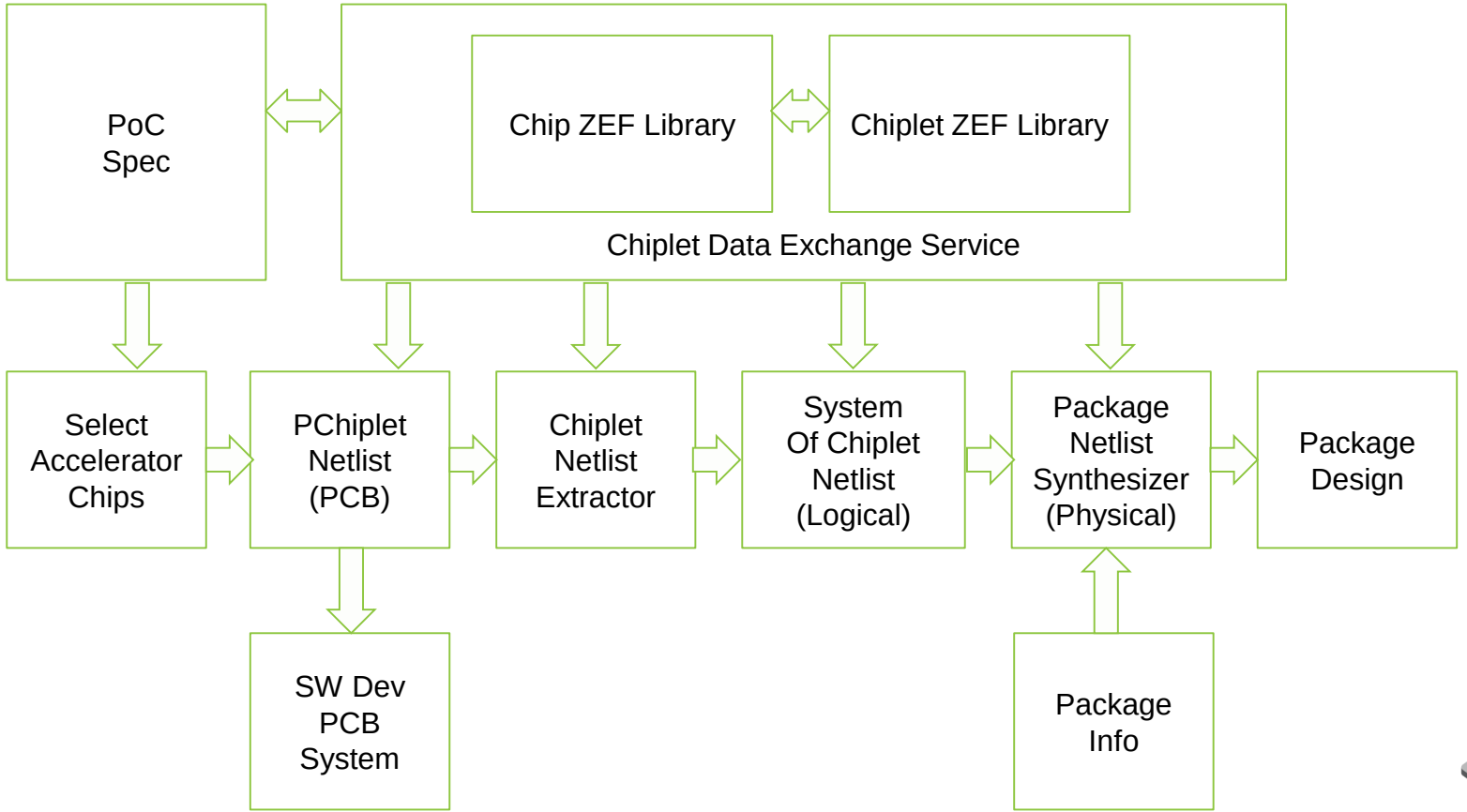


conceptual

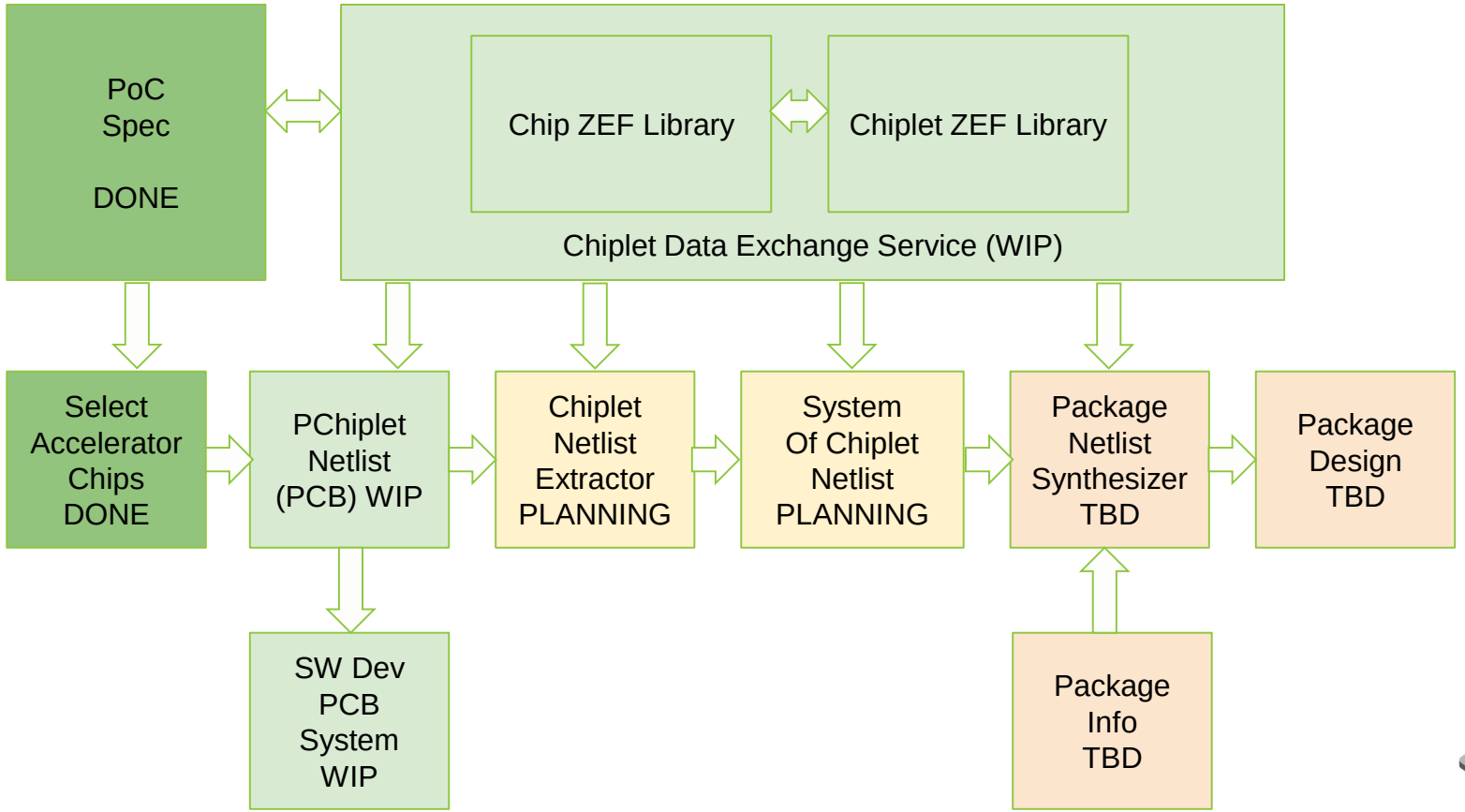
POC Implementation Summary

- POC Package Design Challenges
- Disaggregated Pchiplet based PCB first design to mitigate design risks
- Flexible Platform for Architecture Evaluation
- How to Automate PCB netlist to PKG netlist ?

POC Design Process



POC Design Process



PoC Work Schedule

	2019										2020		
Tasks	**Mar**	**Apr**	**May**	**Jun**	**Jul**	**Aug**	**Sep**	**Oct**	**Nov**	**Dec**	**Jan**	**Feb**	**Mar**
Architecture and Overall	Component Selection, Arch												
PoC SDV Design				Schematics		Layout	Mfg	Bring Up					
PoC Package Design					Design								
Packge Manufacturing										Mfg			
Software/Firmware (Bring UP and demo)											Bring UP		

Please Join Us

We are looking for fellow travellers for all areas

- Specification Write Ups
- System Netlist Verification
- Board Design
- Board Bring Up
- Package Design
- System Level Test Development
- Sponsor Board Manufacturing
- Sponsor Package Manufacturing

Reach out to jawad@zglue.com

Consume. Collaborate. Contribute.

Backup