ODSA: Proof OF Concept (POC)

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ODSA Project Workshop
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Why do a Proof-of-Concept

- Learn
- Reduce Risk
- Convince Skeptics
Multiple dimensions of POC

• Architectural
  - Validate interfaces protocols
  - Evaluate performance issues
  - **Develop software programming models**

• Physical
  - Explore chiplet integration and packaging
  - Validate power distribution
  - Develop high-speed I/O solutions

• Business
  - Force information sharing at a bare die-level
  - Exposing issues of sharing sensitive business metrics
  - Validate risk and value sharing models
POC Architecture

40G Ethernet copper
40G Ethernet optical
X8 PCIe G3 (64Gbps)
ODSA POC Platform Development Flow

POC PKG

- Accelerator chiplet
- Accelerator chiplet
- Accelerator chiplet

POC Bring up Board

- Software
- Libraries, FPGA FW
- Drivers, BSP

ODSA Development Platform

- DesignValidation, Performance Benchmarks, Algorithm Development etc
PoC Package Design Challenges

• **Package Fabrication, Assembly and Test is Expensive**
• **Package design is challenging with 3 Large multivendor chiplets**
  - Prone to Errors
  - Limited resources
• **Evolving Architecture**
  - Need to Test drive before commit
ODSA POC Platform Development Flow to Mitigate Package Design Risks

- Consume
- Collaborate
- Contribute

Accelerator SOC

Bring up Board

Software Libraries, FPGA FW, Drivers, BSP

Design Validation, Performance Benchmarks, Algorithm Development etc

POC PKG

Accelerator chiplet

Accelerator chiplet

Accelerator chiplet

Accelerator chiplet
POC Bringup Platform Requirements

- Disaggregated Architecture enabling independent design and test of Accelerator SOCs
  - Ease of Component Upgrades & Debug
  - Enable Different Architecture Evaluation
- Support various Domain Specific Acceleration Use Cases
- Flexible Form Factor
  - Attached directly to server host
  - Standalone operation
POC Bring up Platform Architecture
POC Bringup Platform Physical Implementation

22110 M.2 SSD at the backside

Accelerator - A
PChiplet

Accelerator - B
PChiplet

Accelerator - C
PChiplet

FHFL PCIe Card

conceptual
PChiplet Architectures

NFP PChiplet
- Chiplet boundary
- SFP / QSFP Module
- Host
- PCIe x1
- PCIe x4
- PCIe x8
- DDR3 8GB
- DDR4 16GB
- GPD / I2C Links
- Peer PChiplets

FPGA PChiplet
- Chiplet boundary
- SFP / QSFP Module
- Host
- PCIe x1
- PCIe x4
- PCIe x8
- DDR3 8GB
- DDR4 16GB
- GPD / I2C Links
- Peer PChiplets

NXP PChiplet
- Chiplet boundary
- SFP / QSFP Module
- Host
- PCIe x1
- PCIe x4
- PCIe x8
- DDR4 16GB
- GPD / I2C Links
- Peer Modules

PChiplet Physical Implementation

Accelerator Chip
45 x 45 mm

conceptual
POC Implementation Summary

- POC Package Design Challenges
- Disaggregated Pchiplet based PCB first design to mitigate design risks
- Flexible Platform for Architecture Evaluation
- How to Automate PCB netlist to PKG netlist?
POC Design Process

PoC Spec

Select Accelerator Chips

PChiplet Netlist (PCB)

Chiplet Netlist Extractor

System Of Chiplet Netlist (Logical)

Package Netlist Synthesizer (Physical)

Package Design

Chip ZEF Library

Chiplet ZEF Library

Chiplet Data Exchange Service

SW Dev PCB System

Package Info
POC Design Process

- PoC Spec
  - DONE
- Select Accelerator Chips
  - DONE
- PChiplet Netlist (PCB) WIP
- SW Dev PCB System WIP
- Chip ZEF Library
- Chiplet ZEF Library

- Chiplet Data Exchange Service (WIP)
- System Of Chiplet Netlist PLANNING
- Package Netlist Synthesizer TBD
- Package Design TBD
- Package Info TBD
## PoC Work Schedule

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*Consume. Collaborate. Contribute.*
Please Join Us

We are looking for fellow travellers for all areas

- Specification Write Ups
- System Netlist Verification
- Board Design
- Board Bring Up
- Package Design
- System Level Test Development
- Sponsor Board Manufacturing
- Sponsor Package Manufacturing

Reach out to jawad@zglue.com
Backup