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Lightning Talk - OAI Workstreams Update : High Speed, System and Power

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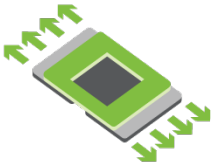
Lightning Talk - OAI Workstream Update: High Speed, System and Power

Song Kok Hang, Principal Engineer, Intel
Chuang Ruan, FAE, Wiwynn
Anthony Chan, Electrical Engineer, Facebook

High Speed Workstream Update

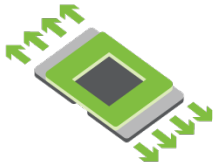


OPEN ACCELERATOR INFRASTRUCTURE

OAM v2.0 Update

- Spec Release – Q2/Q3 2022
- New Form Factor – 170mm x 102mm
- Support 112G-PAM4 and PCIe Gen5/6
- Support > 1KW Module TDP with Dual Power Entries

OAM v2.0 Form Factor



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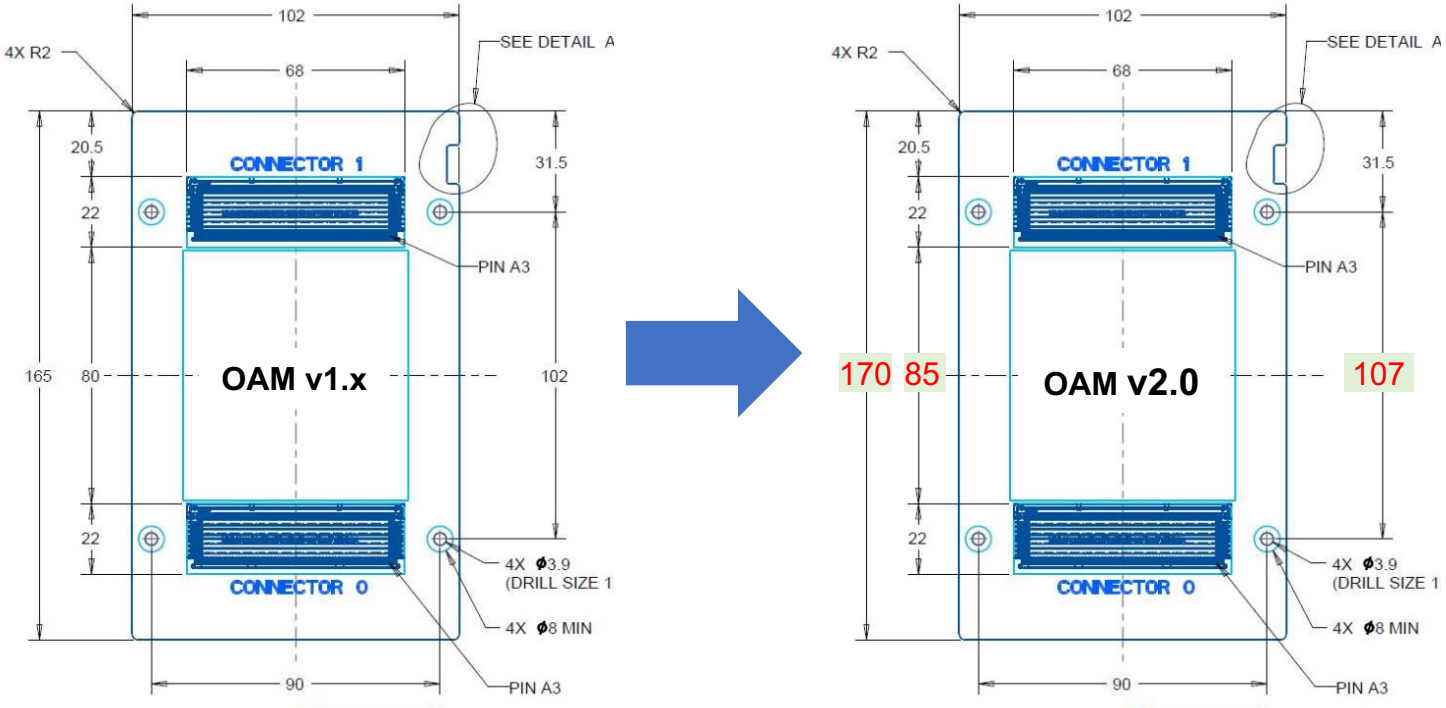

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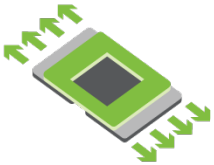
OAI v2.0 End to End Channel Budget



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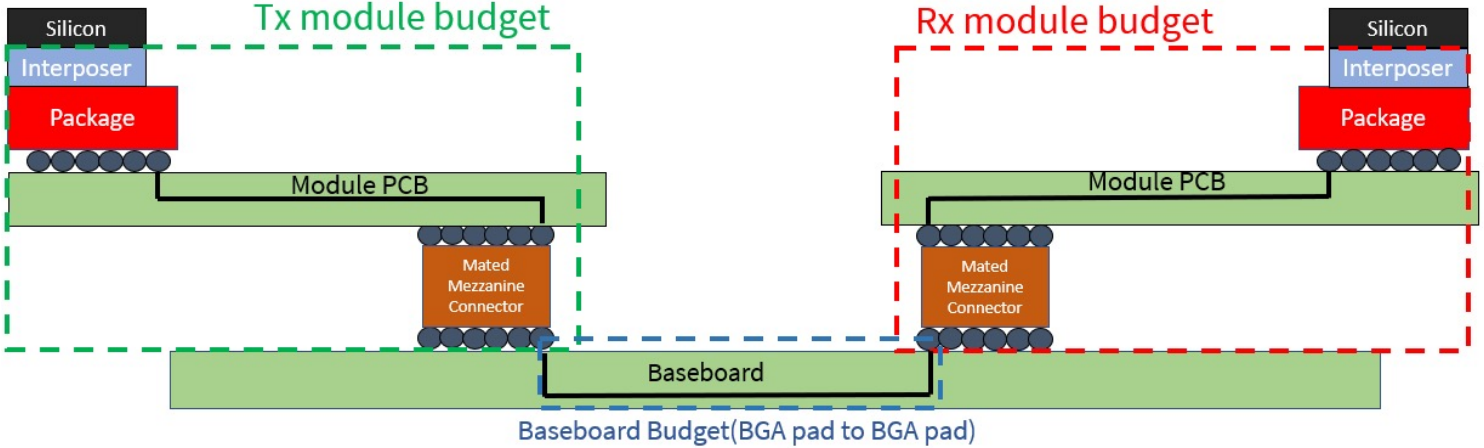
- OAM/UBB v2.0 Total Channel Loss Budget (28GHz): 28-30dB
  - OAM Tx (**8dB**) + UBB (**12-14dB**) + OAM Rx (**8dB**)



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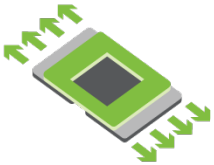
SI Challenges with New Topologies



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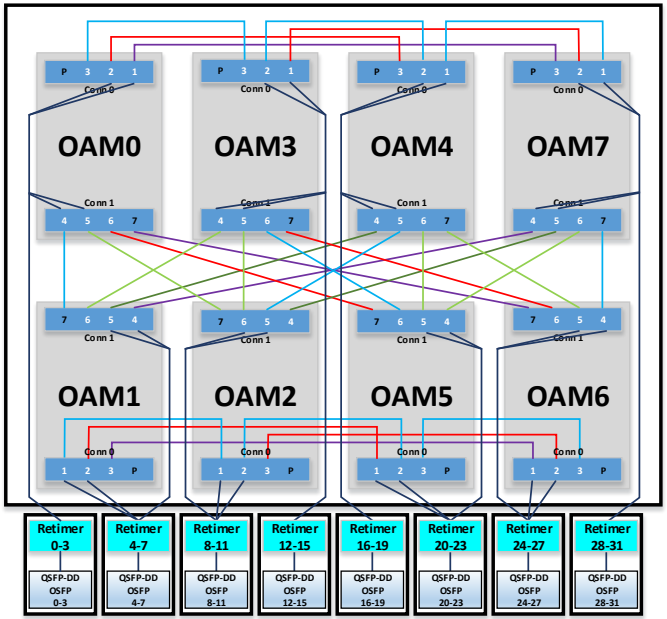
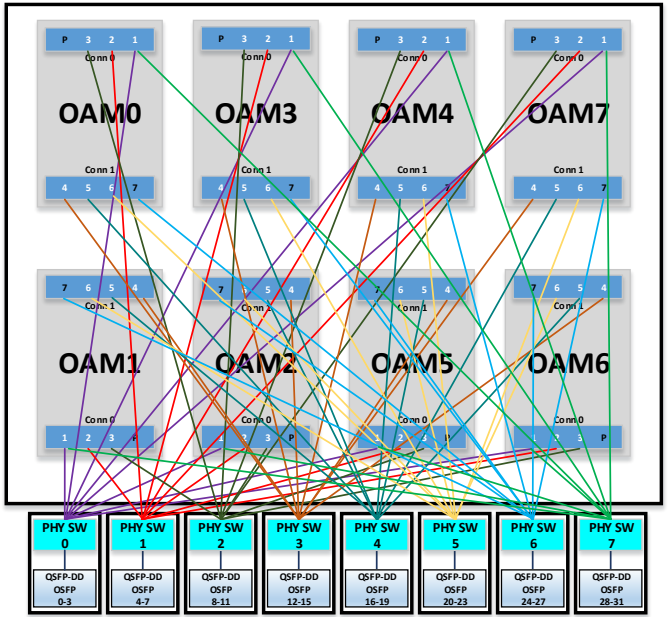
7 Scale Up + 4 Scale Out Topology



8 Switch Based SU/SO Topology



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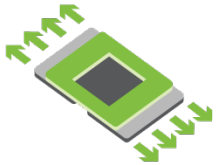
System Workstream Update



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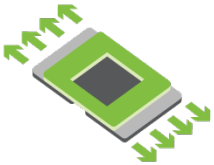
UBB v1.5 Update

- 112G-PAM4 with Improved SI Performance Molex MMPro Connector
- PCIe Gen5
- 700W PI Assessment
- 112G-PAM4 End to End Channel Assessment Test Fixture

UBB v2.0 Update

- Design and SI Challenges with 32 Scale Out Ports
- 112G-PAM4 and PCIe Gen5/6 **SI Test Fixture**
- 1KW **PI Test Fixture**

UBB v1.5 Update



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PCB Material

UBB v1.0 Reference Design – Ultra Low Loss Material

- @14GHz (loss/inch): **~0.88dB**

UBB v1.5 Reference Design – Hyper/Extreme Low Loss Material

- @28GHz (loss/inch): **0.73 – 0.92dB**

Material	Stack up (Core/PP)	Loss @28GHz	UBB Length (Inch)
Vendor A	4/5	0.92	14.2
Vendor A	5/6	0.73	17.8
Vendor B	4/5	0.85	15.3
Vendor B	5/6	0.78	16.7

UBB v1.5 Update

Mezzanine Connector (90ohm)

OAM/UBB v1.0 – Molex Mirror Mezz

OAM/UBB v1.5 – Molex Mirror Mezz Pro

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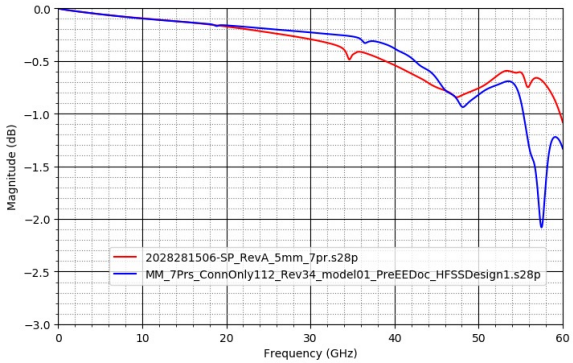
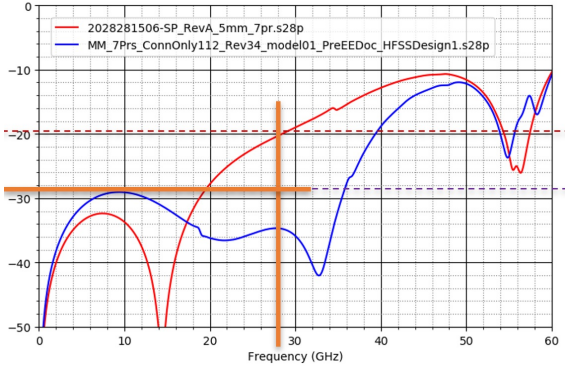
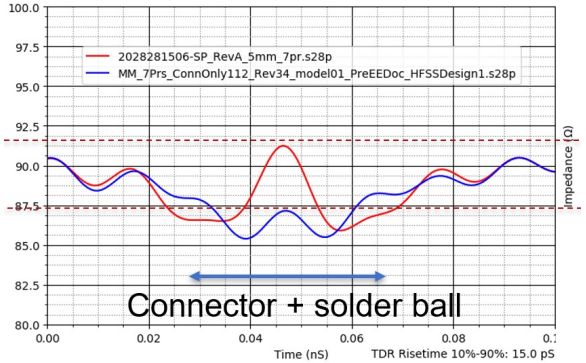
IL



RL



TDR



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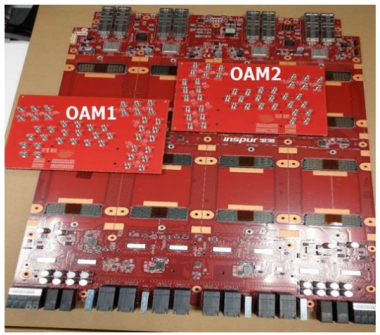
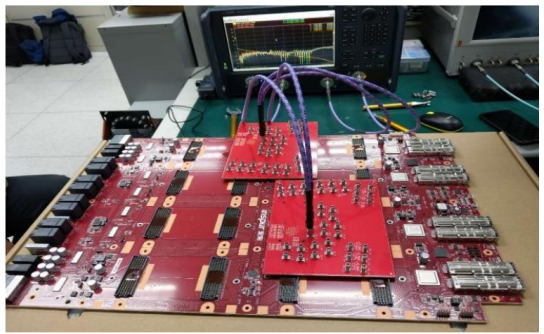
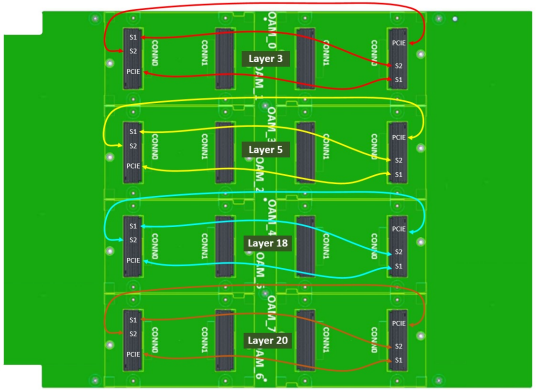
UBB v1.5 Update

112G-PAM4 Test Fixture

	Port	OAM Layer	OAM Length (inch)	MMPro Loss (dB)	SMA Loss (dB)	OAM Via Loss (dB)	OAM Loss (dB)	UBB Lenght (inch)	UBB Length Loss (dB)	UBB Via Loss (dB)	UBB Total Loss (dB)	UBB Layer	OAM Length (inch)	MMPro Loss (dB)	SMA Loss (dB)	OAM Via Loss (dB)	OAM Loss (dB)	OAM Layer	Port	
OAM1	S1_RX[12]	L5	7.99	0.21	0.25	0.71	8	15.20	13.00	1.00	14.00	L3	7.99	0.21	0.25	0.71	8	L9	S2_RX[8]	
	S2_RX[8]	L9	7.99	0.21	0.25	0.71	8	15.20	13.00	1.00	14.00	L3	7.99	0.21	0.25	0.71	8	L26	PCIE_RX[8]	OAM0
	PCIE_RX[8]	L26	7.99	0.21	0.25	0.71	8	15.20	13.00	1.00	14.00	L3	7.99	0.21	0.25	0.71	8	L5	S1_RX[12]	
OAM2	S1_RX[12]	L5	7.99	0.21	0.25	0.71	8	15.20	13.00	1.00	14.00	L5	7.99	0.21	0.25	0.71	8	L9	S2_RX[8]	
	S2_RX[8]	L9	7.99	0.21	0.25	0.71	8	15.20	13.00	1.00	14.00	L5	7.99	0.21	0.25	0.71	8	L26	PCIE_RX[8]	OAM3
	PCIE_RX[8]	L26	7.99	0.21	0.25	0.71	8	15.20	13.00	1.00	14.00	L5	7.99	0.21	0.25	0.71	8	L5	S1_RX[12]	
OAM5	S1_RX[12]	L5	7.99	0.21	0.25	0.71	8	15.20	13.00	1.00	14.00	L19	7.99	0.21	0.25	0.71	8	L9	S2_RX[8]	
	S2_RX[8]	L9	7.99	0.21	0.25	0.71	8	15.20	13.00	1.00	14.00	L19	7.99	0.21	0.25	0.71	8	L26	PCIE_RX[8]	OAM4
	PCIE_RX[8]	L26	7.99	0.21	0.25	0.71	8	15.20	13.00	1.00	14.00	L19	7.99	0.21	0.25	0.71	8	L5	S1_RX[12]	
OAM6	S1_RX[12]	L5	7.99	0.21	0.25	0.71	8	15.20	13.00	1.00	14.00	L20	7.99	0.21	0.25	0.71	8	L9	S2_RX[8]	
	S2_RX[8]	L9	7.99	0.21	0.25	0.71	8	15.20	13.00	1.00	14.00	L20	7.99	0.21	0.25	0.71	8	L26	PCIE_RX[8]	OAM7
	PCIE_RX[8]	L26	7.99	0.21	0.25	0.71	8	15.20	13.00	1.00	14.00	L20	7.99	0.21	0.25	0.71	8	L5	S1_RX[12]	







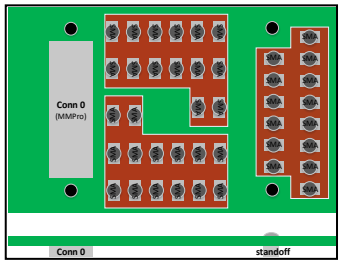


Figure 6: UBB Measurement Setting

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UBB v2.0 Update

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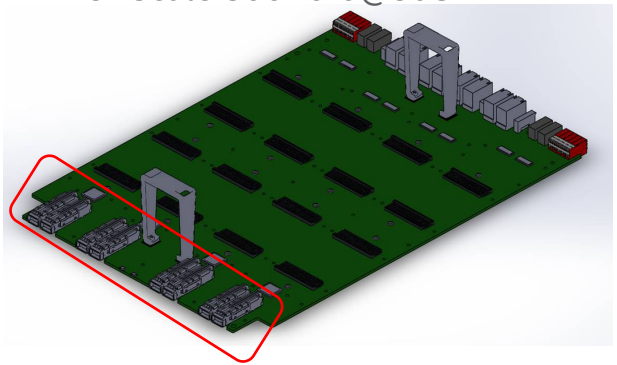
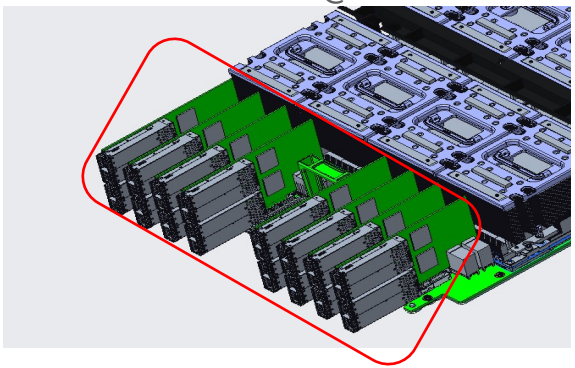
Design and SI Challenges with 32 Scale Out Ports

- UBB SerDes Routing
- OAM to UBB to Scale Out Card SI Assessment
- Form Factor Fit in 4U UBB Tray
- Thermal Challenges

UBB v1.x
8x Scale Out Port @56G-PAM4



UBB v2.0
32x Scale Out Port @112G-PAM4



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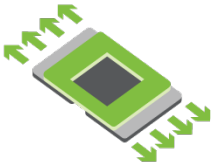
Power Workstream Update



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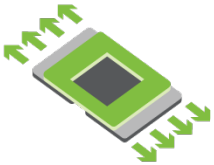
UBB v2.0 Update

- Trending Power Architecture

OAM v2.0 Update

- Dual Power Entries Approach
- Excursion Design Power (EDP) Guidelines

Trending Power Architecture*



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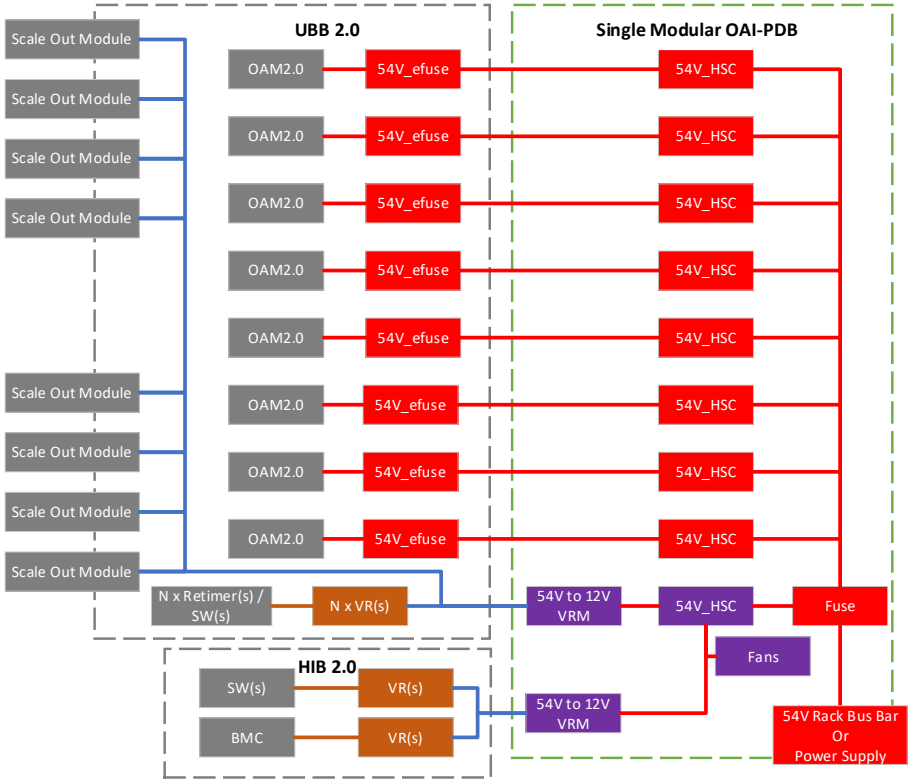
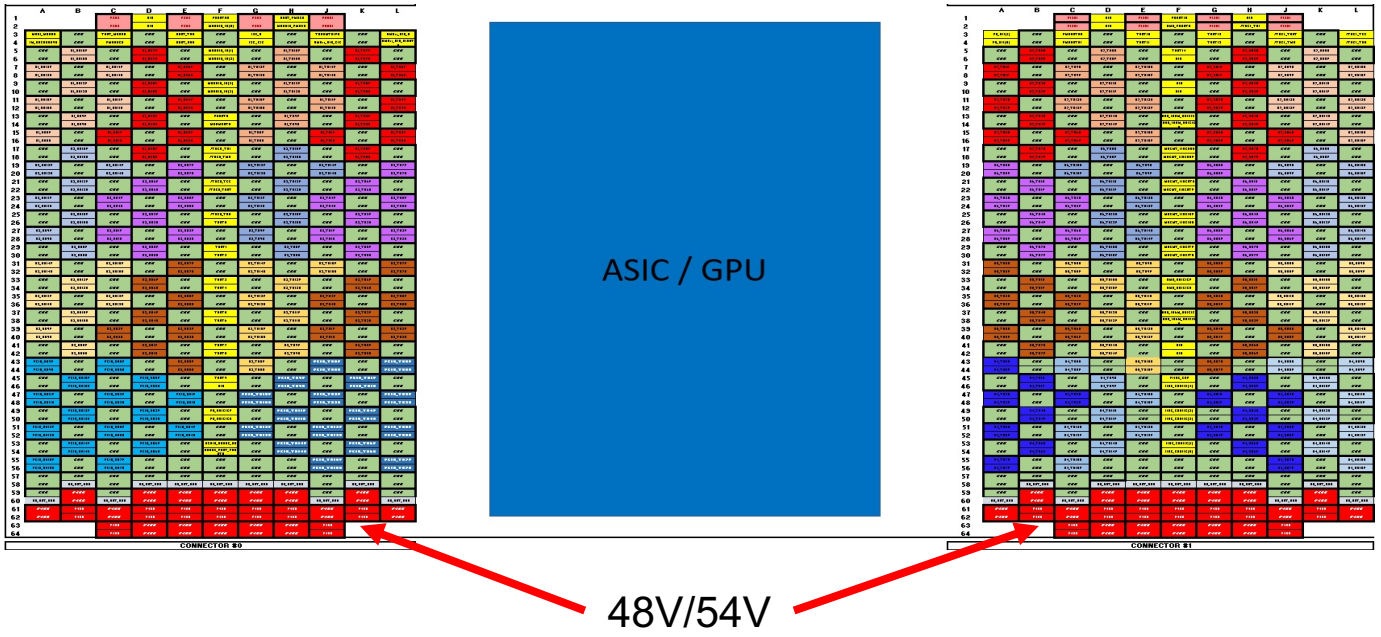


1. Single Modular PDB Approach
2. Simplified Design (48V/54V OAMs only)
3. Optimize End to End Power Efficiency

OPEN POSSIBILITIES.

*Only high-power paths shown, miscellaneous/standby power not finalized at this time

OAM v2.0 Dual Power Entries



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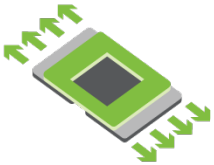
OAM v2.0 EDP Guidelines*



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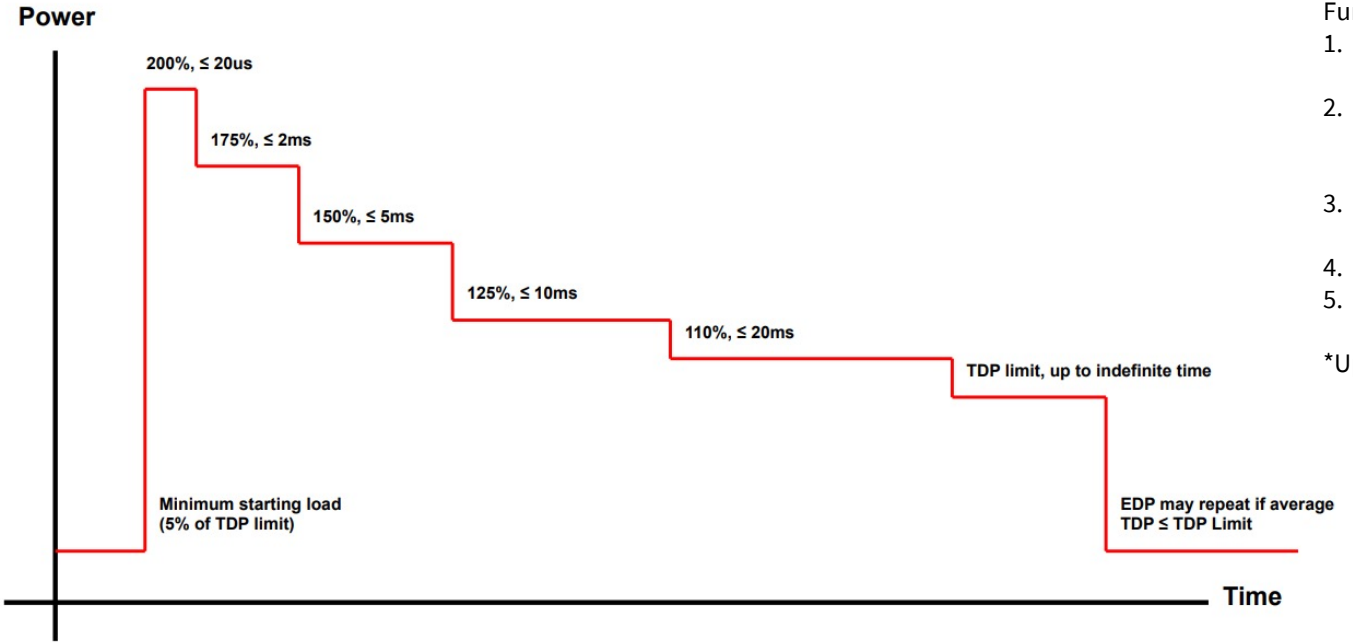
- Improve Interoperability of OCP-OAI Ecosystem
- Opportunity to Align on Common EDP Profile
- Minimize Stranded Power in Data Centers

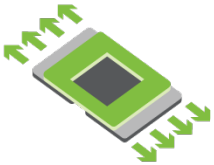


Fundamental underlying assumptions:

1. Average power over time must be ≤ TDP limit
2. Iterative EDP peaks must occur in descending staircase order and within duration limits
3. EDP events are absolute worst case peak conditions (not averaged over time)
4. Minimum starting load at 5% of TDP limit
5. EDP scales with TDP, otherwise upper limit shall be 1kW*

*Upper limit may differ between ODM vendors

Call to Action



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Get involved in the project:

OCP Server Project: https://www.opencompute.org/projects/server

OAI Subgroup: https://www.opencompute.org/wiki/server/OAI

OAI Mailing List: https://oc-all.goup.io/g/OCP-OAI

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Thank you!

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